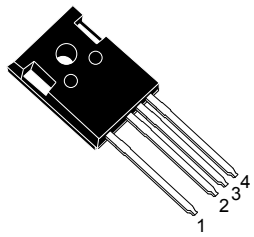
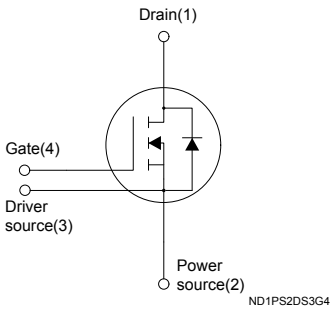
STW69N65M5-4

Datasheet

N-channel 650 V, 37 mΩ typ., 58 A MDmesh M5 Power MOSFET in a TO247-4 package



TO247-4



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STW69N65M5-4	650 V	45 mΩ	58 A

- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance thanks to the extra driving source pin
- Extremely low $R_{DS(on)}$
- 100% avalanche tested

Applications

- High efficiency switching applications:
  - Servers
  - PV inverters
  - Telecom infrastructure
  - Multi kW battery chargers

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Product status link
STW69N65M5-4

Product summary	
Order code	STW69N65M5-4
Marking	69N65M5
Package	TO247-4
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	58	A
	Drain current (continuous) at T_C = 100 °C	36.5	
I_{DM}(1)	Drain current (pulsed)	232	A
P_{TOT}	Total power dissipation at T_C = 25 °C	330	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Maximum operating junction temperature	150	°C

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 58 A, di/dt ≤ 400 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*
3. *V_{DD} ≤ 640 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.38	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	50	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	12	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	1410	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C(1)	-	-	100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V	-	-	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 29 A	-	37	45	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	6420	-	pF
C_{oss}	Output capacitance		-	170	-	pF
C_{rss}	Reverse transfer capacitance		-	11	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	536	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	146	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	1.3	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 29 A, V_{GS} = 0 to 10 V (see the Figure 15)	-	143	-	nC
Q_{gs}	Gate-source charge		-	38	-	nC
Q_{gd}	Gate-drain charge		-	64	-	nC

1. *$C_{o(tr)}$ is an equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.*
2. *$C_{o(er)}$ is an equivalent capacitance that provides the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 38 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 16, and the Figure 19)	-	102	-	ns
$t_{r(v)}$	Voltage rise time		-	10	-	ns
$t_{f(i)}$	Current fall time		-	11.5	-	ns
$t_{c(off)}$	Crossing time		-	14.5	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	58	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	232	A
V_{SD}(2)	Forward on voltage	I_{SD} = 58 A, V_{GS} = 0 V	-	-	1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 58 A, di/dt = 100 A/µs, V_{DD} = 100 V (see the Figure 16)	-	480	-	ns
Q_{rr}	Reverse recovery charge		-	11	-	µC
I_{RRM}	Reverse recovery current		-	46	-	A
t_{rr}	Reverse recovery time	I_{SD} = 58 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_J = 150 °C (see the Figure 16)	-	592	-	ns
Q_{rr}	Reverse recovery charge		-	16	-	µC
I_{RRM}	Reverse recovery current		-	53	-	A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics curves

Figure 1. Safe operating area

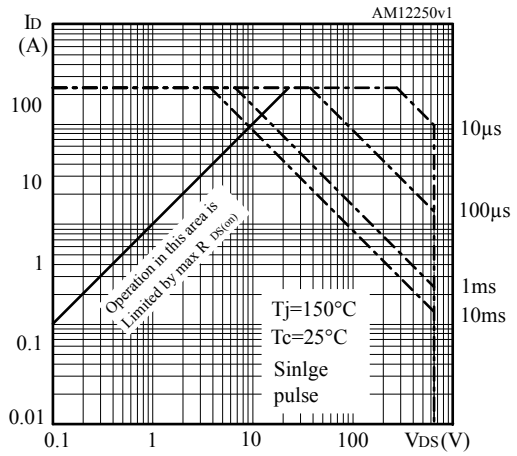


Figure 2. Normalized transient thermal impedance

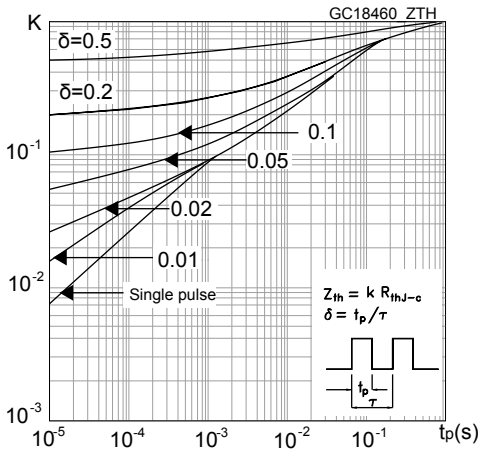


Figure 3. Typical output characteristics

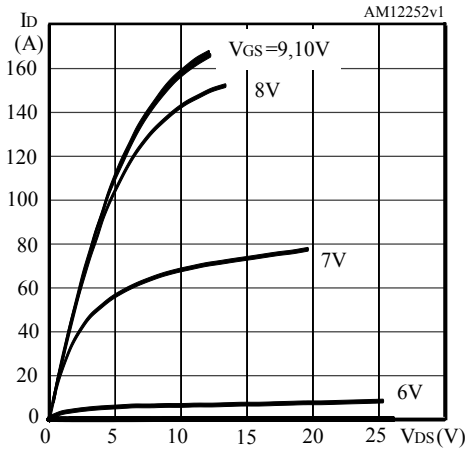


Figure 4. Typical transfer characteristics

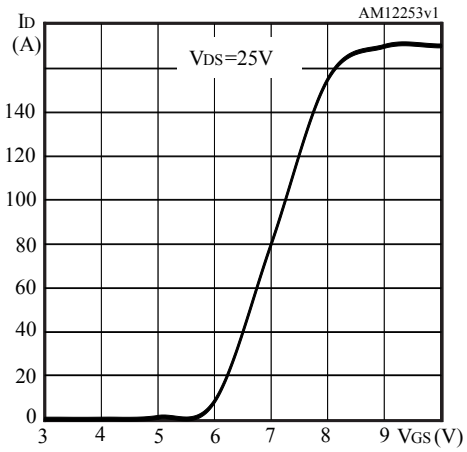


Figure 5. Typical gate charge characteristics

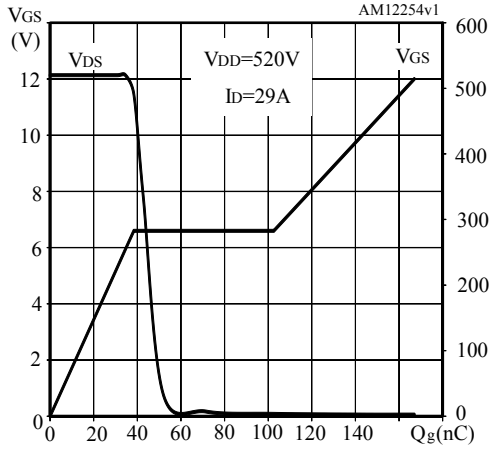


Figure 6. Typical drain-source on-resistance

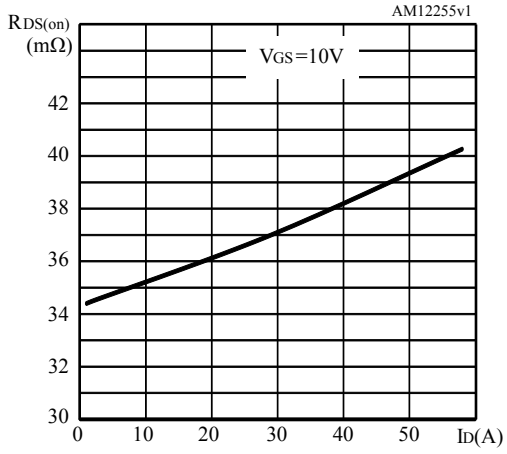


Figure 7. Typical capacitance characteristics

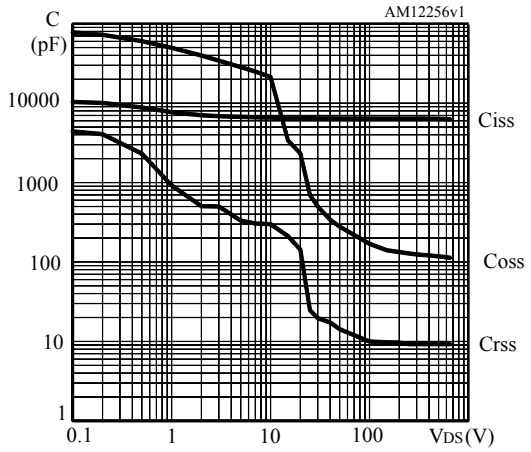


Figure 8. Typical output capacitance stored energy

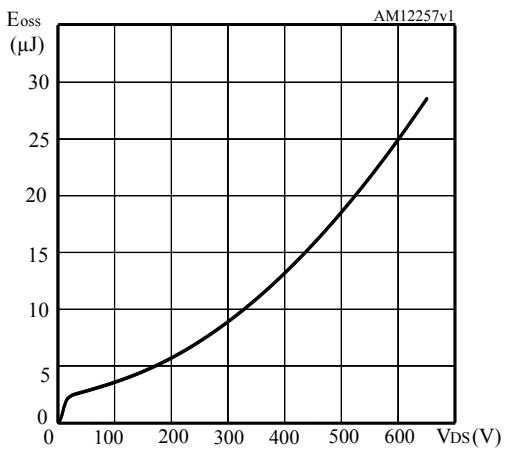


Figure 9. Normalized gate threshold vs temperature

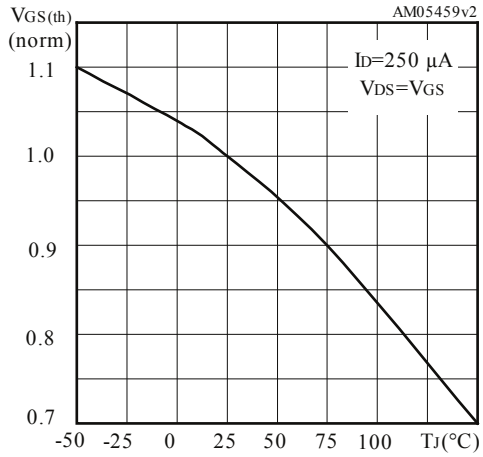


Figure 10. Normalized on-resistance vs temperature

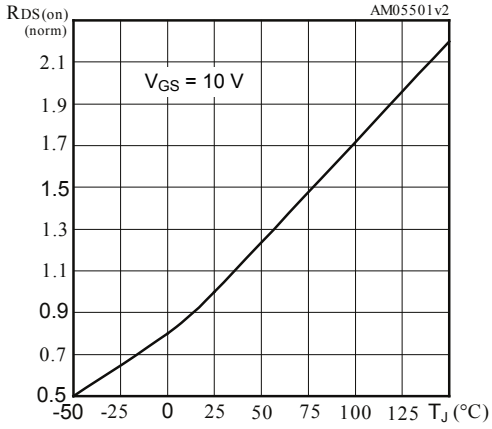


Figure 11. Typical reverse diode forward characteristics

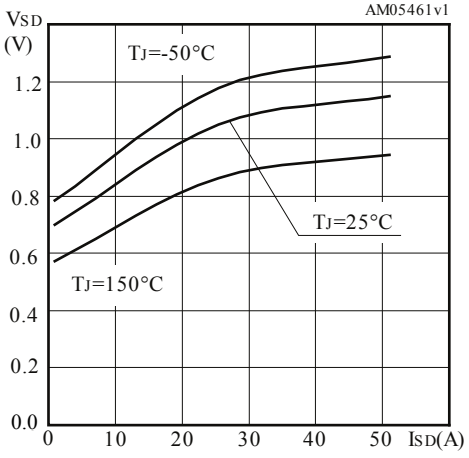


Figure 12. Normalized breakdown voltage vs temperature

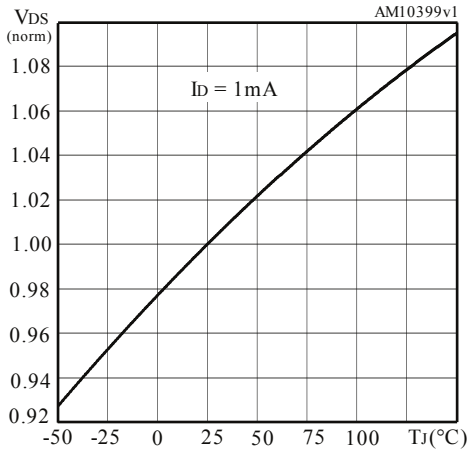
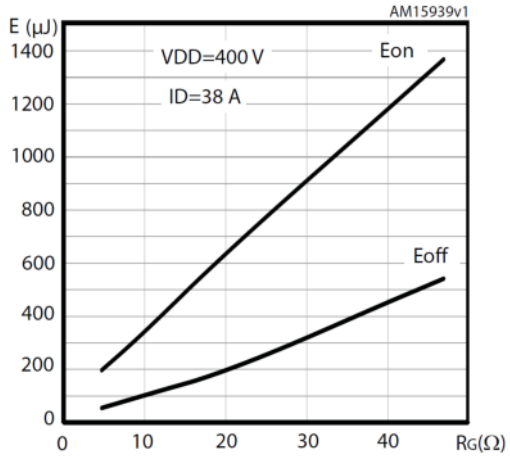


Figure 13. **Typical switching energy vs gate resistance**



Note: *E_{on} including reverse recovery of a SiC diode.*

3 Test circuits

Figure 14. Switching times test circuit for resistive load

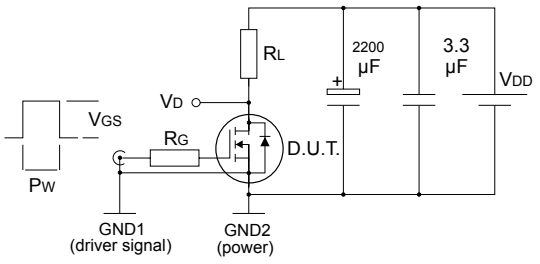


Figure 15. Gate charge test circuit

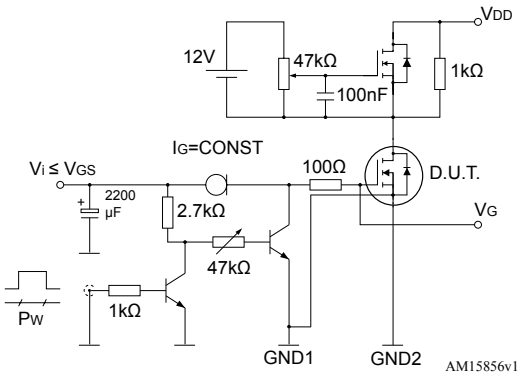


Figure 16. Test circuit for inductive load switching and diode recovery times

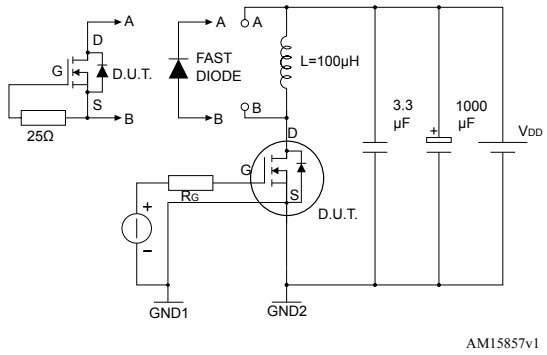


Figure 17. Unclamped inductive load test circuit

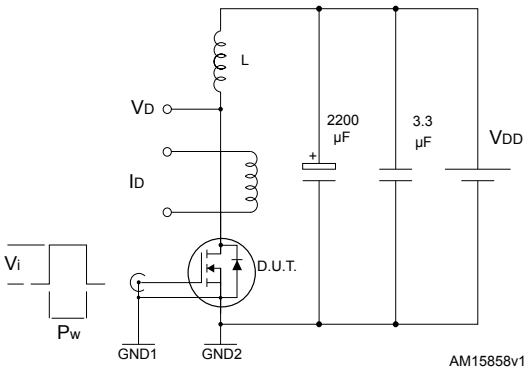


Figure 18. Unclamped inductive waveform

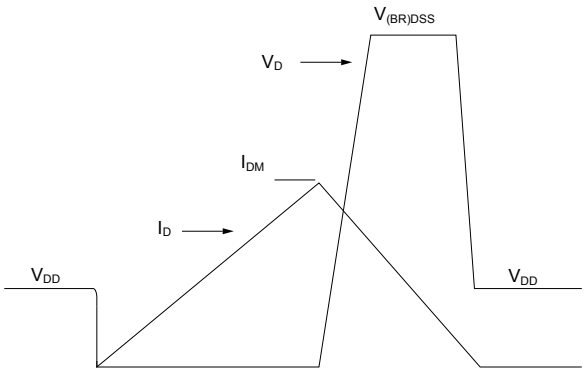
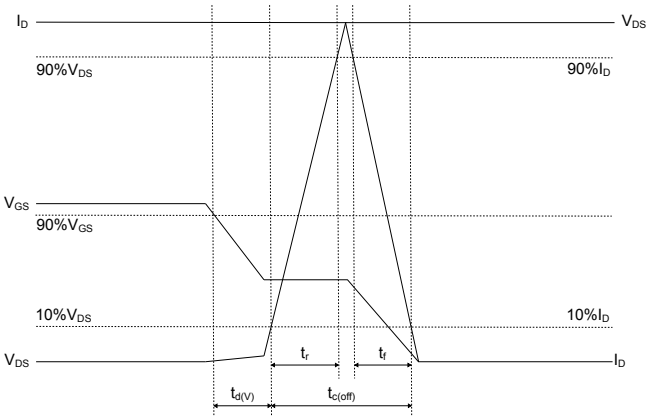


Figure 19. Switching time waveform



4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO247-4 package information

Figure 20. TO247-4 package outline

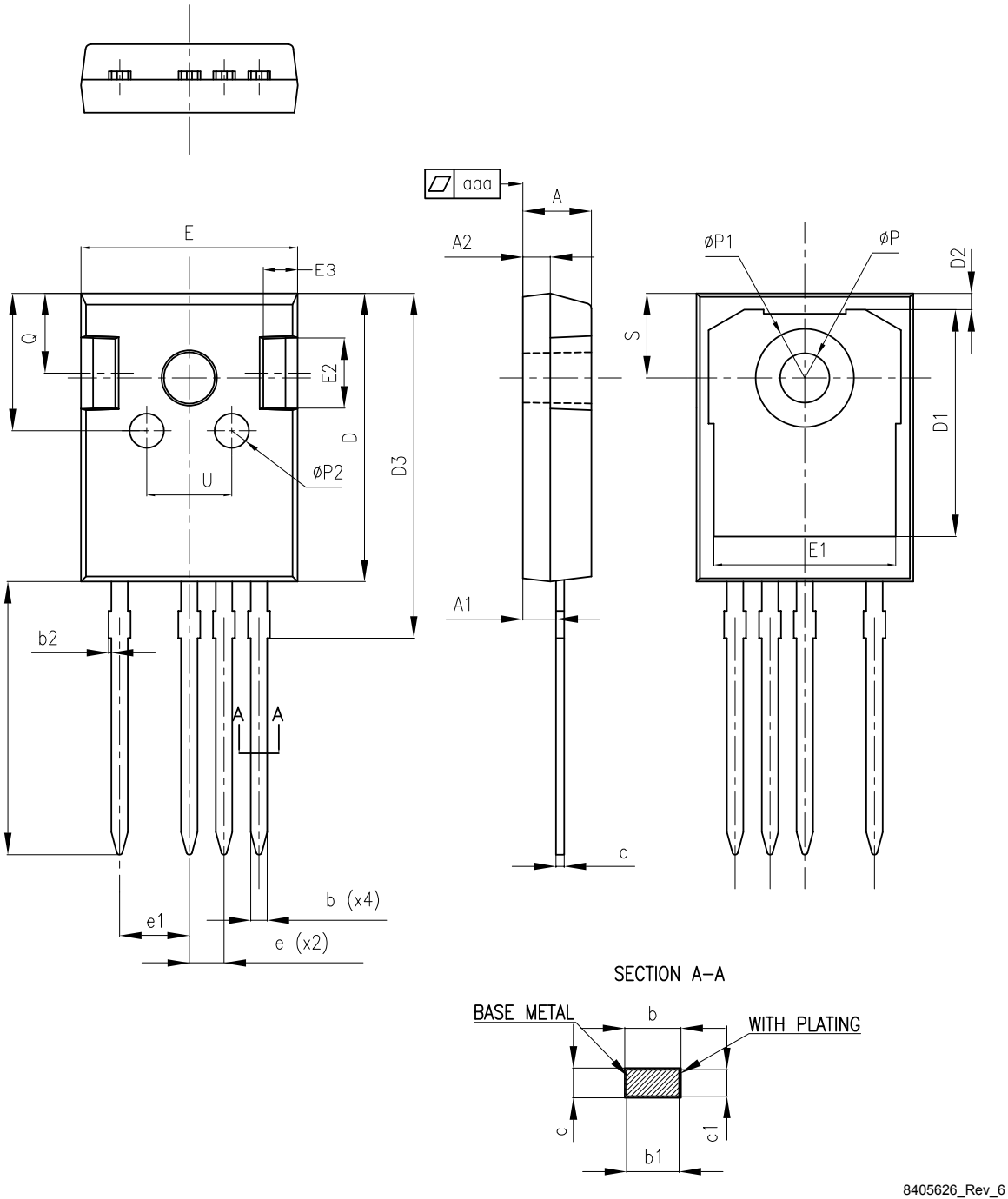


Table 8. **TO247-4 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.29
b1	1.15	1.20	1.25
b2	0.00		0.20
c	0.59		0.66
c1	0.58	0.60	0.62
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.20	1.35
D3	24.97	25.12	25.27
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	2.44	2.54	2.64
e1	4.98	5.08	5.18
L	19.80	19.92	20.10
P	3.50	3.60	3.70
P1			7.40
P2	2.40	2.50	2.60
Q	5.60		6.00
S		6.15	
T	9.80		10.20
U	6.00		6.40
aaa		0.04	0.10

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
28-Jun-2013	1	Initial release.
17-Jan-2014	2	Document status promoted from preliminary to production data.
04-Feb-2026	3	Updated Section 4.1: TO247-4 package information. Minor text changes.

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