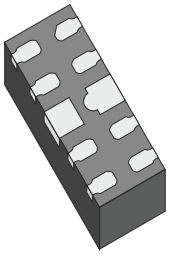
HSP051-4M10

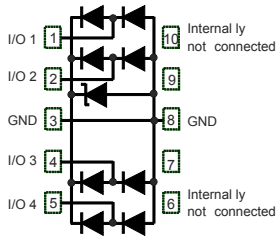
Datasheet

4-line ESD protection for high speed lines



µQFN-10L package

Functional schematic (top view)



Product status
HSP051-4M10

Features

- Flow-through routing to keep signal integrity
- Ultralarge bandwidth: 10 GHz
- Ultralow capacitance:
  - 0.2 pF (I/O to I/O)
  - 0.35 pF (I/O to GND)
- Very Low dynamic resistance: 0.48 Ω
- 100 Ω differential impedance
- Low leakage current: 100 nA at 25 °C
- Extended operating junction temperature range: -40 °C to 150 °C
- Thin package: 0.5 mm max.
- RoHS compliant
- High ESD protection level
- High integration
- Suitable for high density boards
- Complies with following standards:
  - MIL-STD 883G Method 3015-7 Class 3B: – 8 kV
  - IEC 61000-4-2 level 4: 8 kV (contact discharge), 15 kV (air discharge)

Applications

The HSP051-4M10 is designed to protect against

electrostatic discharge on sub micron technology

circuits driving:

- HDMI 2.0 and 1.4
- USB 3.1 and USB3.0
- Digital Video Interface
- Display Port
- Serial ATA

Description

The HSP051-4M10 is a 4-channel ESD array with a rail to rail architecture designed specifically for the protection of high speed differential lines.

The ultralow variation of the capacitance ensures very low influence on signal-skew. The large bandwidth make it compatible with HDMI2.0.4k/2k (=5.94 Gbps) and USB3.1 (= 10 Gbps).

The device is packaged in µQFN 2.5 mm x 1 mm with a 500 µm pitch.

1 Characteristics

Table 1. Absolute maximum ratings T_{amb} = 25 °C

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 contact discharge	8	kV
		IEC 61000-4-2 air discharge	25	
T_j	Operating junction temperature range		-40 to +150	°C
T_{stg}	Storage temperature range		-65 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

Table 2. Electrical characteristics T_{amb} = 25 °C

Symbol	Parameter		Value			Unit
			Min.	Typ.	Max.	
V_{BR}	I_R = 1 mA		4.5	5.8		V
I_{RM}	V_{RM} = 3.6 V			10	100	nA
V_{CL}	I_{PP} = 1 A, 8/20 µs				10	V
V_{CL}	IEC 61000-4-2, +8 kV contact (I_{PP} = 16 A), measured at 30 ns			13		V
R_d	Dynamic resistance, pulse duration 100 ns	I/O to GND		0.48		Ω
		GND to I/O		0.96		Ω
CI/O - I/O	VI/O = 0 V, F = 200 MHz to 9 GHz			0.2	0.3	pF
CI/O - GND	VI/O = 0 V	F = 200 MHz to 2.5 GHz		0.4	0.55	pF
		F = 2.5 GHz to 9 GHz		0.35	0.45	pF
f_C	-3dB			10		GHz
Z_{diff}	Time domain reflectometry: t_r = 200 ps (10 - 90%), Z_0 = 100 Ω		85	100	115	Ω

1.1 On-board measurements

Figure 1. Leakage current versus junction temperature (typical values)

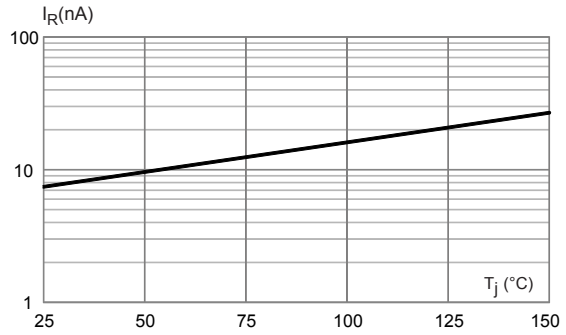


Figure 2. S21 attenuation measurement

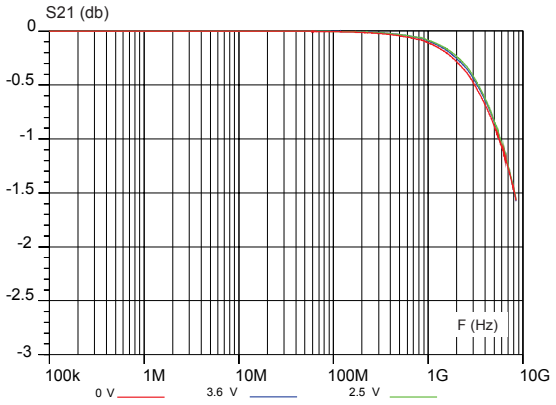


Figure 3. Eye diagram - HDMI mask at 3.35 Gbps per channel(1)(without HSP051-4M10)

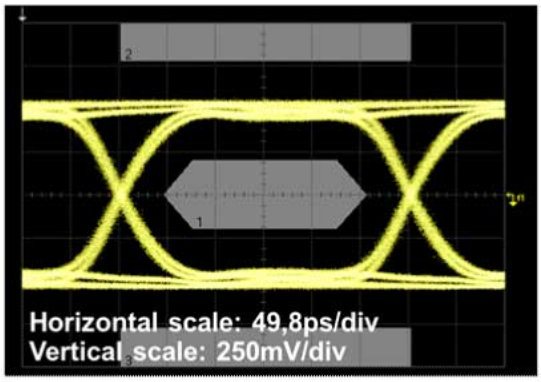


Figure 4. Eye diagram - HDMI mask at 3.35 Gbps per channel(1) (with HSP051-4M10)

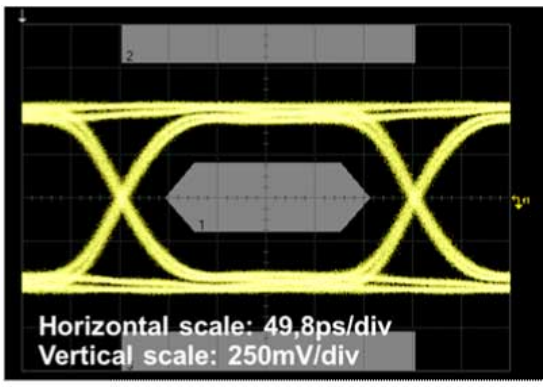


Figure 5. Eye diagram - HDMI 2.0 mask at 5.94 Gbps per channel (without HSP051-4M10)

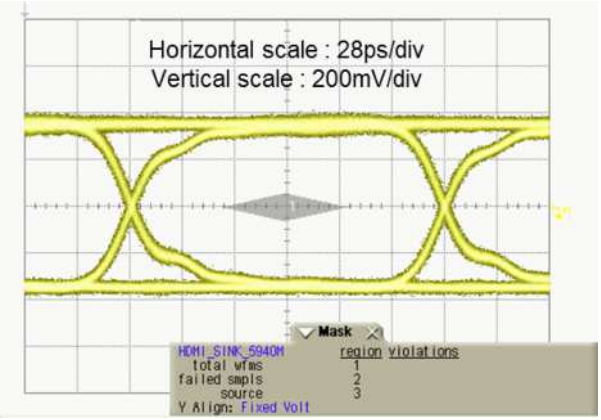


Figure 6. Eye diagram - HDMI 2.0 mask at 5.94 Gbps per channel (with HSP051-4M10)

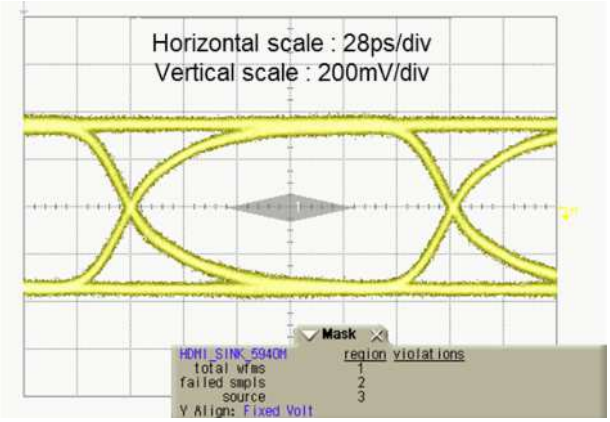


Figure 7. Eye diagram - USB 3.0 mask at 5.0 Gbps per channel (without HSP051-4M10)

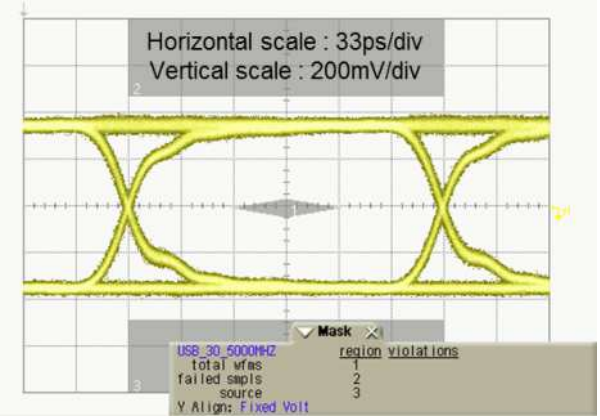


Figure 8. Eye diagram - USB 3.0 mask at 5.0 Gbps per channel (with HSP051-4M10)

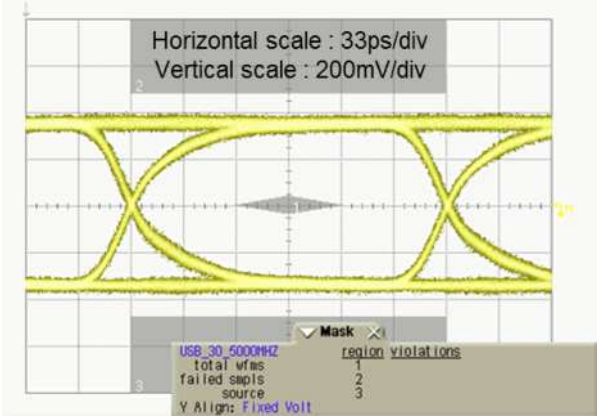


Figure 9. Eye diagram - USB 3.1 mask at 10.0 Gbps per channel (without HSP051-4M10)

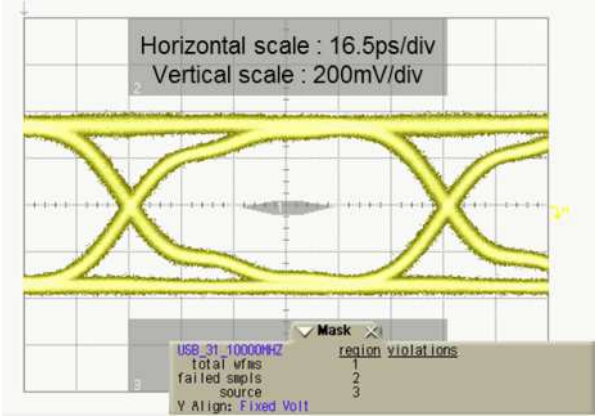


Figure 10. Eye diagram - USB 3.1 mask at 10.0 Gbps per channel (with HSP051-4M10)

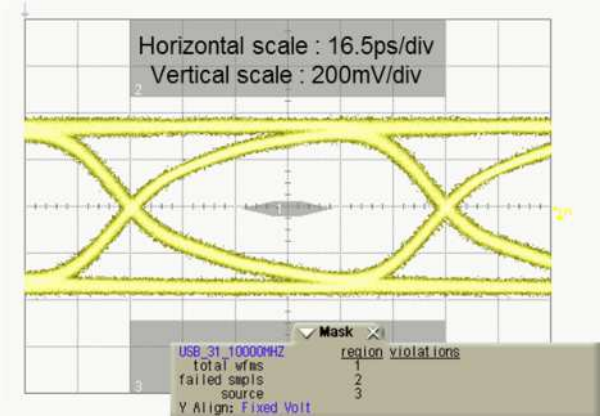


Figure 11. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

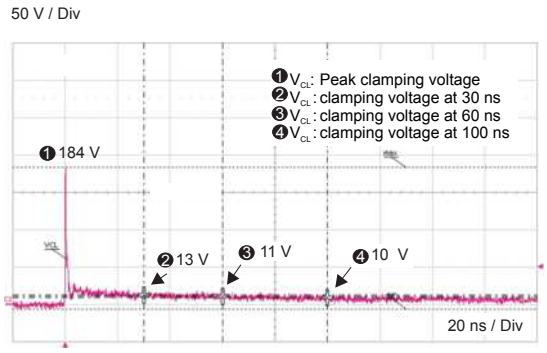


Figure 12. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

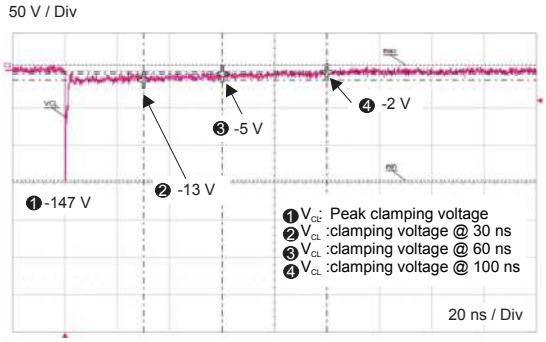


Figure 13. TLP measurement (pulse duration 100 ns)

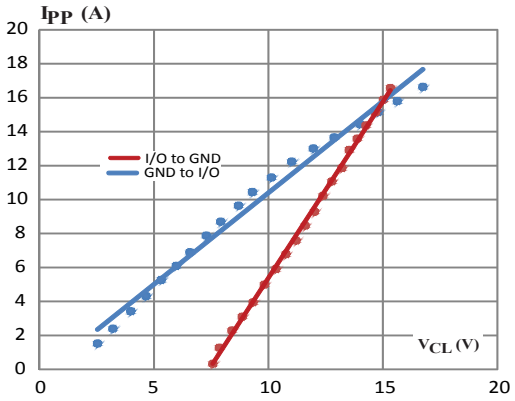


Figure 14. TDR measurement



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 µQFN-10L dimension values

- Epoxy meets UL94, V0
- Lead-free package

Figure 15. µQFN-10L dimension definitions

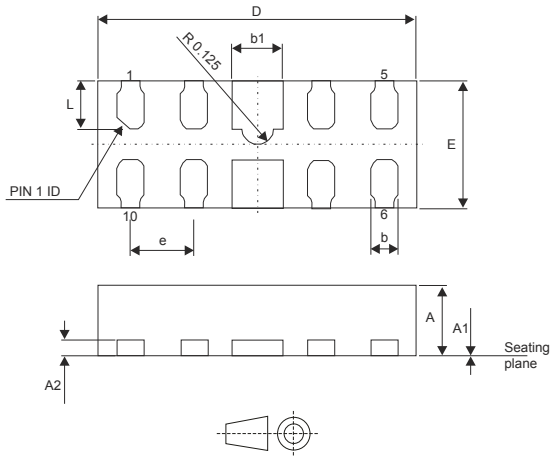


Table 3. µQFN-10L dimension values

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.40	0.47	0.50	0.018	0.018	0.020
A1	0.00	0.00	0.05	0.00	0.000	0.002
A2		0.13			0.005	
b	0.15	0.20	0.25	0.006	0.008	0.009
b1	0.35	0.40	0.45	0.014	0.016	0.041
D	2.40	2.50	2.60	0.094	0.098	0.102
E	0.90	1.00	1.10	0.035	0.039	0.043
e		0.50			0.206	
L	0.33	0.38	0.43	0.012	0.015	0.017
aaa		0.08			0.003	
bbb		0.10			0.004	

Figure 16. Footprint recommendations (dimensions in mm)

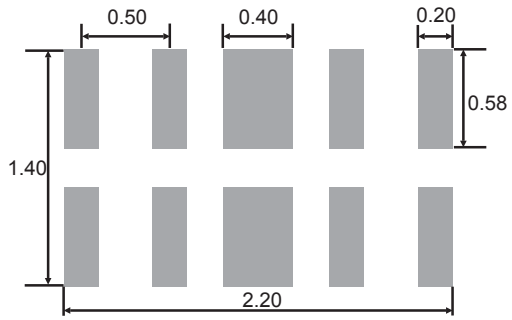
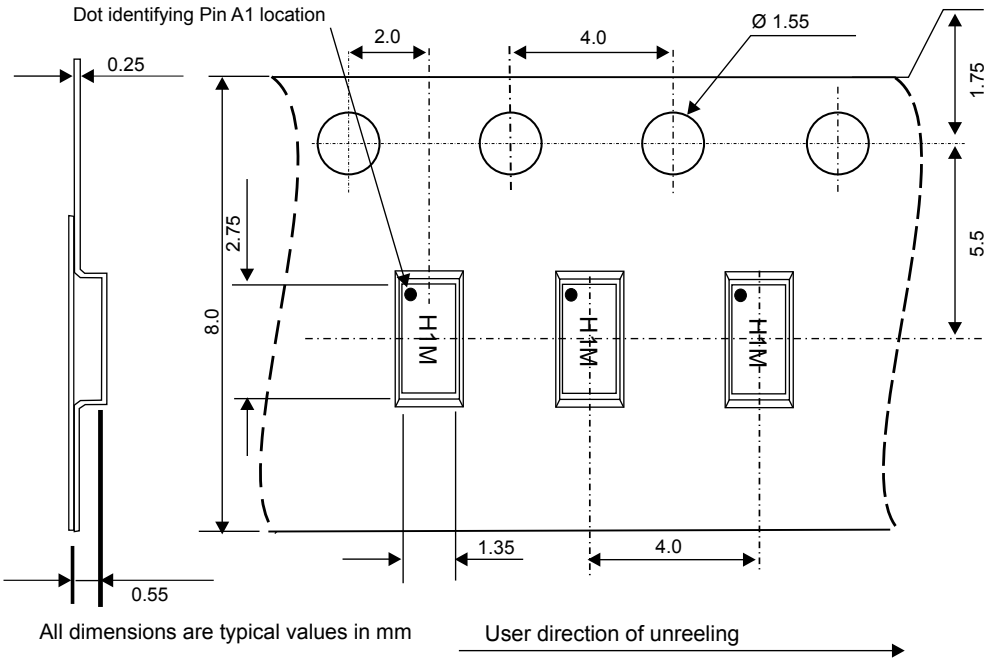


Figure 17. Marking



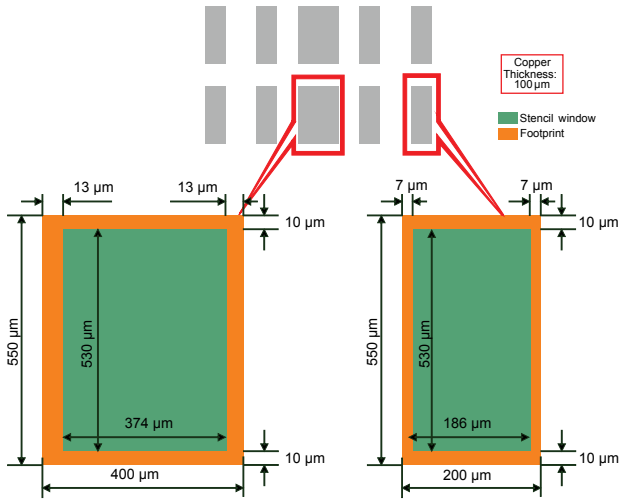
Note: Product marking may be rotated by 180° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 18. µQFN-10L tape and reel specification



3 Recommendation on PCB assembly

Figure 19. **µQFN-10L dimension definitions**



3.1 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

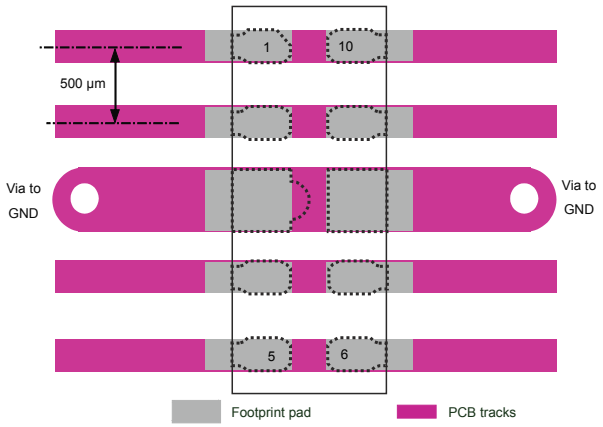
3.2 Placement

1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.3 PCB design preference

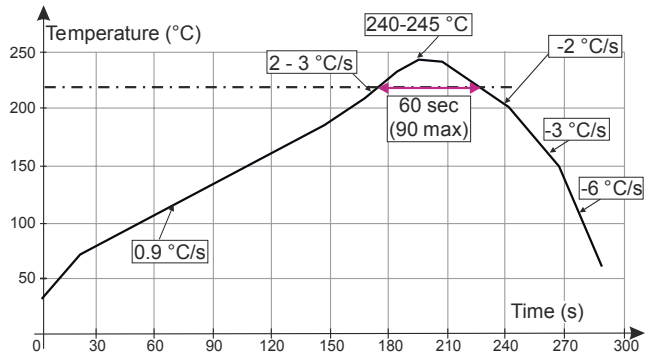
1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

Figure 20. Printed circuit board layout recommendations



3.4 Reflow profile

Figure 21. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

Note: Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Figure 22. **Ordering information scheme**

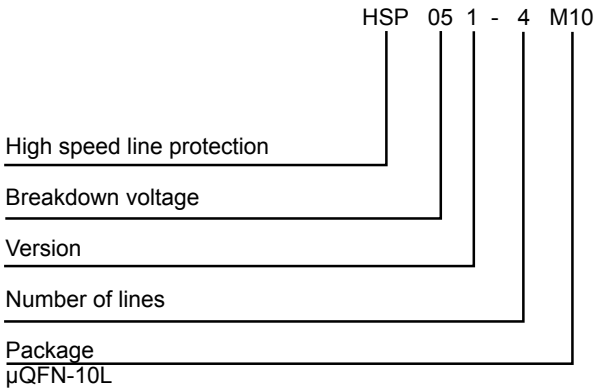


Table 4. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
HSP051-4M10	H1M	µQFN-10L	3.27 mg	3000	Tape and reel

Revision history

Table 5. **Document revision history**

Date	Version	Changes
29-Jul-2013	1	Initial release.
15-Oct-2013	2	Updated status to production data.
17-Jun-2014	3	Updated Figure 19.
14-Nov-2014	4	Updated Features, Applications and Description. Updated Table 1 and Table2. Added Figure 6 to Figure 11.
22-Feb-2018	5	Added a note for Figure 17. Marking.
07-Feb-2019	6	Updated links syntax.

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