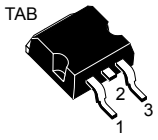
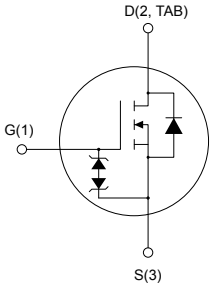
# N-channel 600 V, 0.108 Ω typ., 26 A MDmesh M2 Power MOSFET in a D²PAK package




**D²PAK**




AM01476v1_tab

## Features

| Order code | $V_{DS}$ @ $T_J$ max. | $R_{DS(on)}$ max. | $I_D$ |
|---|---|---|---|
| STB33N60M2 | 650 V | 0.125 Ω | 26 A |

- Extremely low gate charge
- Excellent output capacitance ($C_{oss}$) profile
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications
- LLC converters, resonant converters

## Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

| Product status link |
|---|
| STB33N60M2 |

| Product summary | |
|---|---|
| **Order code** | STB33N60M2 |
| **Marking** | 33N60M2 |
| **Package** | D²PAK |
| **Packing** | Tape and reel |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate-source voltage | ±25 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 26 | A |
| | Drain current (continuous) at $T_C$ = 100 °C | 16 | A |
| $I_{DM}$(1) | Drain current (pulsed) | 104 | A |
| $P_{TOT}$ | Total power dissipation at $T_C$ = 25 °C | 190 | W |
| dv/dt(2) | Peak diode recovery voltage slope | 15 | V/ns |
| dv/dt(3) | MOSFET dv/dt ruggedness | 50 | V/ns |
| $T_{stg}$ | Storage temperature range | -55 to 150 | °C |
| $T_j$ | Operating junction temperature range | | |

1. *Pulse width is limited by safe operating area.*
2. *$I_{SD}$ ≤ 26 A, di/dt ≤ 400 A/µs, $V_{DS(peak)}$ < $V_{(BR)DSS}$, $V_{DD}$ = 400 V.*
3. *$V_{DS}$ ≤ 480 V*

**Table 2. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thJC}$ | Thermal resistance, junction-to-case | 0.66 | °C/W |
| $R_{thJA}$(1) | Thermal resistance, junction-to-ambient | 30 | °C/W |

1. *When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.*

**Table 3. Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$) | 5 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 450 | mJ |

# 2 Electrical characteristics

$T_C$ = 25 °C unless otherwise specified

**Table 4. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V, $I_D$ = 1 mA | 600 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0 V, $V_{DS}$ = 600 V | | | 1 | µA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 600 V, $T_C$ = 125 °C(1) | | | 100 | µA |
| $I_{GSS}$ | Gate-body leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = ±25 V | | | ±10 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 13 A | | 0.108 | 0.125 | Ω |

1. *Specified by design, not tested in production.*

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 100 V, f = 1 MHz, $V_{GS}$ = 0 V | - | 1781 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 85 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 2.5 | - | pF |
| $C_{oss\ eq.}$(1) | Equivalent output capacitance | $V_{DS}$ = 0 to 480 V, $V_{GS}$ = 0 V | - | 135 | - | pF |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz, $I_D$ = 0 A | - | 5.2 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 480 V, $I_D$ = 26 A, $V_{GS}$ = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior) | - | 45.5 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 9.9 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 18.5 | - | nC |

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$.*

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 300 V, $I_D$ = 13 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform) | - | 16 | - | ns |
| $t_r$ | Rise time | | - | 9.6 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 109 | - | ns |
| $t_f$ | Fall time | | - | 9 | - | ns |

**Table 7. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 26 | A |
| $I_{SDM}$(1) | Source-drain current (pulsed) | | - | | 104 | A |
| $V_{SD}$(2) | Forward on voltage | $V_{GS}$ = 0 V, $I_{SD}$ = 26 A | - | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 26 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V (see Figure 16. Test circuit for inductive load switching and diode recovery times) | - | 375 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 5.6 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 30 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 26 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V, $T_j$ = 150 °C (see Figure 16. Test circuit for inductive load switching and diode recovery times) | - | 478 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 7.7 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 32.5 | | A |

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5 %.*

## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

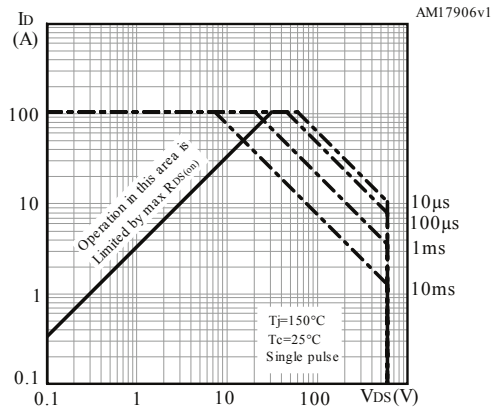



**Figure 2. Normalized thermal impedance**

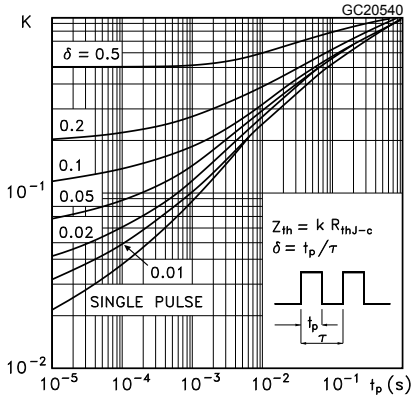



**Figure 3. Output characteristics**

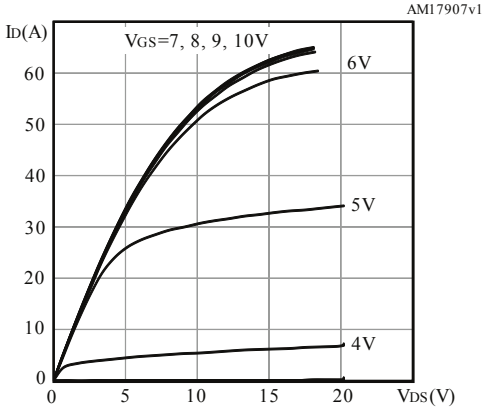



**Figure 4. Transfer characteristics**

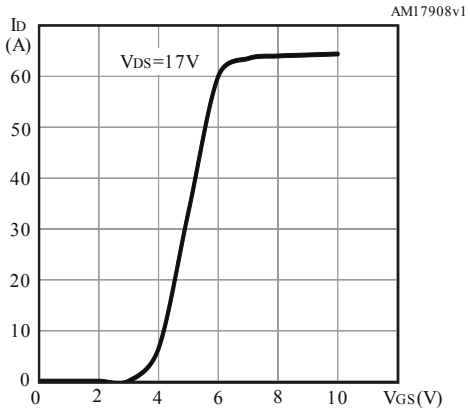



**Figure 5. Gate charge vs gate-source voltage**

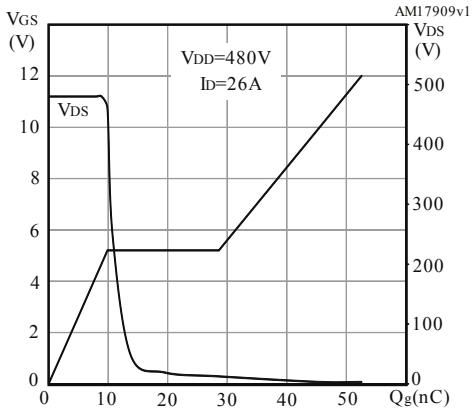



**Figure 6. Static drain-source on-resistance**

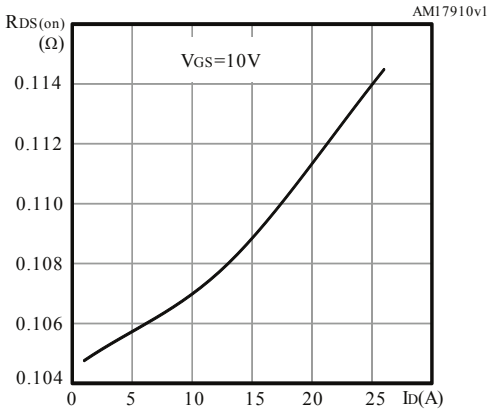


**Figure 7. Capacitance variations**

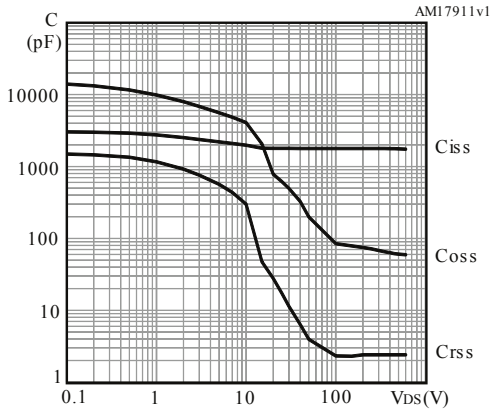



**Figure 8. Output capacitance stored energy**

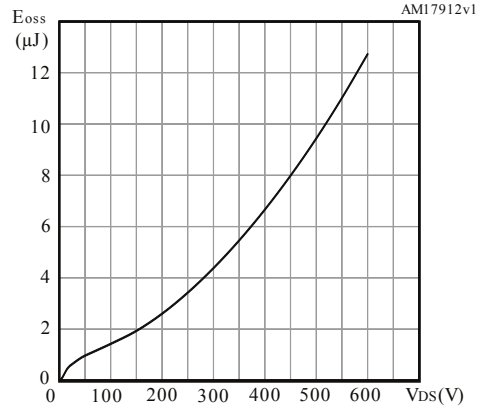



**Figure 9. Normalized gate threshold voltage vs temperature**

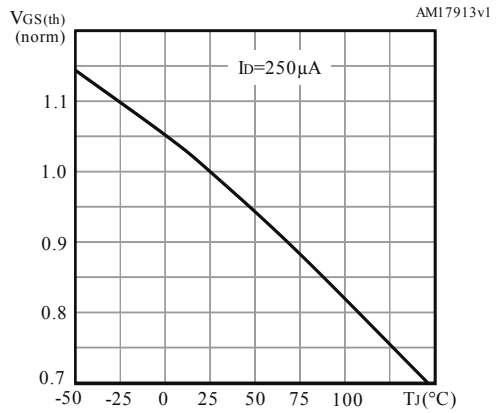



**Figure 10. Normalized on-resistance vs temperature**

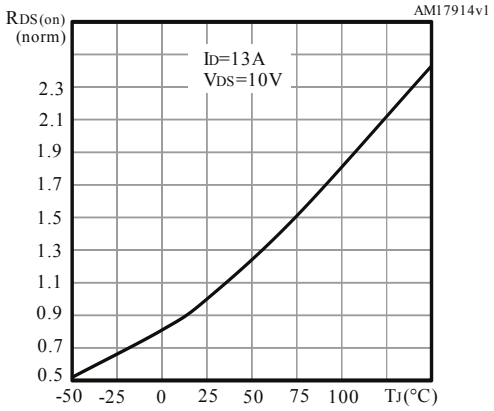



**Figure 11. Normalized $V_{DS}$ vs temperature**

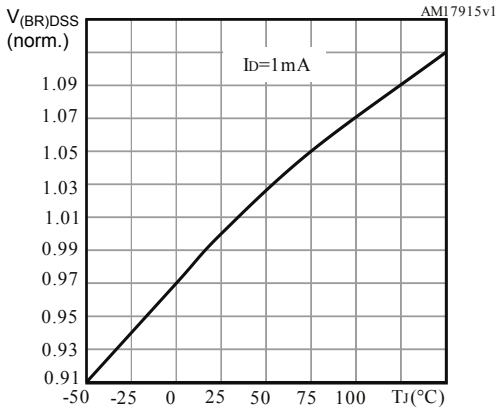



**Figure 12. Source-drain diode forward characteristics**

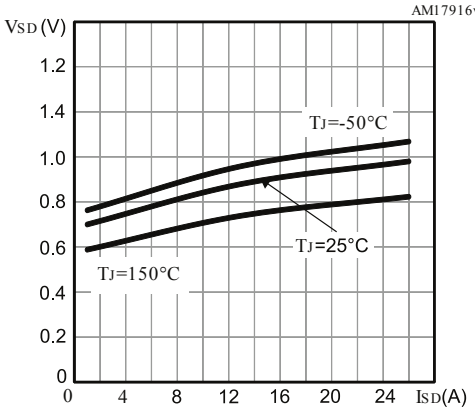
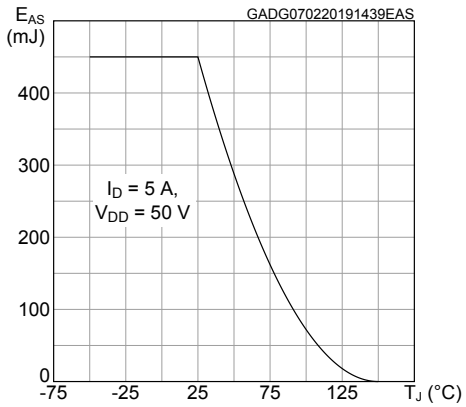
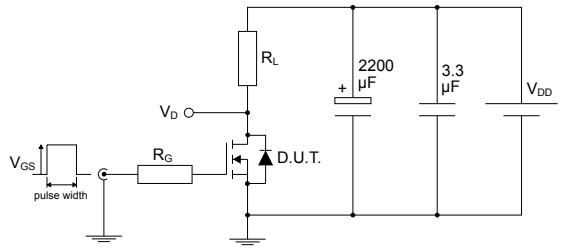


Figure 13. **Maximum avalanche energy vs temperature**



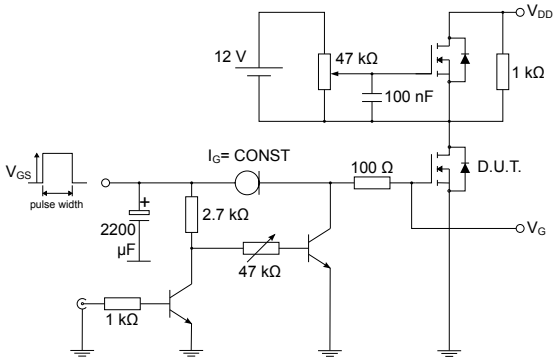
# 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**



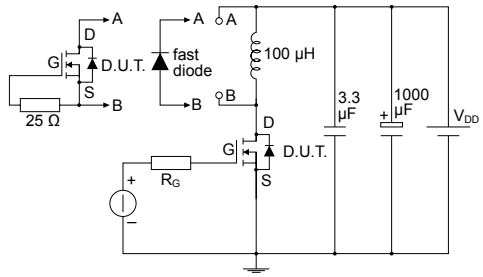

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**Figure 15. Test circuit for gate charge behavior**



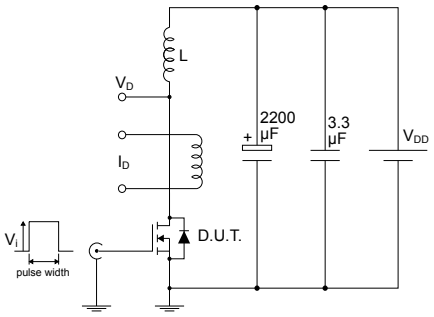

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**Figure 16. Test circuit for inductive load switching and diode recovery times**



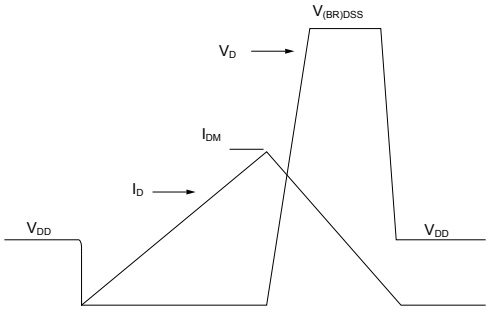

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**Figure 17. Unclamped inductive load test circuit**



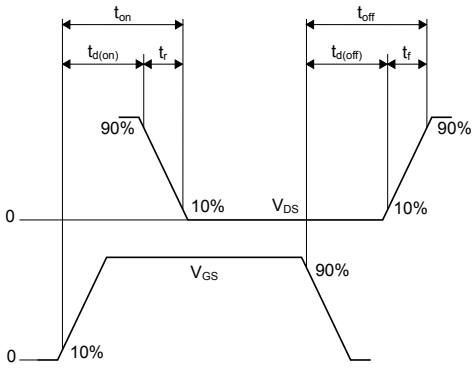

AM01471v1

**Figure 18. Unclamped inductive waveform**




AM01472v1

**Figure 19. Switching time waveform**




AM01473v1

# 4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 4.1 D²PAK (TO-263) type A package information

Figure 20. **D²PAK (TO-263) type A package outline**

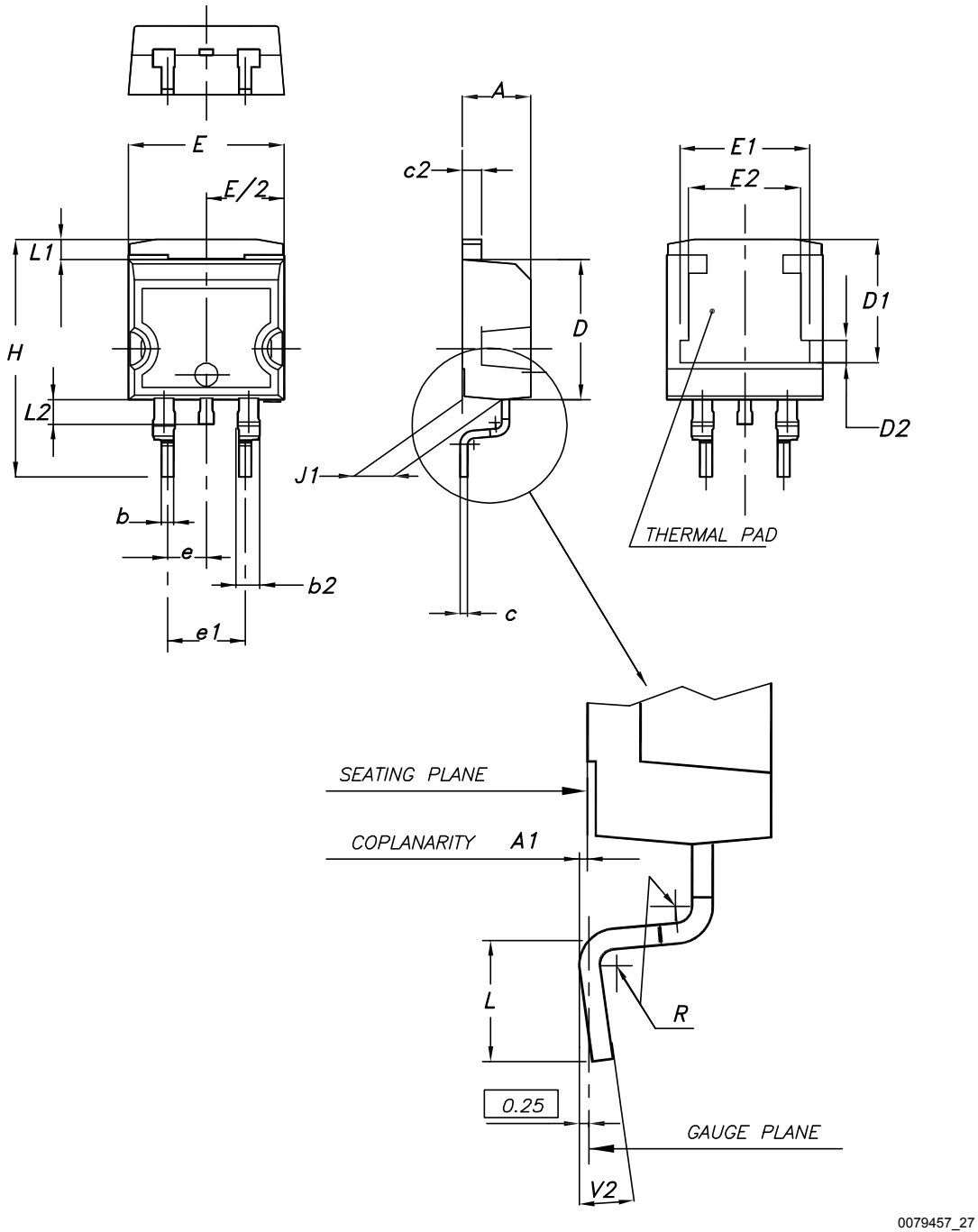
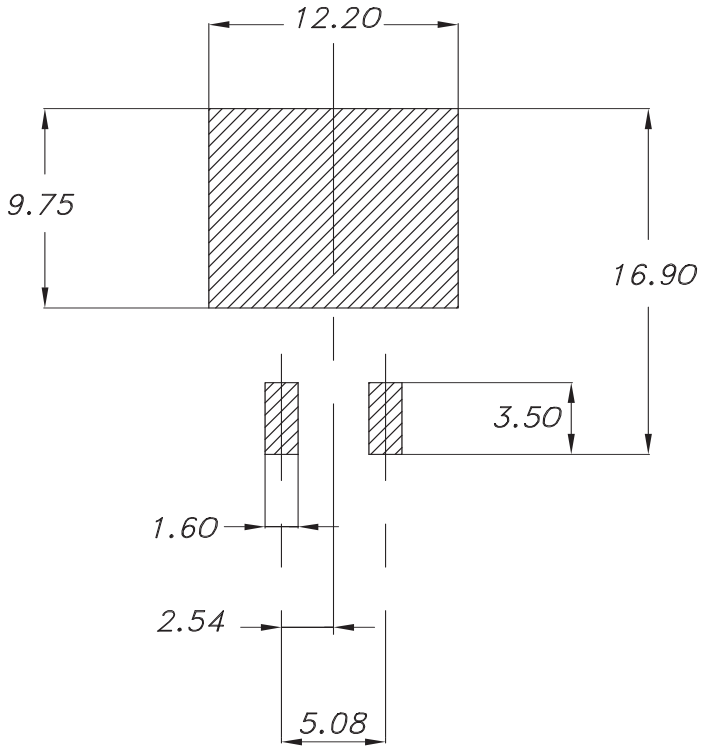


Table 8. D²PAK (TO-263) type A package mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| A1 | 0.03 | | 0.23 |
| b | 0.70 | | 0.93 |
| b2 | 1.14 | | 1.70 |
| c | 0.45 | | 0.60 |
| c2 | 1.23 | | 1.36 |
| D | 8.95 | | 9.35 |
| D1 | 7.50 | 7.75 | 8.00 |
| D2 | 1.10 | 1.30 | 1.50 |
| E | 10.00 | | 10.40 |
| E1 | 8.30 | 8.50 | 8.70 |
| E2 | 6.85 | 7.05 | 7.25 |
| e | | 2.54 | |
| e1 | 4.88 | | 5.28 |
| H | 15.00 | | 15.85 |
| J1 | 2.49 | | 2.69 |
| L | 2.29 | | 2.79 |
| L1 | 1.27 | | 1.40 |
| L2 | 1.30 | | 1.75 |
| R | | 0.40 | |
| V2 | 0° | | 8° |

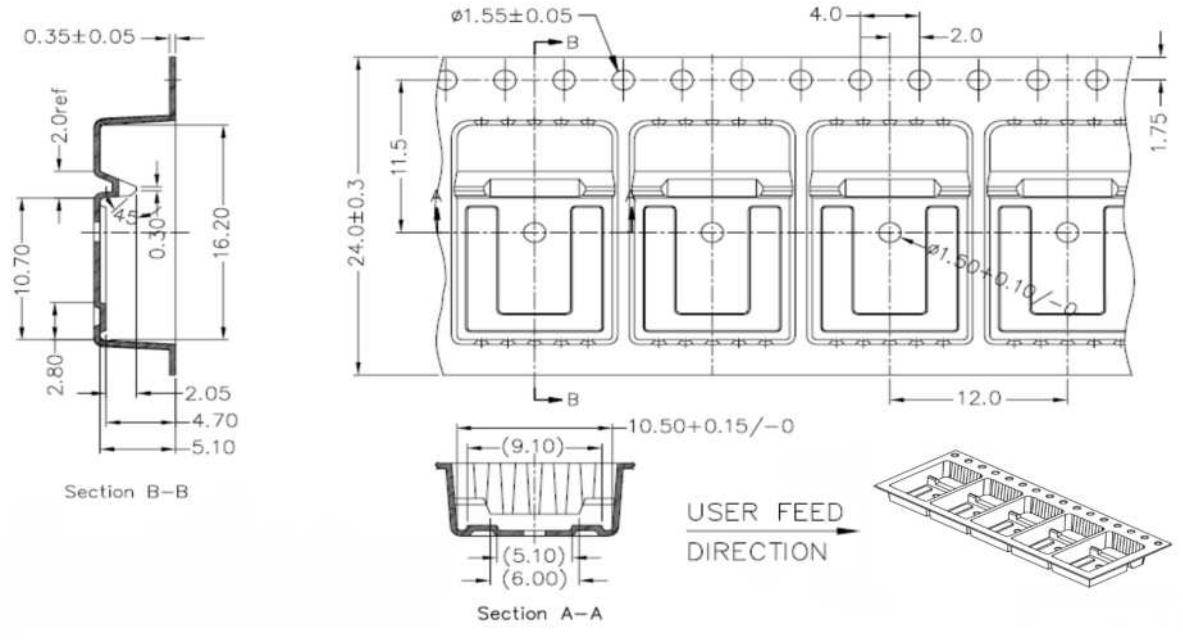
Figure 21. D²PAK (TO-263) recommended footprint (dimensions are in mm)




0079457_Rev27_footprint

## 4.2 D²PAK packing information

Figure 22. D²PAK tape drawing (dimensions are in mm)




DM01095771_2

## Revision history

Table 9. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 13-Sep-2013 | 1 | First release. |
| 19-Nov-2013 | 2 | – Modified: $R_{DS(on)}$ and $I_D$ values in cover page<br>– Modified: values in *Table 4*<br>– Modified: $R_{DS(on)}$ typical and maximum values in *Table 5*, the entire typical values in *Table 6*, *7* and *8*<br>– Added: *Section 2.1: Electrical characteristics (curves)*<br>– Minor text changes |
| 18-Jun-2019 | 3 | Removed maturity status indication from cover page. The document status is production data.<br>Update *Table 3. Avalanche characteristics.*<br>Added *Figure 13. Maximum avalanche energy vs temperature.*<br>Minor text changes. |
| 01-Aug-2025 | 4 | Update Section 4: Package information.<br>Minor text changes. |

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