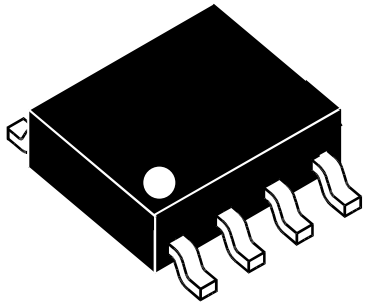
# LCP22

## Protection IC for ringing SLICs

**Datasheet – production data**



SO-8 wide

## Features

- Protection IC recommended for ringing SLICs
- Wide firing voltage range: -120 V to +120 V
- Low gate triggering current: $I_G$ = 5 mA max
- Peak pulse current: $I_{PP}$ = 50 A (10/1000 µs)
- Holding current: $I_H$ = 150 mA min.

## Applications

- Dual battery supply voltage SLICs
- Central office (CO)
- Private branch exchange (PBX)
- Digital loop carrier (DLC)
- Digital subscriber line access multiplexer (DSLAM)
- Fiber in the loop (FITL)
- Wireless local loop (WLL)
- Hybrid fiber coax (HFC)
- ISDN terminal adapter
- Cable modem

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## Description

The LCP22 has been developed to protect SLICs operating on both negative and positive battery supplies, as well as high voltage SLICs. It provides crowbar mode protection for both TIP and RING lines. The surge suppression is assumed for each wire by two thyristor structures, one dedicated to positive surges the second one for negative surges. Both positive and negative threshold levels are programmable by two gates.

LCP22 can be used to help equipment to meet various standards such as UL1950, IEC 60950 / CSAC22.2, UL1459 and TIA-968-A. LCP22 pinout and clearance is compatible with UL60950. A Trisil ™ meets UL94 V0.

The LCP22 associated with Epcos PTC model B59173C1130A151 is compliant with ITU TK20/K21 (4 kV lightning and AC power fault tests).

**Figure 1. Functional diagram**

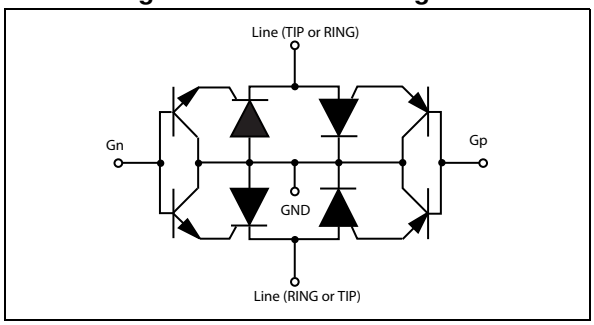
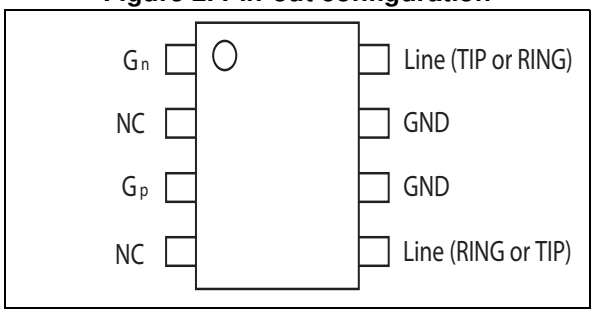



**Figure 2. Pin-out configuration**






This is information on a product in full production. www.st.com

# 1 Characteristics

**Table 1. Compliant with the following standards**

| Standard | Peak surge voltage (V) | Voltage waveform | Required peak current (A) | Current waveform | Minimum series resistor Rs to meet standard ( Ω ) |
|---|---|---|---|---|---|
| **GR-1089 Core First level** | 2500<br>1000 | 2/10 µs<br>10/1000 µs | 500<br>100 | 2/10 µs<br>10/1000 µs | 12<br>10 |
| **GR-1089 Core Second level** | 5000 | 2/10 µs | 500 | 2/10 µs | 24 |
| **GR-1089 Core Intra-building** | 1500 | 2/10 µs | 100 | 2/10 µs | 0 |
| **ITU-T-K20/K21** | 6000<br>4000<br>1500 | 10/700 µs | 150<br>100<br>37.5 | 5/310 µs | 35<br>10<br>0 |
| **ITU-T-K20 (IEC61000-4-2)** | 8000<br>15000 | 1/60 ns | ESD contact discharge<br>ESD air discharge | | 0<br>0 |
| **IEC61000-4-5** | 4000<br>4000 | 10/700 µs<br>1.2/50 µs | 100<br>100 | 5/310 µs<br>8/20 µs | 14<br>0 |
| **TIA-968-A (formerly FCC part 68) type A** | 1500<br>800 | 10/160 µs<br>10/560 µs | 200<br>100 | 10/160 µs<br>10/560 µs | 20<br>15 |
| **TIA-968-A (formerly FCC part 68) type B** | 1000 | 9/720 µs | 25 | 5/320 µs | 0 |

**Table 2. Absolute maximum ratings ($T_{amb}$ = 25 °C)**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $I_{PP}$ | Peak pulse current | 10/1000 µs<br>5/310 µs<br>2/10µs | 50<br>80<br>150 | A |
| $I_{TSM}$ | Non repetitive surge peak on-state current (F = 50 Hz)<br>$I_{TSM}$ value specified for each line<br>$I_{TSM}$ value can be applied on both lines at the same time (GND capability is twice the line $I_{TSM}$) | $t_p$ = 0.2 s<br>$t_p$ = 1 s<br>$t_p$ = 15 min. | 11<br>7.5<br>3 | A |
| $V_{Gn}$<br>$V_{Gp}$ | Negative battery voltage range<br>Positive battery voltage range | | -120 to 0<br>0 to +120 | V |
| $T_j$ | Operating junction temperature range | | -55 to +125 | °C |
| $T_{stg}$ | Storage temperature range | | -55 to +150 | °C |
| $T_L$ | Lead solder temperature (10 s duration) | | 260 | °C |

**Figure 3. Pulse waveform**

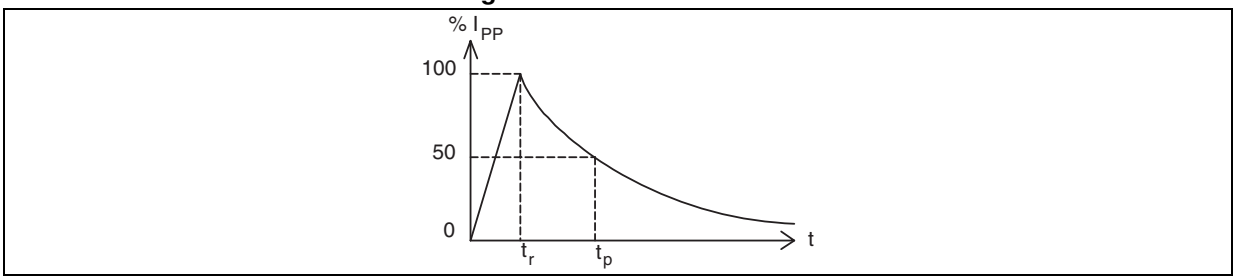



**Table 3. Thermal resistance**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{th(j-a)}$ | Junction to ambient | 150 | °C/W |

**Table 4. Parameters related to the negative suppressor**

| Symbol | Parameter | Test conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{Gn}$ | Negative gate trigger current | $V_{Gn/GND}$ = -60 V<br>Measured at 50 Hz | | 5 | mA |
| $I_{H-}$ | Holding current (see *Figure 4*) | $V_{Gn}$ = -60 V | 150 | | mA |
| $V_{DGL-}$ | Dynamic switching voltage Gn / TIP or RING(1) | $V_{Gn/GND}$ = -60 V<br>10/700 µs 2 kV $R_s$ = 25 Ω $I_{PP}$ = 30 A<br>1.2/50 µs 2 kV $R_s$ = 25 Ω $I_{PP}$ = 30 A | | 8<br>12 | V |
| $V_{GnT}$ | $G_n$ to TIP voltage | $I_{Gn}$ = 20 mA | 0.7 | 1.7 | V |

1. The $V_{DGL}$ value is the difference between the peak line voltage during the surge and the programmed gate voltage.

**Table 5. Parameters related to the positive suppressor**

| Symbol | Parameter | Test conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{Gp}$ | Positive gate trigger current | $V_{Gp/GND}$ = 60 V, measured at 50 Hz | | 5 | mA |
| $V_{DGL+}$ | Dynamic switching voltage Gp / TIP or RING(1) | $V_{Gp/GND}$ = 60 V<br>10/700 µs 2 kV $R_s$ = 25 Ω $I_{PP}$ = 30 A<br>1.2/50 µs 2 kV $R_s$ = 25 Ω $I_{PP}$ = 30 A | | 8<br>20 | V |
| $V_{GpR}$ | $G_P$ to RING voltage | $I_{Gp}$ = -20 mA | 1 | 2 | V |

1. The $V_{DGL}$ value is the difference between the peak line voltage during the surge and the programmed gate voltage.

**Table 6. Parameters related to TIP or RING / GND**

| Symbol | Parameter | Test conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $I_R$ | Reverse leakage current | $V_{TIP\ or\ RING}$ = +120 V $V_{Gp/TIP\ or\ RING}$= +1 V<br>$V_{TIP\ or\ RING}$ = -120 V $V_{Gn/TIP\ or\ RING}$= -1 V | | 5<br>5 | µA |
| C | Capacitance TIP or RING / GND | $V_R$ = -3 V, F =1 MHz, $V_{Gp}$ = 60 V, $V_{Gn}$ = -60 V | | 60 | pF |

**Table 7. Recommended gate capacitance**

| Symbol | Component | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_n$, $C_p$ | Gate decoupling capacitance | 100 | 220 | | nF |

**Figure 4. Relative variation of holding current versus junction temperature**

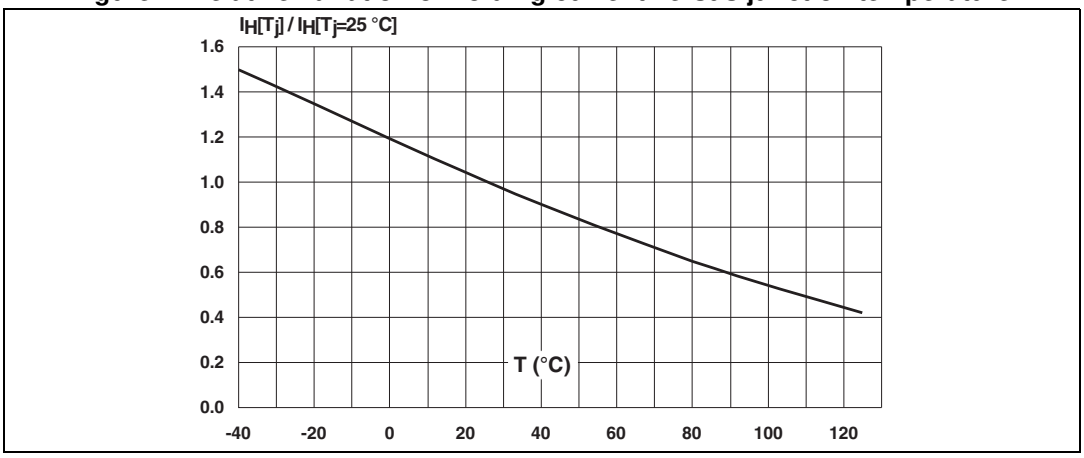



**Figure 5. Maximum non repetitive surge peak on state current versus overload duration**

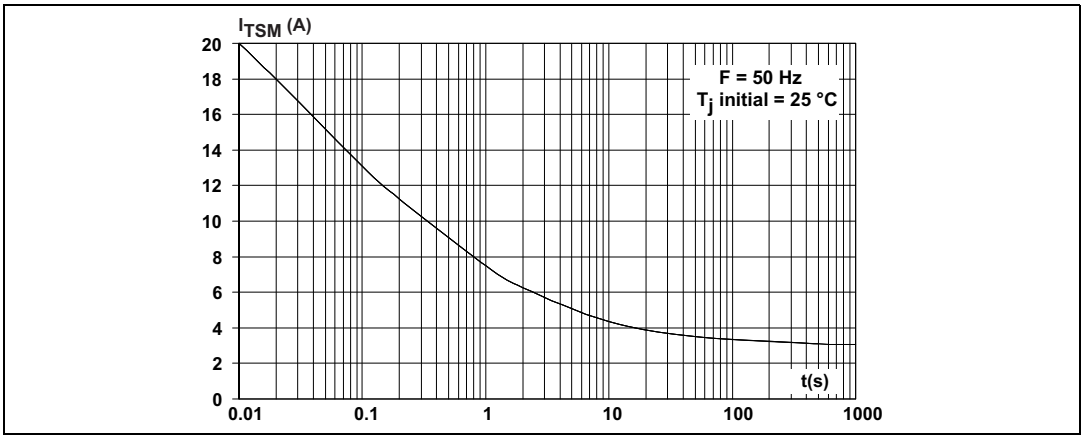
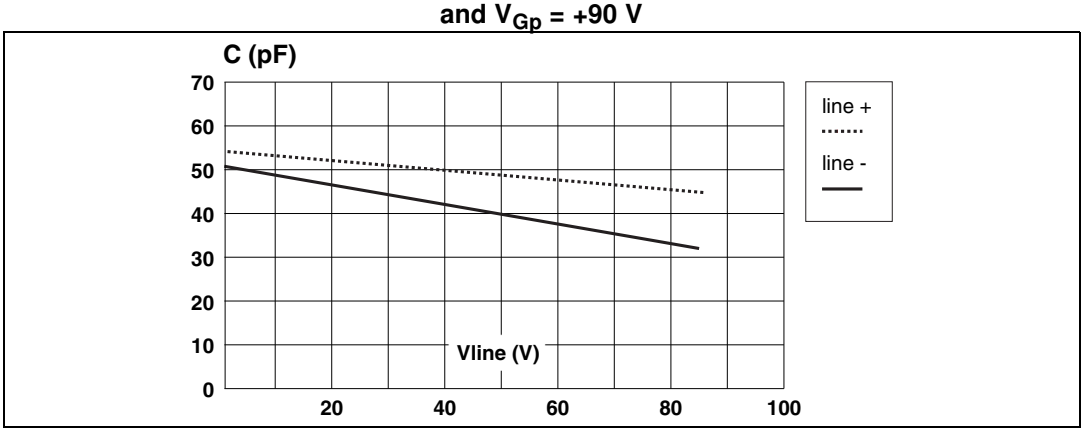



**Figure 6. Capacitance versus reverse applied voltage (typical values) with $V_{Gn}$ = -90 V and $V_{Gp}$ = +90 V**



# 2 Technical information

**Figure 7. LCP22 concept behavior**

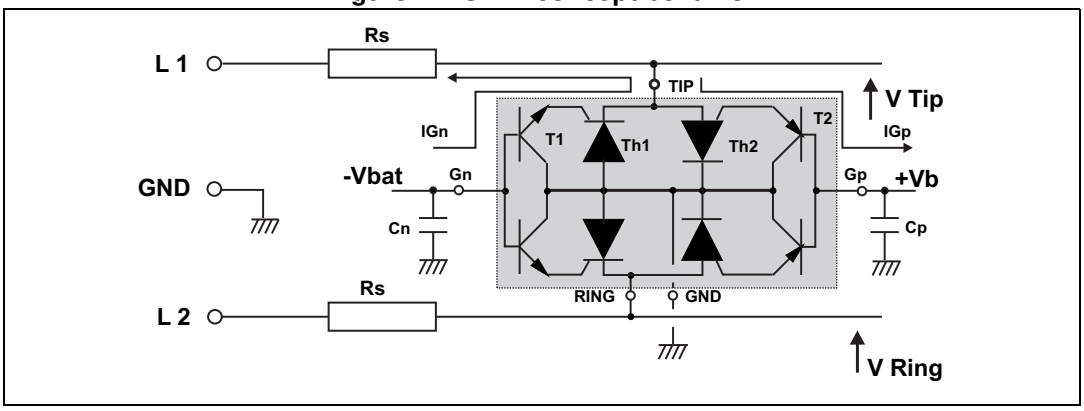



*Figure 7* shows the classical protection circuit using the LCP22 crowbar concept. This topology has been developed to protect two-battery voltage SLICs. It allows both positive and negative firing thresholds to be programmed. The LCP22 has two gates (Gn and Gp). Gn is biased to negative battery voltage -Vbat, while Gp is biased to the positive battery voltage +Vb.

When a negative surge occurs on one wire (L1 for example), a current IGn flows through the base of the transistor T1 and then injects a current in the gate of the thyristor Th1 which turns-on. All the surge current flows through the ground. After the surge, when the current flowing through Th1 becomes less negative than the negative holding current $I_{H-}$, Th1 switches off. This holding current $I_{H-}$ is temperature dependent as per *Figure 4*

When a positive surge occurs on one wire (L1 for example), a current IGp flows through the base of the transistor T2 and then injects a current in the gate of the thyristor Th2 which fires. All the surge current flows through the ground. After the surge, when the current flowing through Th2 becomes less positive than the positive holding current $I_{H+}$, Th2 switches off. This holding current $I_{H+}$, typically 20 mA at 25 °C, is temperature dependent and the same *Figure 4* also applies.

The capacitors Cn and Cp are used to speed up the crowbar structure firing during the fast rise or fall edges. This allows minimization of the dynamic breakover voltage at the SLIC TIP and RING inputs during fast surges. Please note that these capacitors are generally available around the SLIC. To be efficient they have to be as close as possible to the LCP22 gate pins (Gn and Gp) and to the reference ground track (or plan). The optimized value for Cn and Cp is 220 nF.

The series resistors Rs shown in *Figure 7* represent the fuse resistors or the PTCs which are needed to withstand the power contact or the power induction tests imposed by the country standards. Taking this factor into account, the actual lightning surge current flowing through the LCP22 is equal to:

I surge = Vsurge / (Rg + Rs)

With

V surge = peak surge voltage imposed by the standard.

Rg = series resistor of the surge generator

Rs = series resistor of the line card (e.g. PTC)

For a line card with 50 Ω of series resistors which has to be qualified under GR-1089 1000 V 10/1000 µs surge, the present current through the LCP22 is equal to:

I surge = 1000 / (10 + 50) = **17 A**

The LCP22 topology is particularly optimized for the new telecom applications such as fiber in the loop, WLL systems, and decentralized central office, for example.

**Figure 8. Protection of SLIC with positive and negative battery voltages**

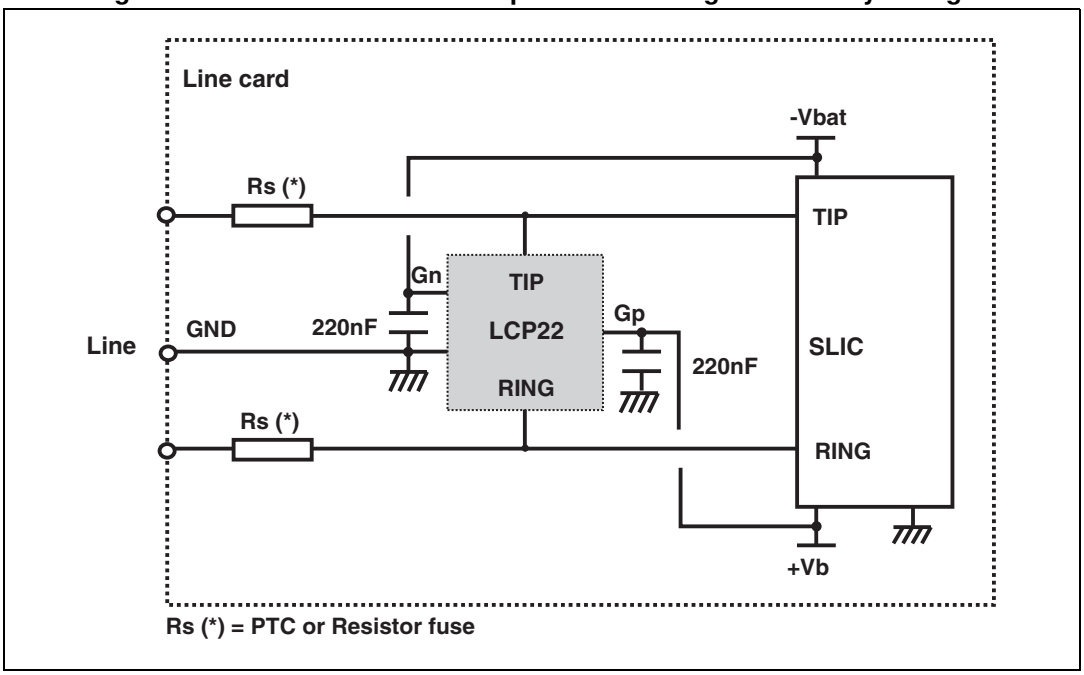



*Figure 8* shows the classical protection topology for SLIC using both positive and negative battery voltages. With such a topology the SLIC is protected against surge over +Vb and lower than -Vbat. In this case, +Vb can be programmed up to +120 V while -Vbat can be programmed down to -120 V.

# 3 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

**Figure 9. SO-8 wide dimension definitions**

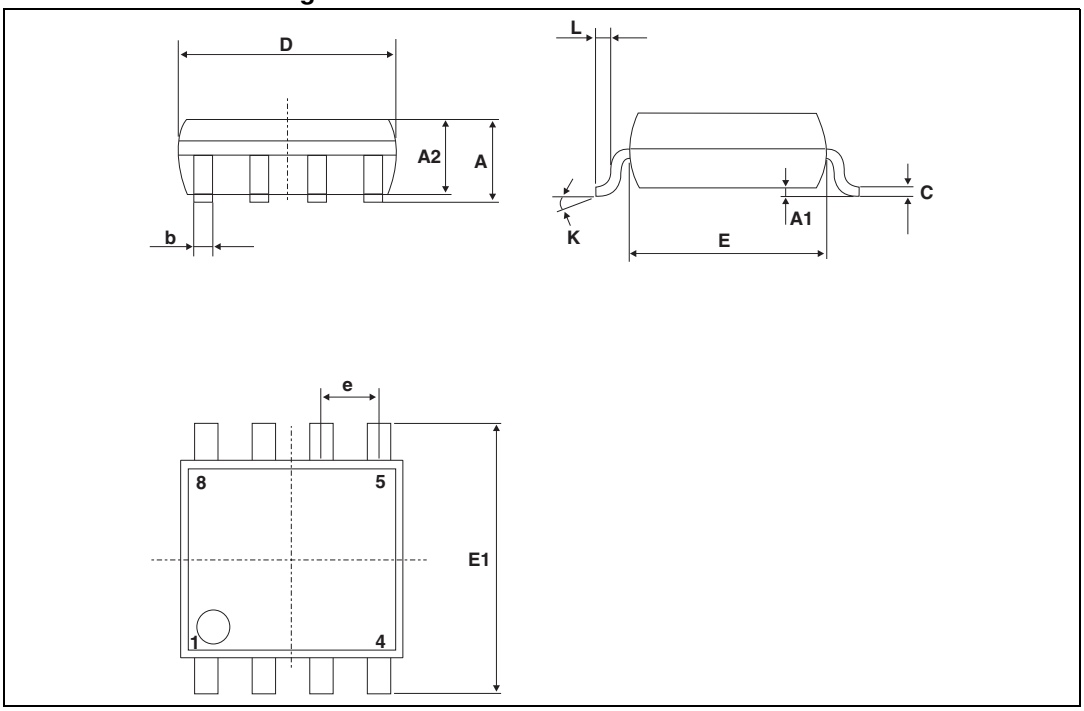


Table 8. SO-8 wide dimension values

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | | Max. | Min. | | Max. |
| A | 1.70 | 1.90 | 2.10 | 0.07 | 0.07 | 0.08 |
| A1 | 0.05 | 0.10 | 0.25 | 0.00 | 0.00 | 0.01 |
| A2 | 1.65 | 1.80 | 1.75 | 0.06 | 0.07 | 0.07 |
| b | 0.38 | 0.43 | 0.48 | 0.01 | 0.02 | 0.02 |
| c | 0.15 | 0.20 | 0.25 | 0.01 | 0.01 | 0.01 |
| D | 5.14 | 5.24 | 5.34 | 0.02 | 0.021 | 0.21 |
| E | 5.20 | 5.30 | 5.40 | 0.02 | 0.021 | 0.21 |
| E1 | 7.70 | 7.80 | 8.25 | 0.30 | 0.031 | 0.32 |
| e | | 1.27 | | 0.05 | 0.05 | |
| K | | | 8.00 | 0.14 | 0.31 | |
| L | 0.55 | 0.75 | 0.85 | 0.02 | 0.03 | 0.03 |

Figure 10. SO-8 wide footprint in mm (inches)

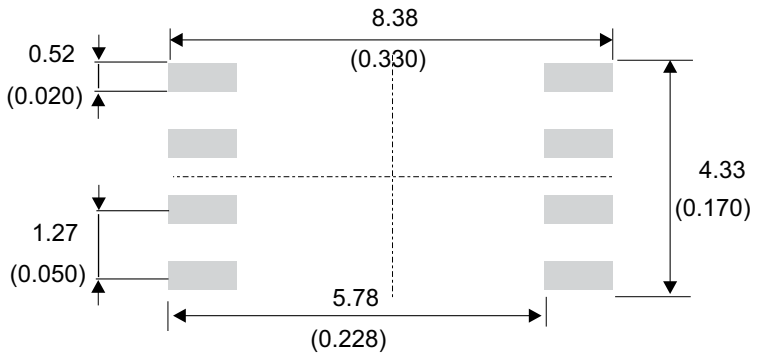
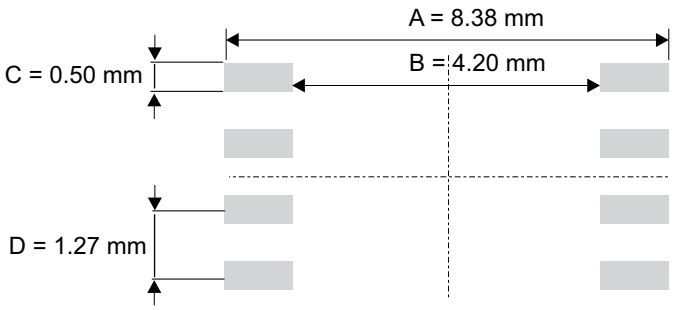



Figure 11. Recommended footprint for SO-8/SO-8 wide compatibility



# 4 Ordering information

**Table 9. Ordering information**

| Order code | Marking | Package | Weight | Base qty | Delivery mode |
|---|---|---|---|---|---|
| LCP22-150B1RL | LCP22 | SO-8 wide | 0.125g | 1500 | Tape and reel |

# 5 Revision history

**Table 10. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 07-Feb-2014 | 1 | Initial release. |
| 03-Jun-2014 | 2 | Updated *Figure 1: Functional diagram*, *Figure 2: Pin-out configuration* and $T_j$ value in *Table 2: Absolute maximum ratings ($T_{amb}$ = 25 °C)*. |
| 22-Oct-2014 | 3 | Added *Figure 11*. |

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