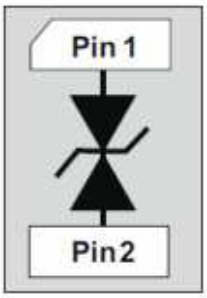
ESDALC5-1BT2Y

Datasheet

Automotive single line low capacitance Transil, transient surge voltage suppressor (TVS) for ESD protection in SOD882T



SOD882T(0402)
(QFN-2L 1.0 x 0.6 x 0.35)



Product status link
ESDALC5-1BT2Y

Features

- AEC-Q101 qualified
- Single-line bidirectional protection
- Breakdown voltage = 5.8 V min.
- Low capacitance = 26 pF at 0 V
- Lead-free packages
- ECOPACK2 compliant component
- Benefits
  - Low capacitance for optimized data integrity
  - Low leakage current < 60 nA
  - Low PCB space consumption: 0.6 mm²
  - High reliability offered by monolithic integration
- Complies with IEC 61000-4-2 (exceeds level 4)
  - ±30 kV (air discharge)
  - ±30 kV (contact discharge)
- Complies with ISO 10605 - C = 330 pF, R = 330 Ω
  - ±30 kV (air discharge)
  - ±30 kV (contact discharge)
- Complies with ISO 7637-3:
  - pulse 3a: V_s = -150 V
  - pulse 3b: V_s = +100 V

Application

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Automotive applications
- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment

Description

The ESDALC5-1BT2Y is bidirectional single-line TVS diode designed to protect data lines or other I/O ports against ESD transients.

This device is ideal for applications where both printed circuit board space and power absorption capability are required.

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 / ISO10605 (C = 330 pF, R = 330 Ω):	30	kV
		MIL STD 883G - Method 3015-7: class 3	25	
P_{PP}	Peak pulse power dissipation (8/20 µs), T_j initial = Tamb		150	W
I_{PP}	Peak Pulse current (8/20 µs)		9	A
T_{OP}	Operating junction temperature range		-50 to +125	°C
T_{stg}	Storage temperature range		-65 to +125	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

Figure 1. Electrical characteristics (definitions)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
V_H	Holding voltage
I_{RM}	Leakage current at V_{RM}
I_{PP}	Peak pulse current
V_{Trig}	Triggering voltage
C_{line}	Input capacitance per line
R_D	Dynamic resistance

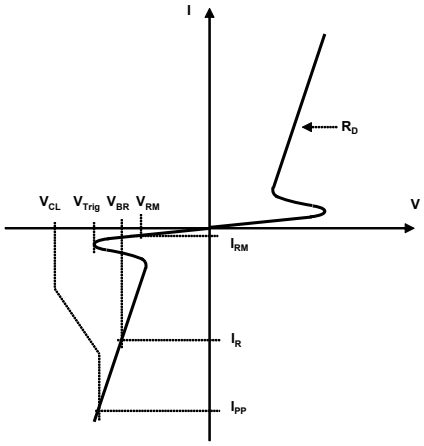


Table 2. Electrical characteristics (values) (T_{amb} = 25° C)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	From I/O1 to I/O2, I_R = 1 mA	11	13	17	V
	From I/O2 to I/O1, IR = 1 mA	5.8	8	11	
I_{RM}	V_R = 5 V			60	nA
R_d	Dynamic resistance, pulse width 100 ns From I/O1 to I/O2 From I/O2 to I/O1		 0.25 0.23		Ω
V_{CL}	8 kV contact discharge after 30 ns IEC 61000 4-2: From I/O1 to I/O2 From I/O2 to I/O1		 17.5 12.5		V
C_{LINE}	F = 1 MHz, VR = 0 V		26	30	pF

1.1 Characteristics (curves)

Figure 2. Peak pulse power versus initial junction temperature (maximum values)

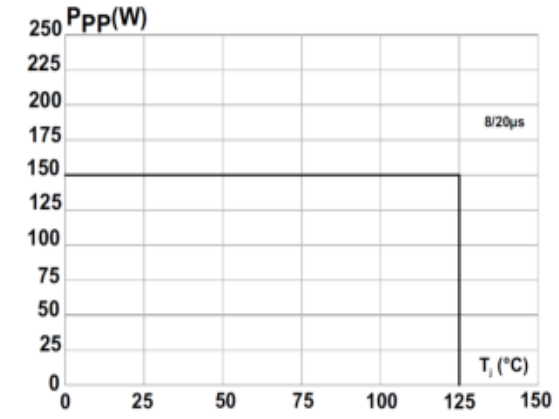


Figure 3. Junction capacitance versus reverse applied voltage (typical values)

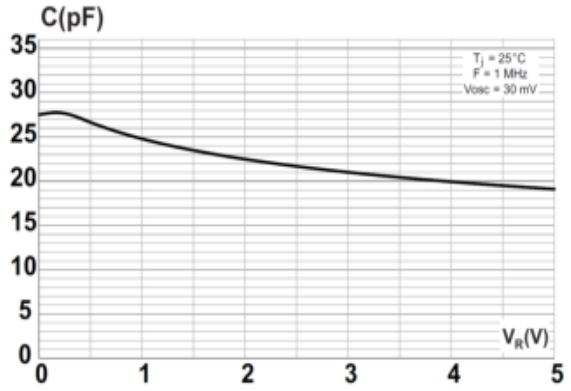


Figure 4. Peak pulse power versus exponential pulse duration (maximum values)

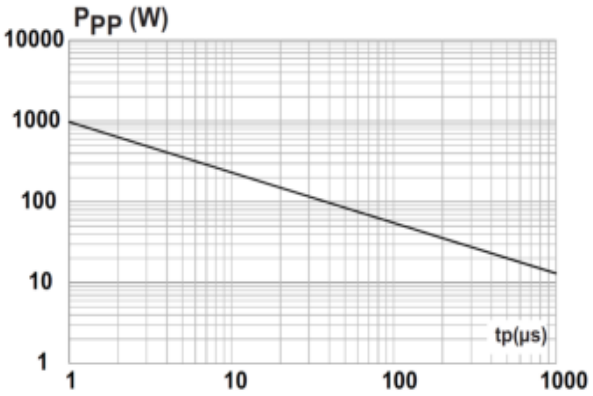


Figure 5. Clamping voltage versus peak pulse current (typical values)

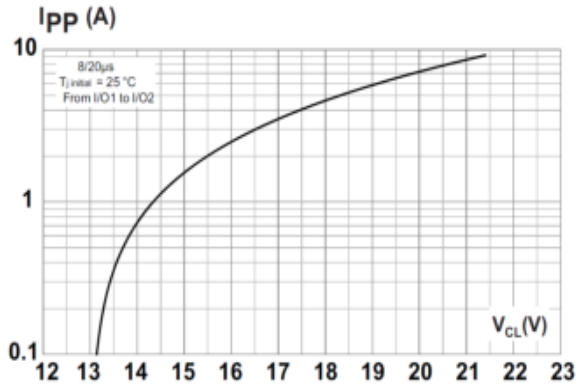


Figure 6. Clamping voltage versus peak pulse current (typical values)

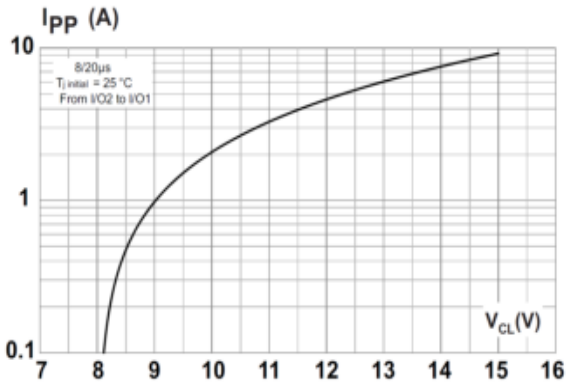


Figure 7. Leakage current versus junction temperature (typical values)

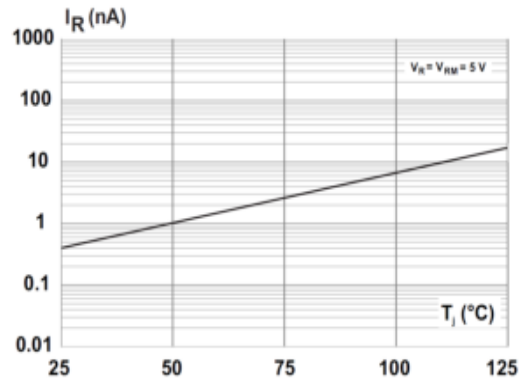


Figure 8. S21 attenuation measurement

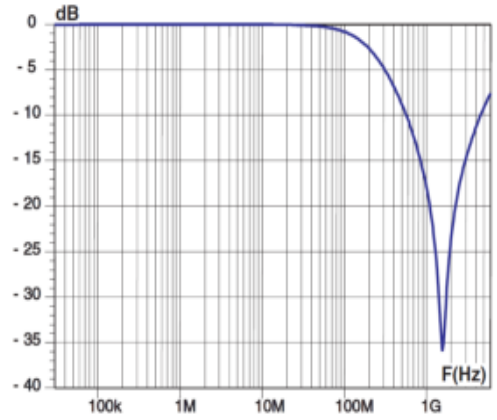


Figure 9. TLP measurements

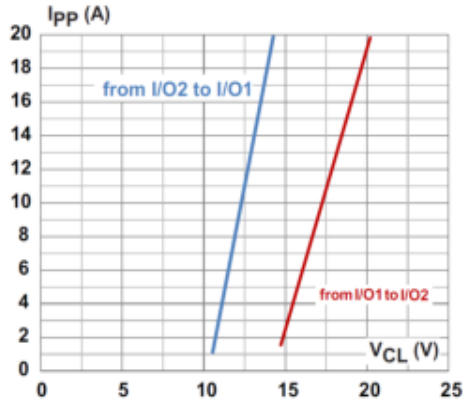


Figure 10. ESD response to ISO 10605, C = 150 pF, R = 330 Ω (+8 kV contact)

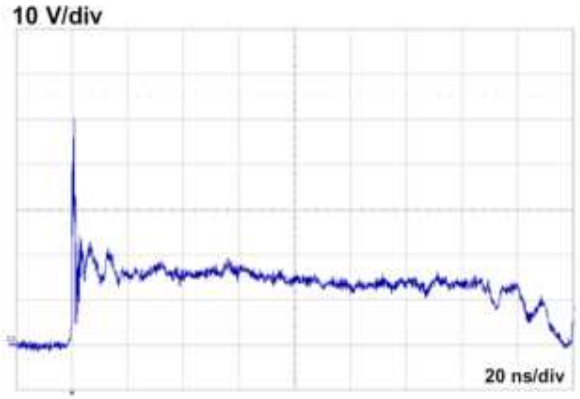


Figure 11. ESD response to ISO 10605, C = 150 pF, R = 330 Ω (-8 kV contact)

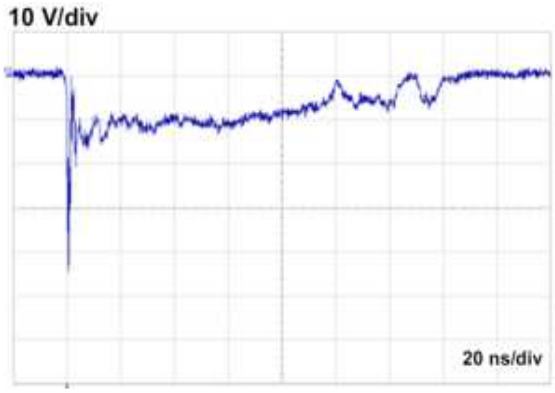


Figure 12. Response to ISO 7637-3 (pulse 3a) US = -150 V

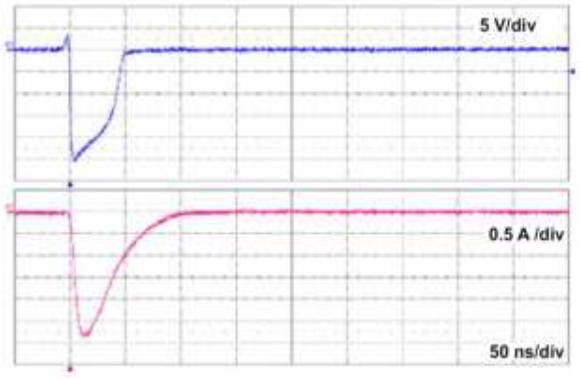
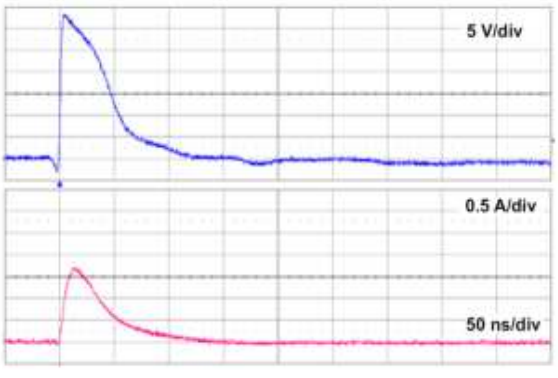


Figure 13. Response to ISO 7637-3 (pulse 3b) US = +100 V



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 Package information

Figure 14. Package outline

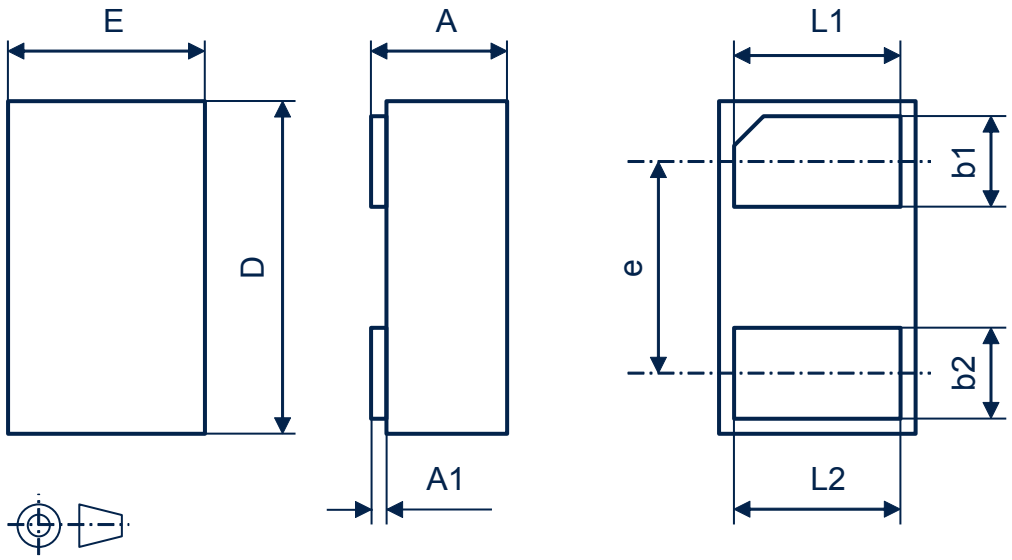
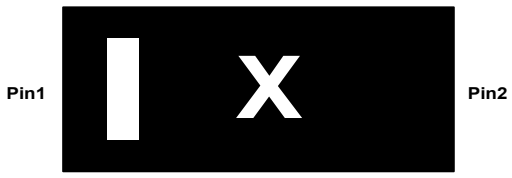


Table 3. Package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.30		0.40
A1	0.00		0.05
L1	0.45	0.50	0.55
L2	0.45	0.50	0.55
D	0.95	1.00	1.05
E	0.55	0.60	0.65
e	0.60	0.65	0.70
b1	0.20	0.25	0.30
b2	0.20	0.25	0.30

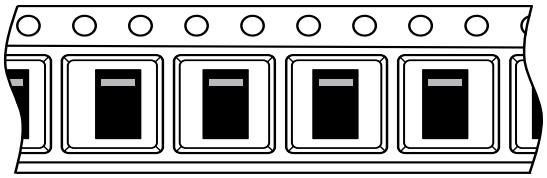
2.2 Packing and marking information

Figure 15. Marking layout



X: Refer to ordering information table for marking.

Figure 16. Package orientation in reel



Taped according to EIA-481

Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package
On bidirectional devices, marking and logo may be not always in the same direction

Figure 17. Tape leader and trailer dimensions

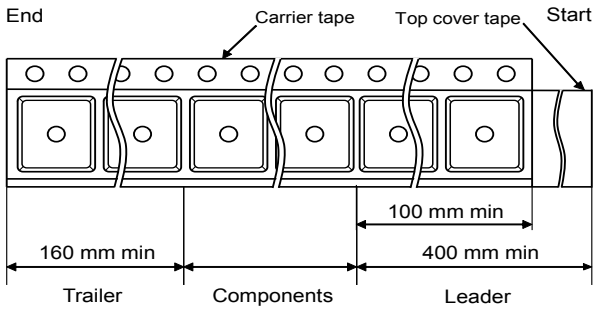


Figure 18. Tape and reel orientation

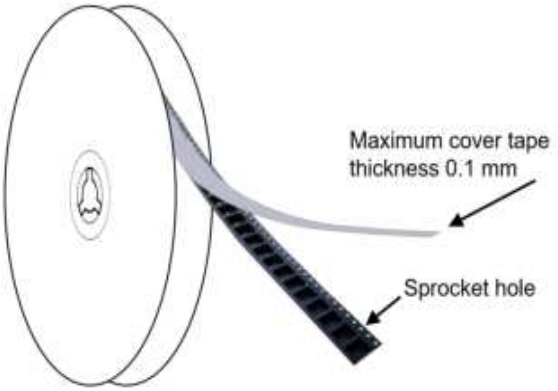


Figure 19. Reel dimensions (mm)

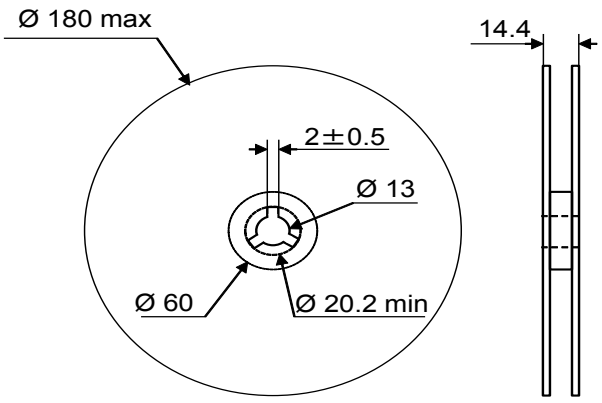


Figure 20. Inner box dimensions (mm)

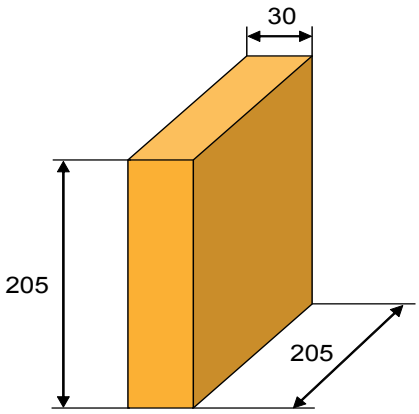
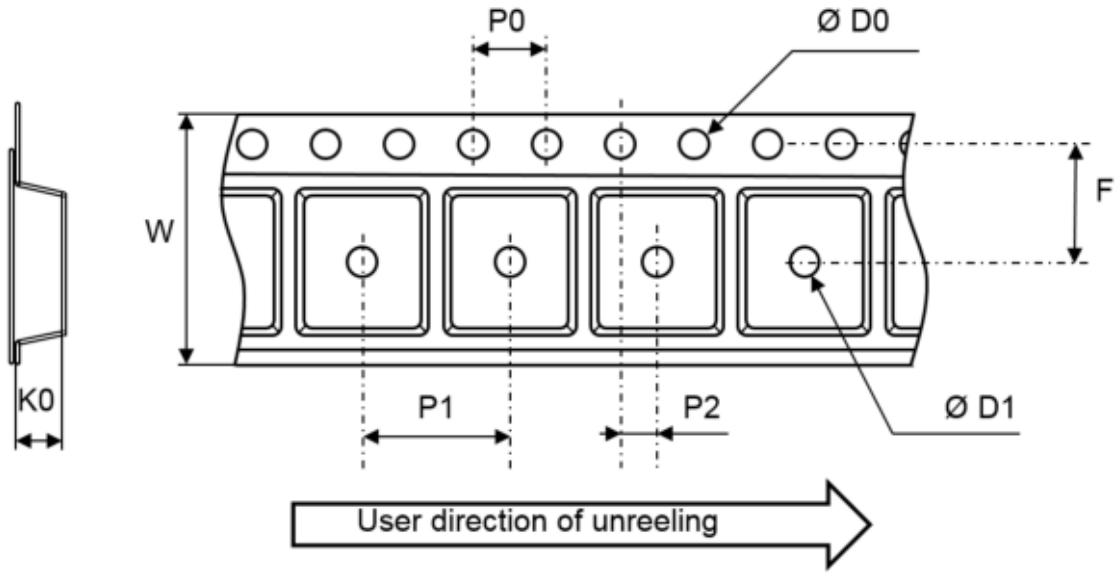


Figure 21. **Tape outline**



Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Table 4. **Tape and reel mechanical data**

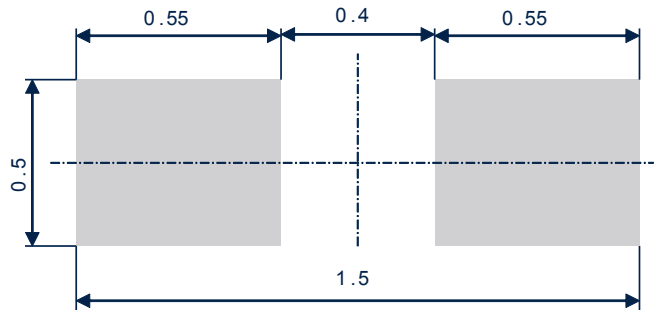
Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
D0	1.45	1.5	1.6
D1	0.35		
F	3.45	3.5	3.55
K0	0.42	0.47	0.52
P0	3.9	4	4.1
P1	1.95	2	2.05
P2	1.95	2	2.05
W	7.9	8	8.3

3 Recommendations on PCB assembly

3.1 Footprint

SMD footprint design is recommended.

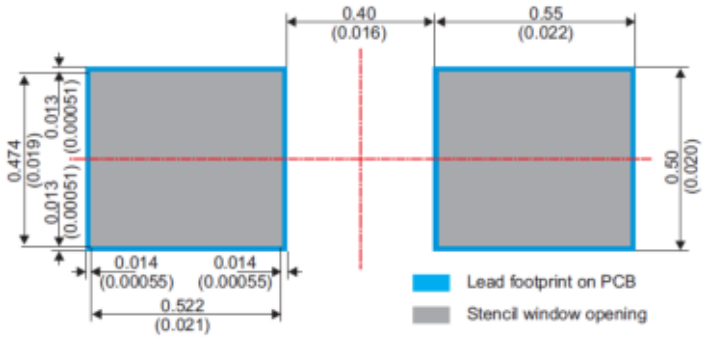
Figure 22. SOD882T recommended footprint



3.2 Stencil opening design

Stencil opening thickness: 100 µm

Figure 23. Stencil opening recommendations



3.3 Solder paste

1. Halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

3.4 Placement

1. Manual positioning is not recommended.

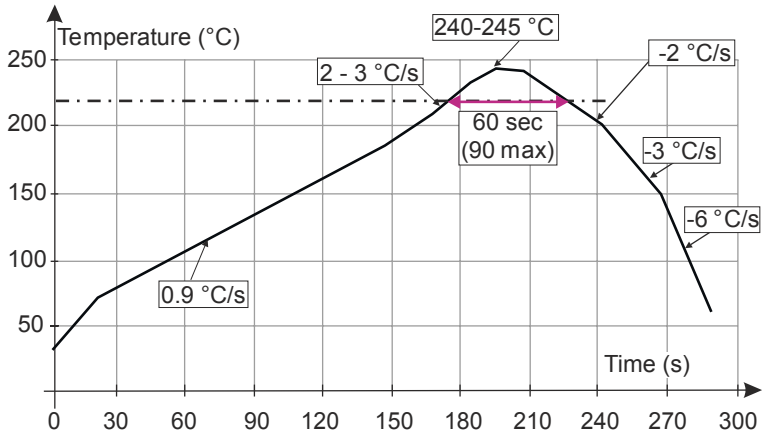
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. Any via around or inside the footprint area must be closed to avoid solderpaste migration in the via.
2. Position and dimensions of the tracks should be well balanced. A symmetrical layout is recommended to prevent assembly troubles.

3.6 Reflow profile

Figure 24. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Figure 25. **Ordering information scheme**

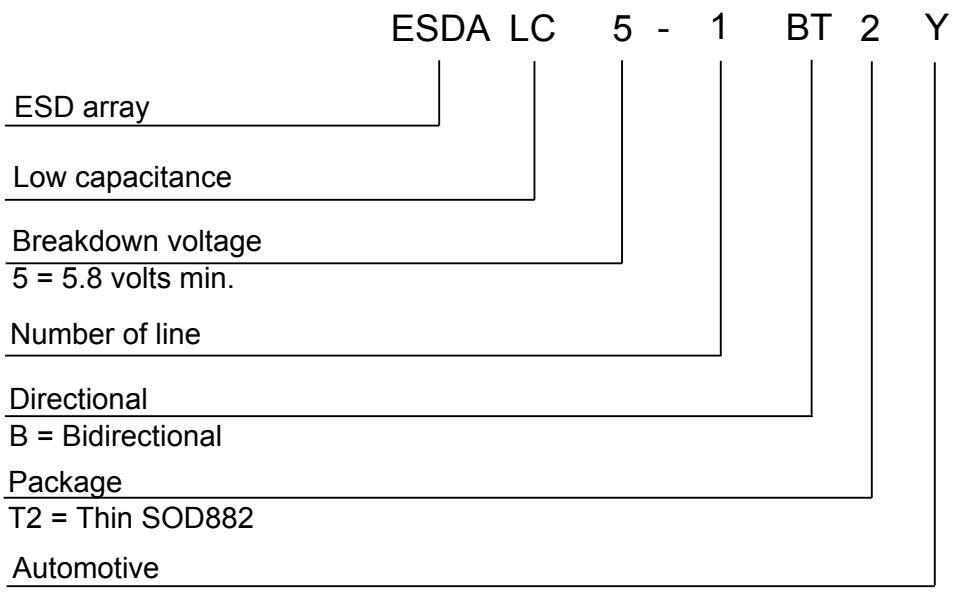


Table 5. **Ordering information**

Order code	Marking[1]	Package	Weight	Base qty.	Delivery mode
ESDALC5-1BT2Y	A	SOD882T (0402)	0.80 mg	12000	Tape and reel

1. *The marking can be rotated by multiples of 90° to differentiate assembly location*

Revision history

Table 6. **Document revision history**

Date	Version	Changes
03-Nov-2014	1	Initial release.
16-Sep-2022	2	Updated SOD882T (0402) package information. Minor text changes.

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