# STL45P3LLH6

## P-channel -30 V, 11 mΩ typ., -45 A STripFET™ H6 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

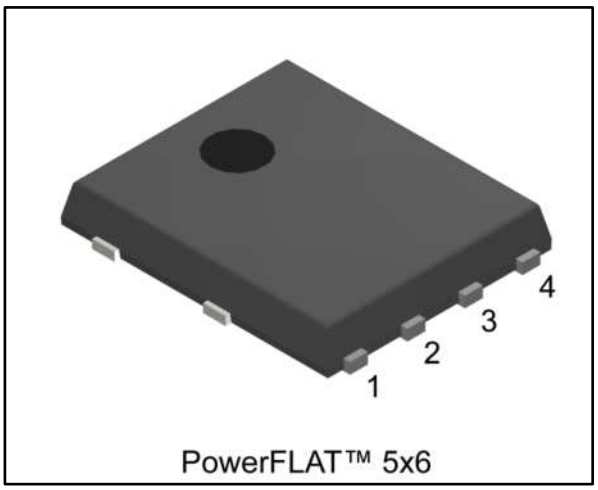
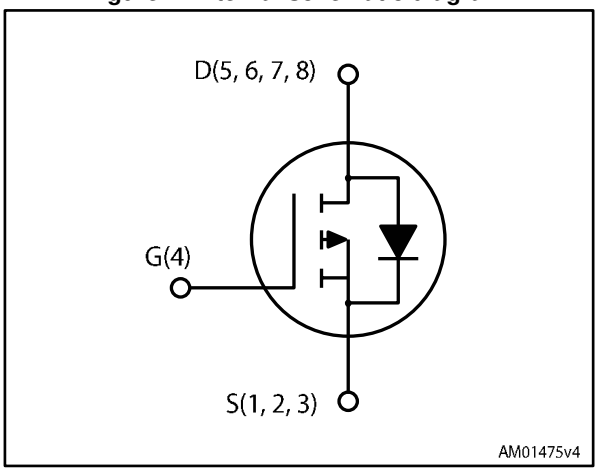



**Figure 1: Internal schematic diagram**




## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|---|
| STL45P3LLH6 | -30 V | 13 mΩ | -45 A |

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

## Applications

- Switching applications

## Description

This device is a P-channel Power MOSFET developed using the STripFET™ H6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

**Table 1: Device summary**

| Order code | Marking | Package | Packing |
|---|---|---|---|
| STL45P3LLH6 | 45P3LLH6 | PowerFLAT™ 5x6 | Tape and reel |



This is information on a product in full production.

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | -30 | V |
| $V_{GS}$ | Gate-source voltage | ± 20 | V |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 25 °C | -45 | A |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 100 °C | -34 | A |
| $I_D$ (2) | Drain current (continuous) at $T_{pcb}$ = 25 °C | -12 | A |
| $I_D$ (2) | Drain current (continuous) at $T_{pcb}$ = 100 °C | -8.7 | A |
| $I_{DM}$ (1)(3) | Drain current (pulsed) | -180 | A |
| $I_{DM}$ (2)(3) | Drain current (pulsed) | -48 | A |
| $P_{TOT}$ (1) | Total dissipation at $T_c$= 25 °C | 75 | W |
| $P_{TOT}$ (2) | Total dissipation at $T_{pcb}$= 25 °C | 4.8 | W |
| $T_{stg}$ | Storage temperature range | - 55 to 175 | °C |
| $T_j$ | Operating junction temperature range | | |

**Notes:**

(1)The value is rated according to $R_{thj\text{-}c}$.

(2)This value is rated according to $R_{thj\text{-}pcb}$

(3)Pulse width is limited by safe operating area

**Table 3: Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case | 2.00 | °C/W |
| $R_{thj\text{-}pcb}$ (1) | Thermal resistance junction-pcb | 31.3 | °C/W |

**Notes:**

(1)When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

# 2 Electrical characteristics

($T_C$ = 25 °C unless otherwise specified)

**Table 4: On /off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0, $I_D$ = - 1 mA | -30 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0, $V_{DS}$ = -30 V | | | -1 | µA |
| | | $V_{GS}$ = 0, $V_{DS}$ = -30 V, $T_C$ = 125 °C (1) | | | -10 | µA |
| $I_{GSS}$ | Gate-body leakage current | $V_{DS}$ = 0, $V_{GS}$ = ± 20 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = -250 µA | -1 | | | V |
| $R_{DS(on)}$ | Static drain-source on- resistance | $V_{GS}$ = -10 V, $I_D$ =-6 A | | 11 | 13 | mΩ |
| | | $V_{GS}$ = -4.5 V, $I_D$ = -6 A | | 16 | 19.5 | mΩ |

**Notes:**

(1)Defined by design, not subject to production test.

**Table 5: Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = -25 V, f = 1 MHz, $V_{GS}$ = 0 | - | 2615 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 340 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 235 | - | pF |
| $Q_g$ | Total gate charge | $V_{DD}$ = -15 V, $I_D$ = -12 A, $V_{GS}$ = -4.5 V | - | 24 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 9 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 8 | - | nC |

**Table 6: Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = -15 V, $I_D$ = -6 A, $R_G$ = 4.7 Ω, $V_{GS}$ = -10 V | - | 13.2 | - | ns |
| $t_r$ | Rise time | | - | 93 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 50 | - | ns |
| $t_f$ | Fall time | | - | 18 | - | ns |

**Table 7: Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SD}$ (1) | Forward on voltage | $I_{SD}$ = -6 A, $V_{GS}$ = 0 | - | | -1.1 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = -6 A, di/dt = 100 A/µs<br>$V_{DD}$ = -16 V, $T_j$=150 °C | - | 20 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 16 | | nC |
| $I_{RRM}$ | Reverse recovery current | | - | -1.6 | | A |

**Notes:**

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

## 2.2 Electrical characteristics (curves)

Note: For the P-channel Power MOSFET, current and voltage polarities are reversed.

**Figure 2: Safe operating area**

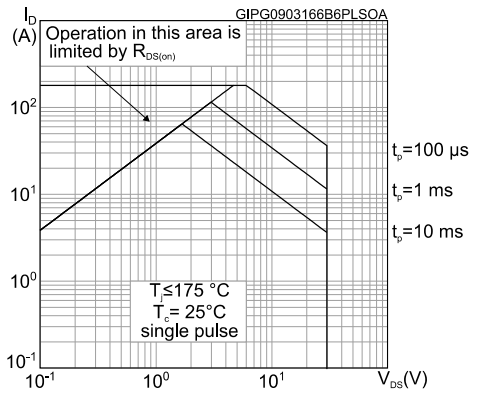



**Figure 3: Thermal impedance**

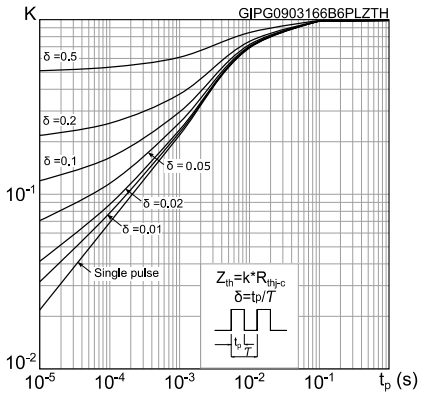



**Figure 4: Output characteristics**

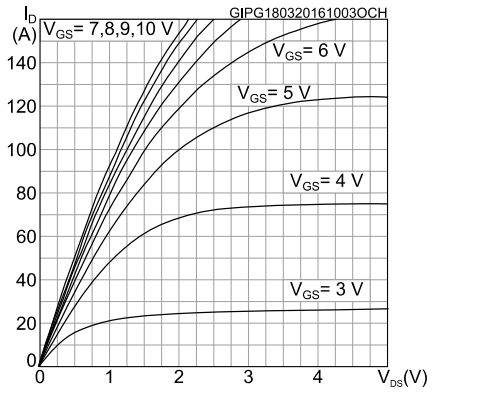



**Figure 5: Transfer characteristics**

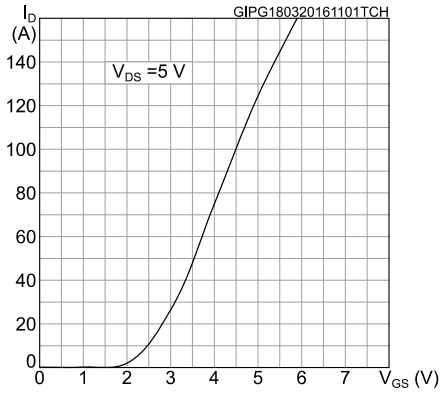



**Figure 6: Gate charge vs gate-source voltage**

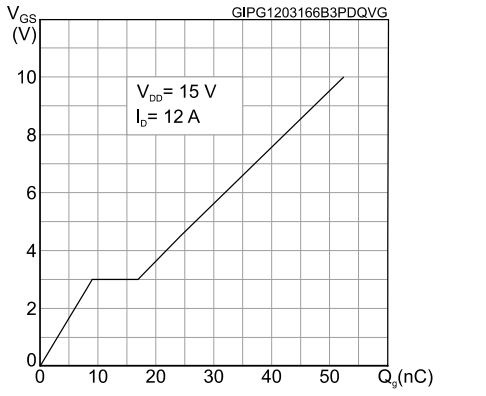



**Figure 7: Static drain-source on-resistance**

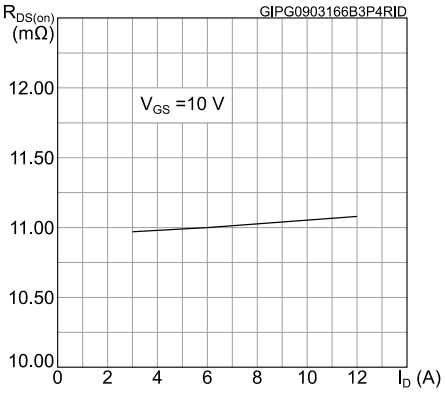


**Figure 8: Capacitance variations**

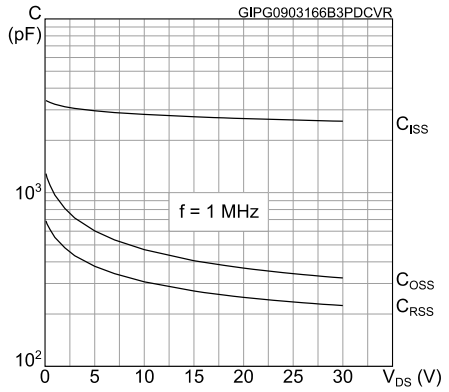



**Figure 9: Normalized gate threshold voltage vs temperature**

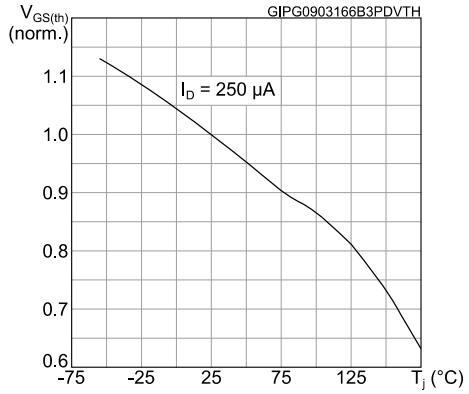



**Figure 10: Normalized on-resistance vs temperature**

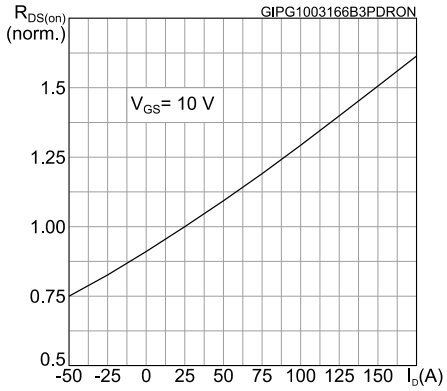



**Figure 11: Normalized $V_{(BR)DSS}$ vs temperature**

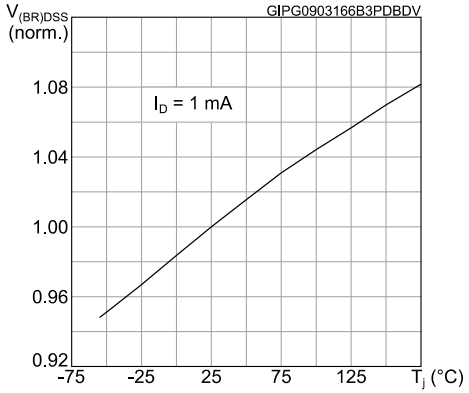
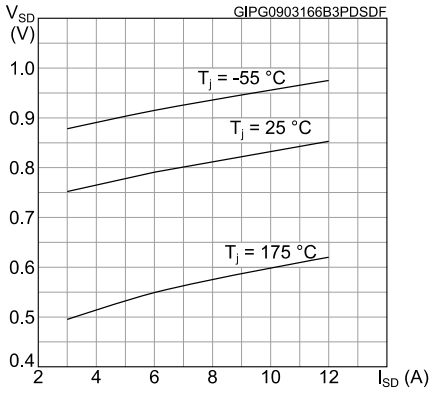



**Figure 12: Source-drain diode forward characteristics**



# 3 Test circuits

**Figure 13: Switching times test circuit for resistive load**

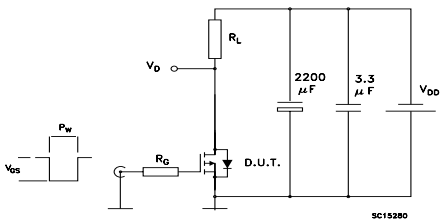



**Figure 14: Gate charge test circuit**

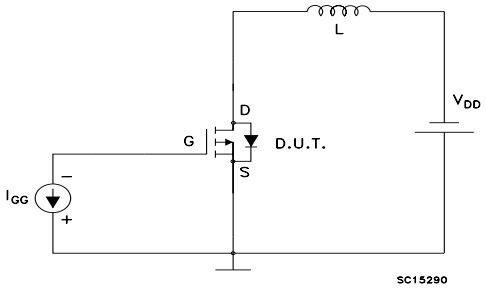
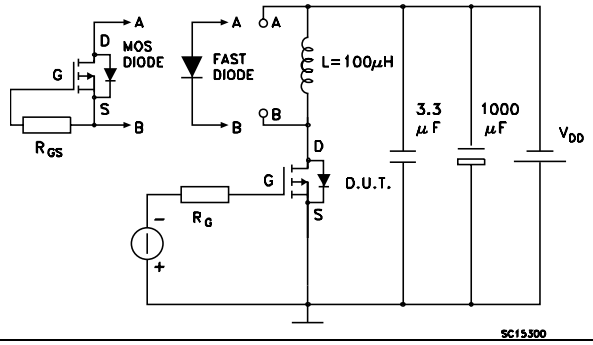



**Figure 15: Test circuit for inductive load switching and diode recovery times**



# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

## 4.1 PowerFLAT™ 5x6 package information

**Figure 16: PowerFLAT™ 5x6 type R package outline**

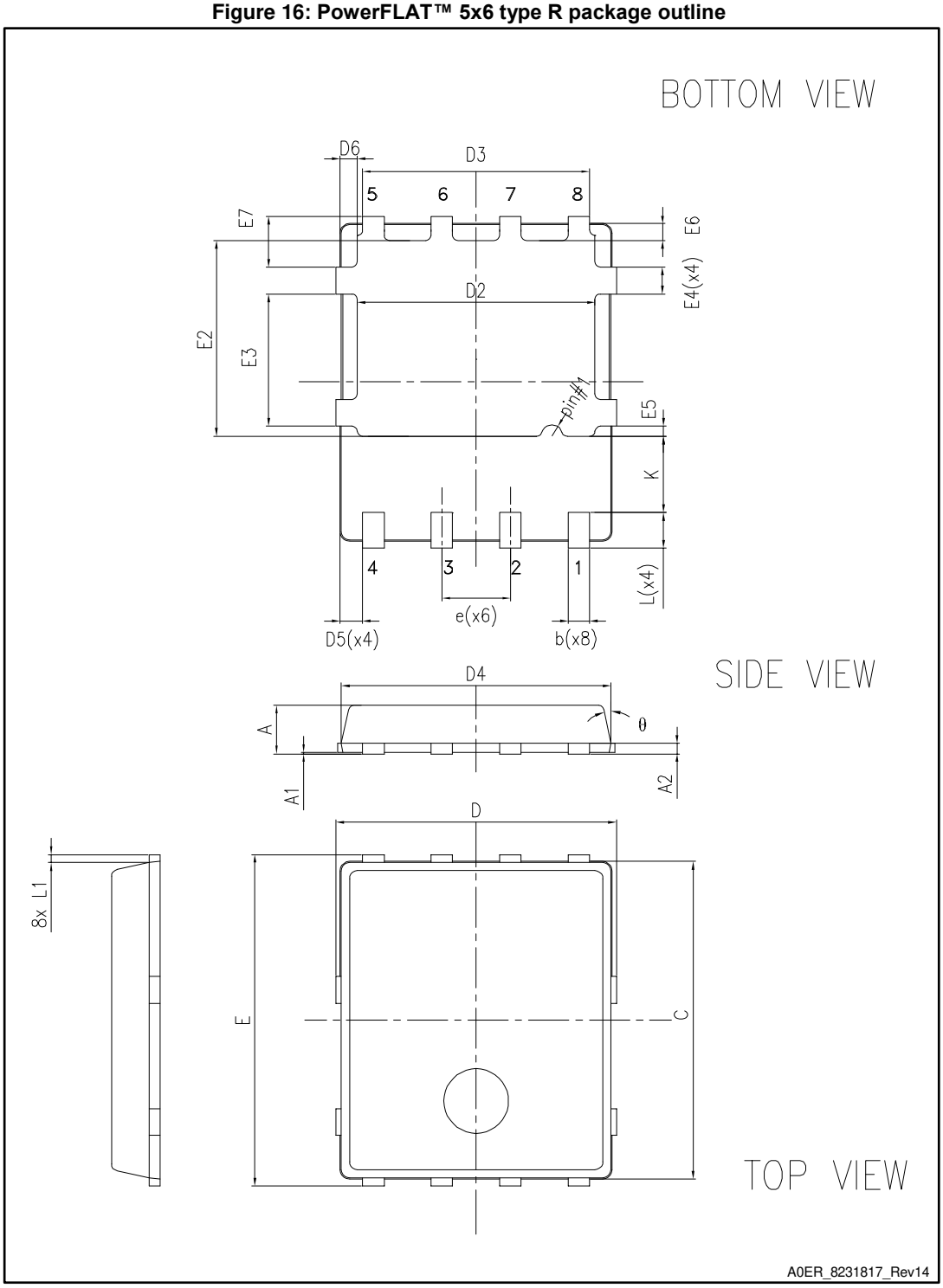
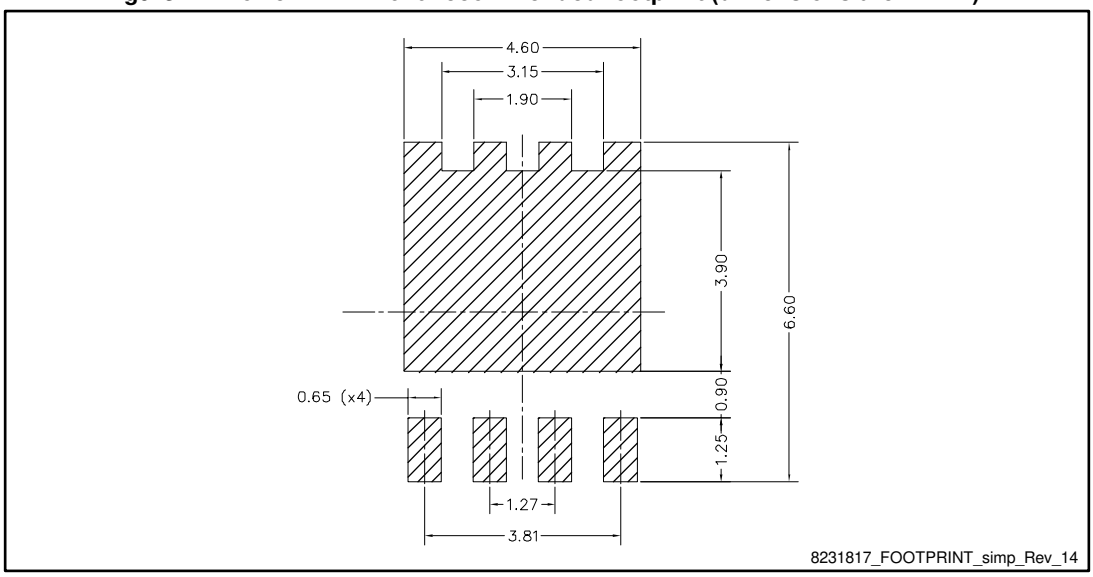


Table 8: PowerFLAT™ 5x6 type R mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.80 | | 1.00 |
| A1 | 0.02 | | 0.05 |
| A2 | | 0.25 | |
| b | 0.30 | | 0.50 |
| C | 5.80 | 6.00 | 6.20 |
| D | 5.00 | 5.20 | 5.40 |
| D2 | 4.15 | | 4.45 |
| D3 | 4.05 | 4.20 | 4.35 |
| D4 | 4.80 | 5.00 | 5.20 |
| D5 | 0.25 | 0.40 | 0.55 |
| D6 | 0.15 | 0.30 | 0.45 |
| e | | 1.27 | |
| E | 5.95 | 6.15 | 6.35 |
| E2 | 3.50 | | 3.70 |
| E3 | 2.35 | | 2.55 |
| E4 | 0.40 | | 0.60 |
| E5 | 0.08 | | 0.28 |
| E6 | 0.20 | 0.325 | 0.45 |
| E7 | 0.75 | 0.90 | 1.05 |
| K | 1.275 | | 1.575 |
| L | 0.60 | | 0.80 |
| L1 | 0.05 | 0.15 | 0.25 |
| θ | | 0° | 12° |

Figure 17: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



## 4.2 PowerFLAT™ 5x6 packaging information

**Figure 18: PowerFLAT™ 5x6 tape (dimensions are in mm)**

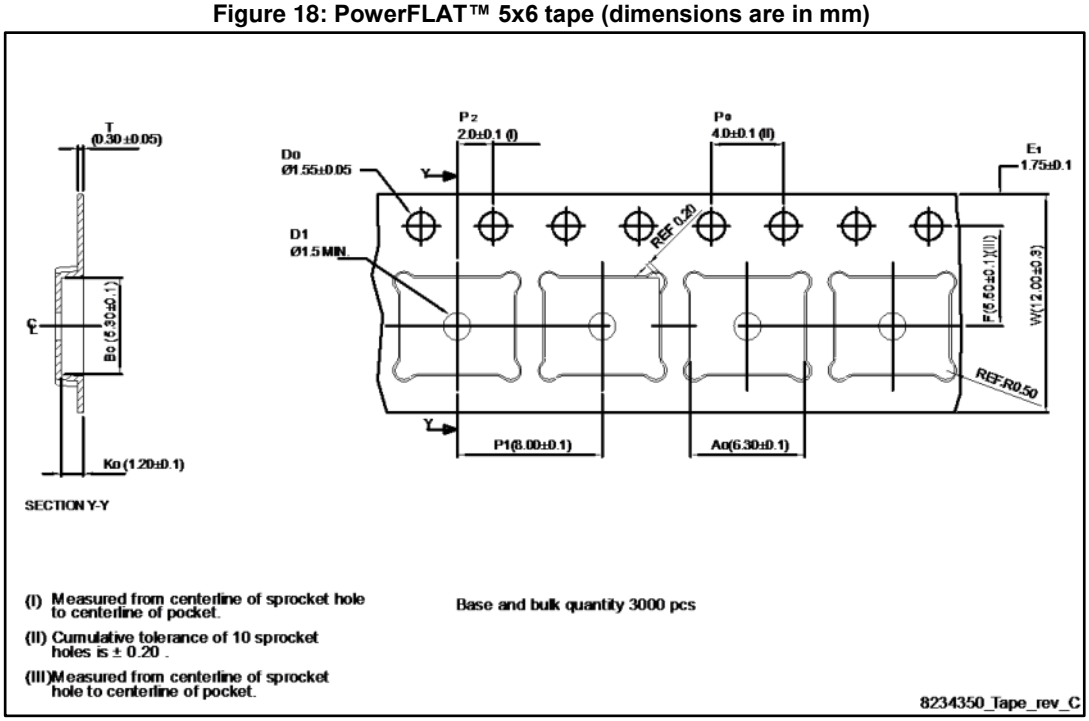



**Figure 19: PowerFLAT™ 5x6 package orientation in carrier tape**

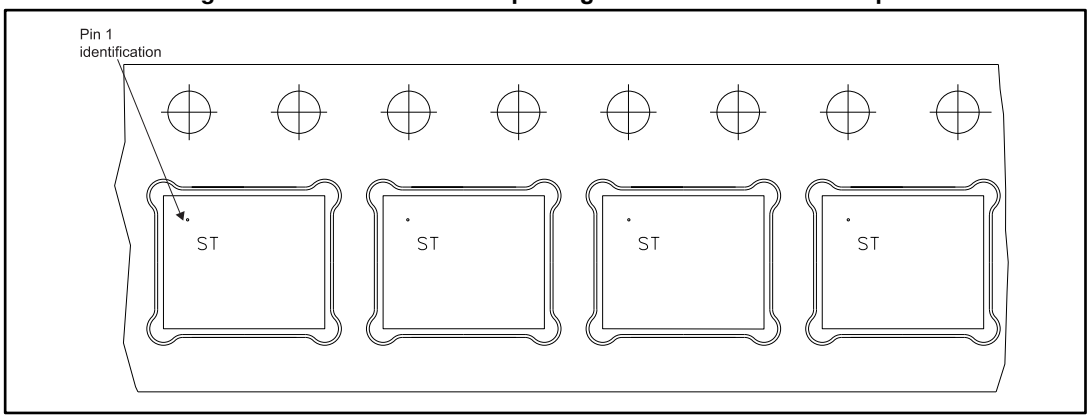
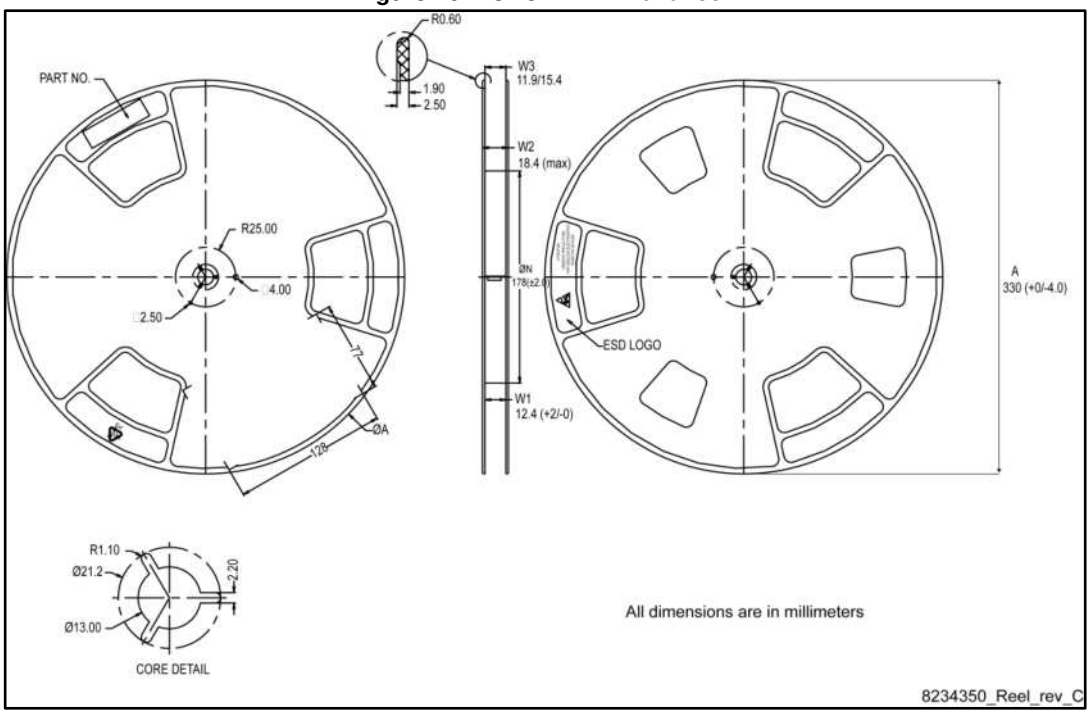


**Figure 20: PowerFLAT™ 5x6 reel**



# 5 Revision history

Table 9: Document revision history

| Date | Revision | Changes |
|---|---|---|
| 01-Apr-2016 | 1 | First release. |

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