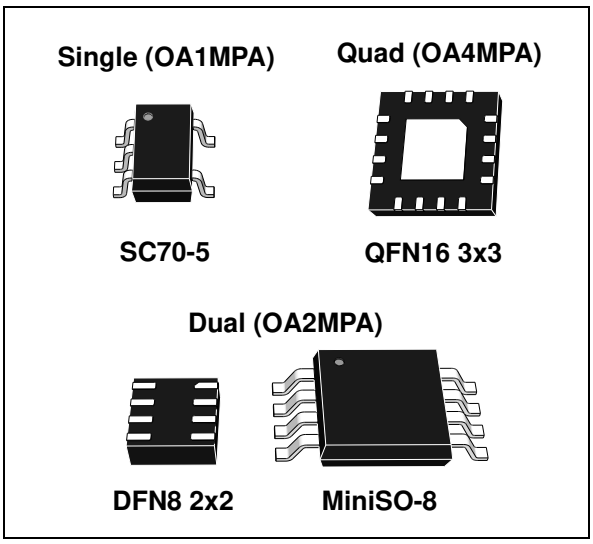
OA1MPA, OA2MPA, OA4MPA

High precision low-power CMOS op amp

Datasheet - production data



Features

- Low offset voltage: 200 µV max.
- Low power consumption: 10 µA at 5 V
- Low supply voltage: 1.5 V to 5.5 V
- Gain bandwidth product: 150 kHz typ.
- Low input bias current: 1 pA typ.
- Rail-to-rail input and output
- EMI hardened operational amplifiers
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40 to +125 °C

Benefits

- High precision without calibration
- Energy saving
- Guaranteed operation on low-voltage battery

Applications

- Wearable
- Fitness and healthcare
- Medical instrumentation

Description

The OA1MPA, OA2MPA, OA4MPA series of single, dual, and quad operational amplifiers offer low-voltage operation, rail-to-rail input and output, and excellent precision (V_{io} lower than 200 µV at 25 °C).

These low power op amps benefit from STMicroelectronics 5 V CMOS technology and offer an excellent speed/power consumption ratio (150 kHz typical gain bandwidth) while consuming less than 14 µA at 5 V. The OA1MPA, OA2MPA, OA4MPA series also feature an ultra-low input bias current.

The OA1MPA, OA2MPA, OA4MPA are respectively the single, dual and quad operational amplifier versions and are housed in the smallest industrial package.

The OA1MPA, OA2MPA, OA4MPA family is the ideal choice for wearable, fitness and healthcare applications.

Table 1. Device summary

Order code	Temperature range	Package	Packaging	Marking
OA1MPA22C	-40° C to +125° C	SC70-5	Tape and reel	K1W
OA2MPA22Q		DFN8 2x2		K1W
OA2MPA34S		MiniSO8		V712
OA4MPA33Q		QFN16 3x3		K1W

This is information on a product in full production. www.st.com

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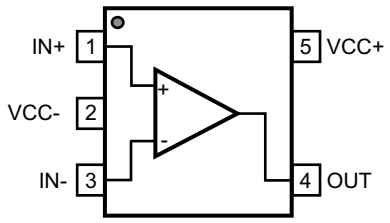
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1 Pin connections

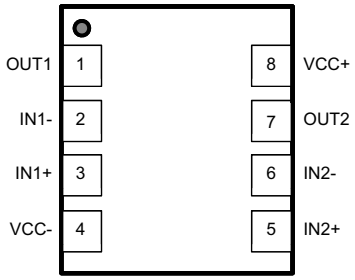
Figure 1. Pin connections (top view)

Single

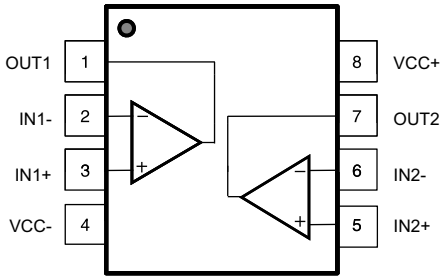


SC70-5 (OA1MPA)

Dual

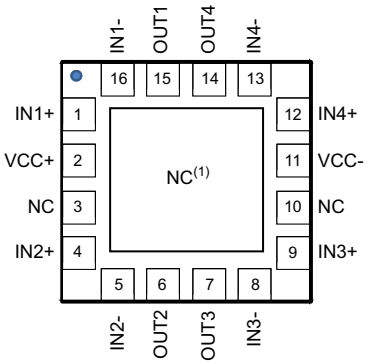


DFN8 2x2 (OA2MPA)



MiniSO-8 (OA2MPA)

Quad



QFN16 3x3 (OA4MPA)

1. The exposed pads of the QFN16 3x3 can be connected to VCC- or left floating.

2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	6	V
V_{id}	Differential input voltage(2)	$\pm V_{CC}$	
V_{in}	Input voltage(3)	V_{CC-} - 0.2 to V_{CC+} + 0.2	
I_{in}	Input current(4)	10	mA
T_{stg}	Storage temperature	-65 to +150	°C
R_{thja}	Thermal resistance junction-to-ambient(5)(6) SC70-5 DFN8 2x2 MiniSO8 QFN16 3x3	 205 120 190 45	°C/W
R_{thjc}	Thermal resistance junction-to-case DFN8 2x2	33	
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model(7)	4	kV
	MM: machine model for OA1MPA(8)	150	V
	MM: machine model for OA2MPA(8)	200	
	MM: machine model for OA4MPA(8)	300	
	CDM: charged device model except MiniSO8(9)	1.5	kV
	CDM: charged device model for MiniSO8(9)	1.3	
	Latch-up immunity	200	mA

1. All voltage values, except the differential voltage are with respect to the network ground terminal.
2. The differential voltage is a non-inverting input terminal with respect to the inverting input terminal. The OA2MPA and OA4MPA devices include an internal differential voltage limiter that clamps internal differential voltage at 0.5 V.
3. V_{CC} - V_{in} must not exceed 6 V, V_{in} must not exceed 6 V.
4. Input current must be limited by a resistor in series with the inputs.
5. Short-circuits can cause excessive heating and destructive dissipation.
6. R_{th} are typical values.
7. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
8. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
9. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.5 to 5.5	V
V_{icm}	Common mode input voltage range	V_{CC-} - 0.1 to V_{CC+} + 0.1	
T_{oper}	Operating free air temperature range	-40 to +125	°C

3 Electrical characteristics

V_{CC+} = 1.8 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T = 25 °C, and R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Table 4. Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage (V_{icm} = 0 V)	T = 25 °C			200	µV
		-40 °C < T< 85 °C			850	
		-40 °C < T< 125 °C			1200	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 125 °C(1)			10	µV/°C
I_{io}	Input offset current (V_{out} = V_{CC}/2)	T = 25 °C		1	10(2)	pA
		-40 °C < T< 125 °C		1	300(2)	
I_{ib}	Input bias current (V_{out} = V_{CC}/2)	T = 25 °C		1	10(2)	
		-40 °C < T< 125 °C		1	300(2)	
CMR	Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$) V_{icm} = 0 V to V_{CC}, V_{out} = V_{CC}/2, R_L > 1 MΩ	T = 25 °C	69	88		dB
		-40 °C < T< 125 °C	61			
A_{vd}	Large signal voltage gain V_{out} = 0.5 V to (V_{CC} - 0.5 V)	T = 25 °C	95			
		-40 °C < T< 125 °C	85			
V_{OH}	High level output voltage (V_{OH} = V_{CC} - V_{out})	T = 25 °C			75	mV
		-40 °C < T< 125 °C			80	
V_{OL}	Low level output voltage	T = 25 °C			40	
		-40 °C < T< 125 °C			60	
I_{out}	I_{sink} (V_{out} = V_{CC})	T = 25 °C	6	12		mA
		-40 °C < T< 125 °C	4			
	I_{source} (V_{out} = 0 V)	T = 25 °C	5	7		
		-40 °C < T< 125 °C	3			
I_{CC}	Supply current (per channel, V_{out} = V_{CC}/2, R_L > 1 MΩ	T = 25 °C		9	14	µA
		-40 °C < T< 125 °C			16	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	100	120		kHz
F_u	Unity gain frequency			100		
F_m	Phase margin			45		Degrees
G_m	Gain margin			19		dB

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SR	Slew rate(3)	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V		0.04		V/µs
e_n	Equivalent input noise voltage	f = 1 kHz		100		$\frac{nV}{\sqrt{Hz}}$
		f = 10 kHz		96		
t_{init}	Initialization time(4)	T = 25 °C			5	ms
		-40 °C < T< 125 °C			60	

1. See *Section 4.4: Input offset voltage drift over temperature*.
2. Guaranteed by characterization.
3. Slew rate value is calculated as the average between positive and negative slew rates.
4. Initialization time is defined as the delay after power-up to guarantee operation within specified performances. Guaranteed by design. See *Section 4.6: Initialization time*.

V_{CC+} = 3.3 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T = 25 °C, and R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Table 5. Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C			200	µV
		-40 °C < T< 85 °C			850	
		-40 °C < T< 125 °C			1200	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 125 °C(1)			10	µV/°C
ΔV_{io}	Long-term input offset voltage drift	T = 25 °C(2)		0.3		$\frac{\mu V}{\sqrt{month}}$
I_{io}	Input offset current (V_{out} = V_{CC}/2)	T = 25 °C		1	10(3)	pA
		-40 °C < T< 125 °C		1	300(3)	
I_{ib}	Input bias current (V_{out} = V_{CC}/2)	T = 25 °C		1	10(3)	
		-40 °C < T< 125 °C		1	300(3)	
CMR	Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$) V_{icm} = 0 V to V_{CC}, V_{out} = V_{CC}/2, R_L > 1 MΩ	T = 25 °C	80	100		dB
		-40 °C < T< 125 °C	69			
A_{vd}	Large signal voltage gain V_{out} = 0.5 V to (V_{CC} - 0.5 V)	T = 25 °C	95			
		-40 °C < T< 125 °C	85			
V_{OH}	High level output voltage (V_{OH} = V_{CC} - V_{out})	T = 25 °C			75	mV
		-40 °C < T< 125 °C			80	
V_{OL}	Low level output voltage	T = 25 °C			40	
		-40 °C < T< 125 °C			60	
I_{out}	I_{sink} (V_{out} = V_{CC})	T = 25 °C	20	34		mA
		-40 °C < T< 125 °C	15			
	I_{source} (V_{out} = 0 V)	T = 25 °C	20	26		
		-40 °C < T< 125 °C	15			
I_{CC}	Supply current (per channel, V_{out} = V_{CC}/2, R_L > 1 MΩ)	T = 25 °C		9	14	µA
		-40 °C < T< 125 °C			16	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF	100	120		kHz
F_u	Unity gain frequency			100		
F_m	Phase margin			45		Degrees
G_m	Gain margin			19		dB
SR	Slew rate(4)	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V		0.05		V/µs

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
e_n	Equivalent input noise voltage	f = 1 kHz		100		$\frac{nV}{\sqrt{Hz}}$
		f = 10 kHz		96		
t_{init}	Initialization time(5)	T = 25 °C			5	ms
		-40 °C < T< 125 °C			50	

1. See *Section 4.4: Input offset voltage drift over temperature*.
2. Typical value is based on the V_{io} drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration. See *Section 4.5: Long-term input offset voltage drift*.
3. Guaranteed by characterization.
4. Slew rate value is calculated as the average between positive and negative slew rates.
5. Initialization time is defined as the delay after power-up which guarantees operation within specified performances. Guaranteed by design. See *Section 4.6: Initialization time*.

V_{CC+} = 5 V with V_{CC-} = 0 V, V_{icm} = V_{CC}/2, T = 25 °C, and R_L = 10 kΩ connected to V_{CC}/2 (unless otherwise specified)

Table 6. Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C			200	µV
		-40 °C < T< 85 °C			850	
		-40 °C < T< 125 °C			1200	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 125 °C(1)			10	µV/°C
ΔV_{io}	Long-term input offset voltage drift	T = 25 °C(2)		0.7		$\frac{\mu V}{\sqrt{month}}$
I_{io}	Input offset current (V_{out} = V_{CC}/2)	T = 25 °C		1	10(3)	pA
		-40 °C < T< 125 °C		1	300(3)	
I_{ib}	Input bias current (V_{out} = V_{CC}/2)	T = 25 °C		1	10(3)	
		-40 °C < T< 125 °C		1	300(3)	
CMR	Common mode rejection ratio 20 log ($\Delta V_{icm}/\Delta V_{io}$) V_{icm} = 0 V to V_{CC}, V_{out} = V_{CC}/2, R_L > 1 MΩ	T = 25 °C	74	94		dB
		-40 °C < T< 125 °C	73			
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$) V_{CC} = 1.5 to 5.5 V, V_{ic} = 0 V, R_L > 1 MΩ	T = 25 °C	71	90		
		-40 °C < T< 125 °C	71			
A_{vd}	Large signal voltage gain V_{out} = 0.5 V to (V_{CC} - 0.5 V)	T = 25 °C	95			
		-40 °C < T< 125 °C	85			
EMIRR	EMI rejection ratio EMIRR = 20 log ($V_{RFpeak}/\Delta V_{io}$)	$V_{RF\ =\ 100\ mV}$ RFpeak, f = 400 MHz		38(4)		
		$V_{RF\ =\ 100\ mV}$ RFpeak, f = 900 MHz		50(4)		
		$V_{RF\ =\ 100\ mV}$ RFpeak, f = 1800 MHz		60(4)		
		$V_{RF\ =\ 100\ mV}$ RFpeak, f = 2400 MHz		63(4)		
V_{OH}	High level output voltage (V_{OH} = V_{CC} - V_{out})	T = 25 °C			75	mV
		-40 °C < T< 125 °C			80	
V_{OL}	Low level output voltage	T = 25 °C			40	
		-40 °C < T< 125 °C			60	
I_{out}	I_{sink} (V_{out} = V_{CC})	T = 25 °C	35	56		mA
		-40 °C < T< 125 °C	20			
	I_{source} (V_{out} = 0 V)	T = 25 °C	35	45		
		-40 °C < T< 125 °C	20			

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current (per channel, $V_{out} = V_{CC}/2$, $R_L > 1\ M\Omega$)	T = 25 °C		10	14	µA
		-40 °C < T< 125 °C			16	
AC performance						
GBP	Gain bandwidth product	$R_L = 10\ k\Omega$, $C_L = 100\ pF$	110	150		kHz
F_u	Unity gain frequency			120		
F_m	Phase margin			45		Degrees
G_m	Gain margin			19		dB
SR	Slew rate(5)	$R_L = 10\ k\Omega$, $C_L = 100\ pF$, $V_{out} = 0.5\ V$ to $V_{CC} - 0.5\ V$		0.06		V/µs
$\int e_n$	Low-frequency peak-to-peak input noise	Bandwidth: f = 0.1 to 10 Hz		10		μV_{pp}
e_n	Equivalent input noise voltage	f = 1 kHz		100		$\frac{nV}{\sqrt{Hz}}$
		f = 10 kHz		96		
THD+N	Total harmonic distortion + noise	$f_{in} = 1\ kHz$, $A_{CL} = 1$, $R_L = 100\ k\Omega$, $V_{icm} = (V_{CC} - 1\ V)/2$, BW = 22 kHz, $V_{out} = 0.5\ V_{pp}$		0.008		%
t_{init}	Initialization time(6)	T = 25 °C			5	ms
		-40 °C < T< 125 °C			50	

1. See *Section 4.4: Input offset voltage drift over temperature*.
2. Typical value is based on the V_{io} drift observed after 1000h at 125 °C extrapolated to 25 °C using the Arrhenius law and assuming an activation energy of 0.7 eV. The operational amplifier is aged in follower mode configuration. See *Section 4.5: Long-term input offset voltage drift*.
3. Guaranteed by characterization.
4. Tested on SC70-5 package.
5. Slew rate value is calculated as the average between positive and negative slew rates.
6. Initialization time is defined as the delay after power-up to guarantee operation within specified performances. Guaranteed by design. See *Section 4.6: Initialization time*.

Figure 2. Supply current vs. supply voltage at $V_{icm} = V_{CC}/2$

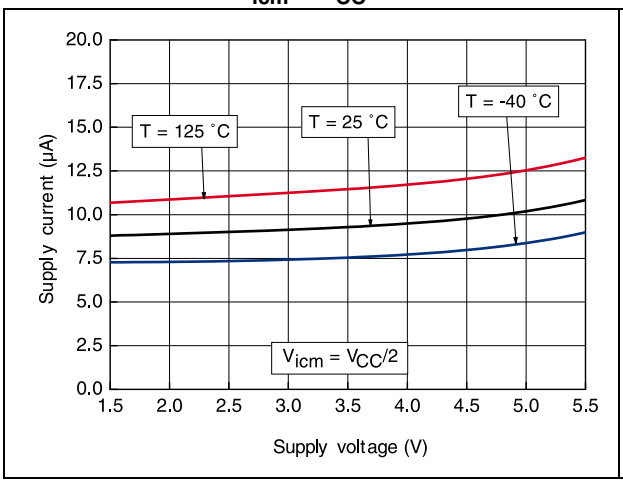


Figure 3. Input offset voltage distribution at $V_{CC} = 5$ V, $V_{icm} = V_{CC}/2$

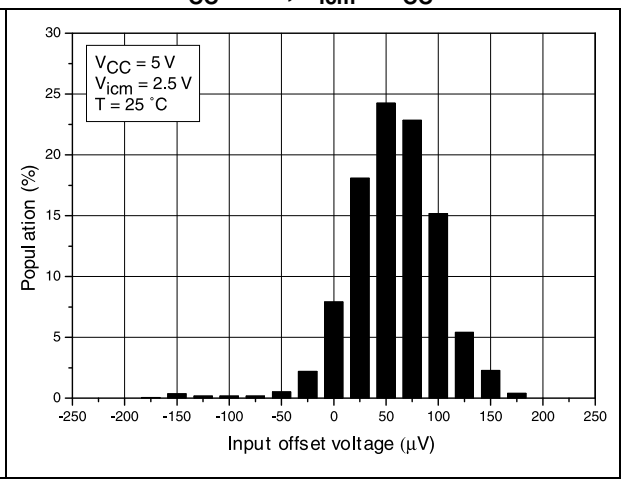


Figure 4. Input offset voltage distribution at $V_{CC} = 3.3$ V, $V_{icm} = V_{CC}/2$

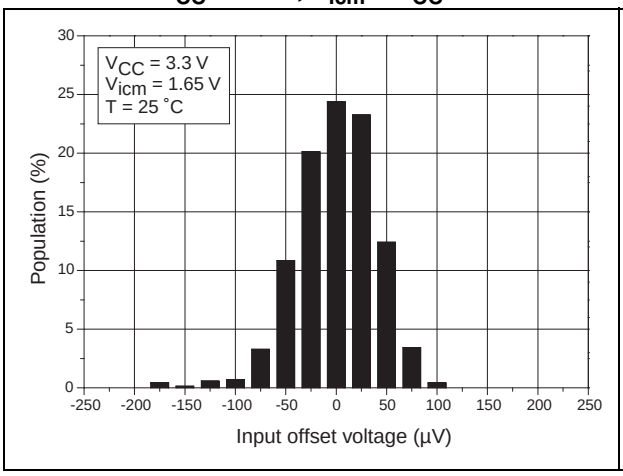


Figure 5. Input offset voltage temperature coefficient distribution

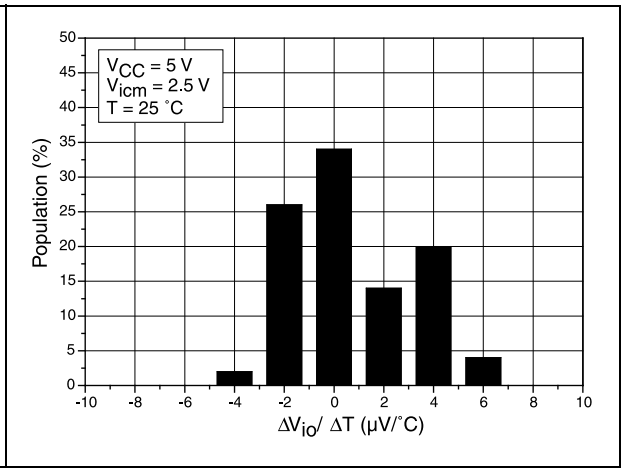


Figure 6. Input offset voltage vs. input common mode voltage

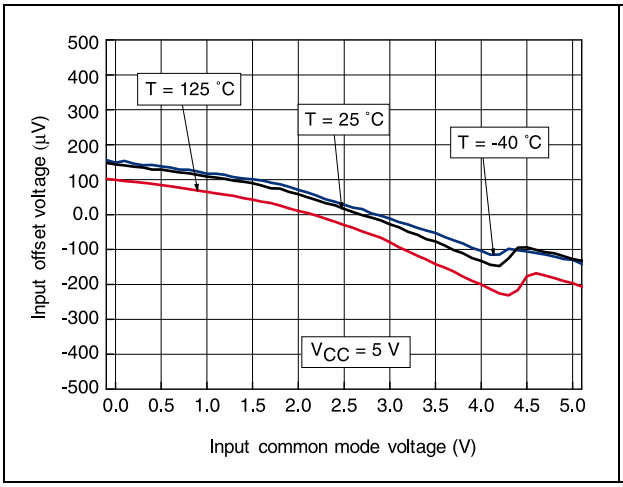


Figure 7. Input offset voltage vs. temperature

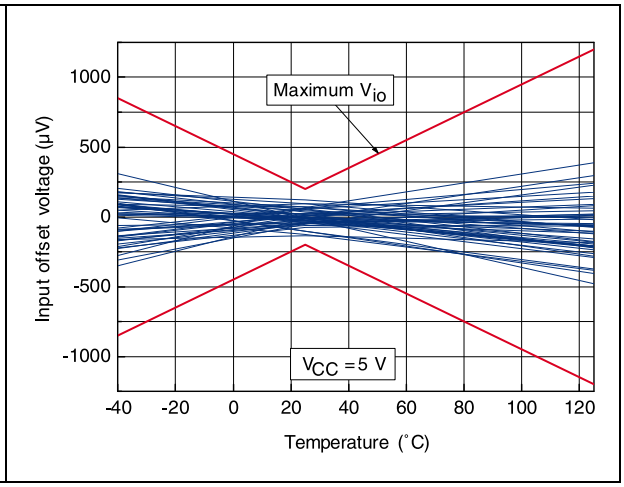


Figure 8. Output current vs. output voltage at V_{CC} = 1.5 V

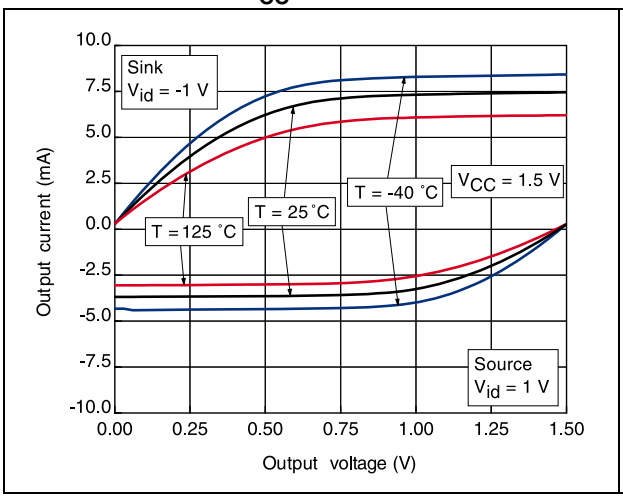


Figure 9. Output current vs. output voltage at V_{CC} = 5 V

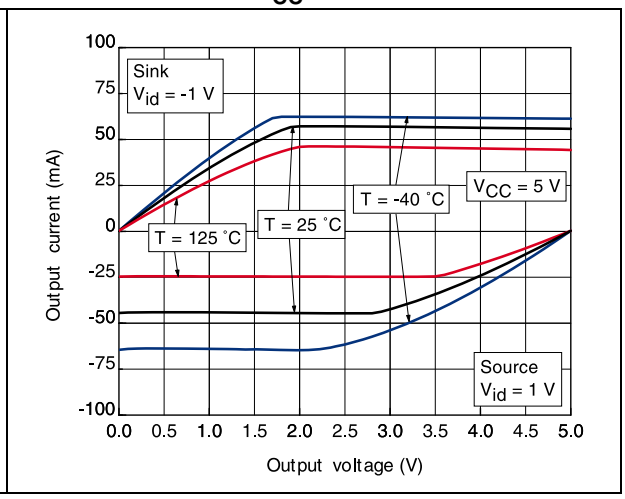


Figure 10. Output current vs. supply voltage

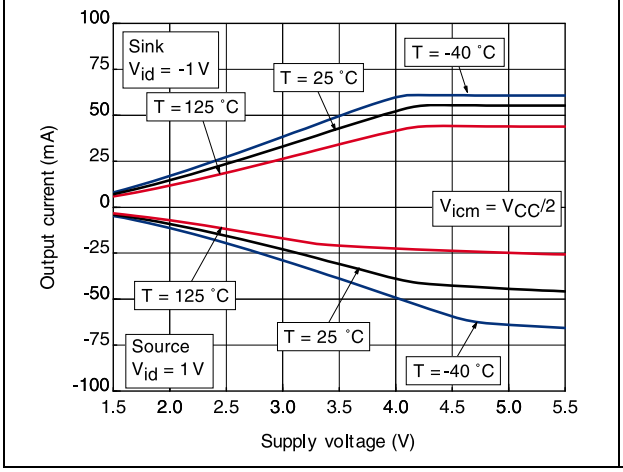


Figure 11. Bode diagram at V_{CC} = 1.5 V

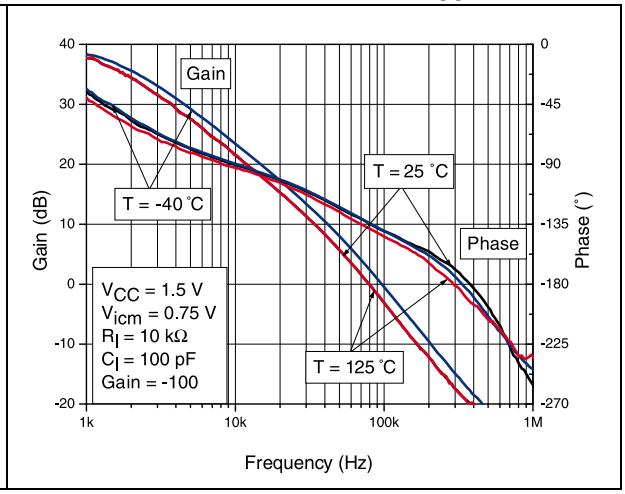


Figure 12. Bode diagram at V_{CC} = 5 V

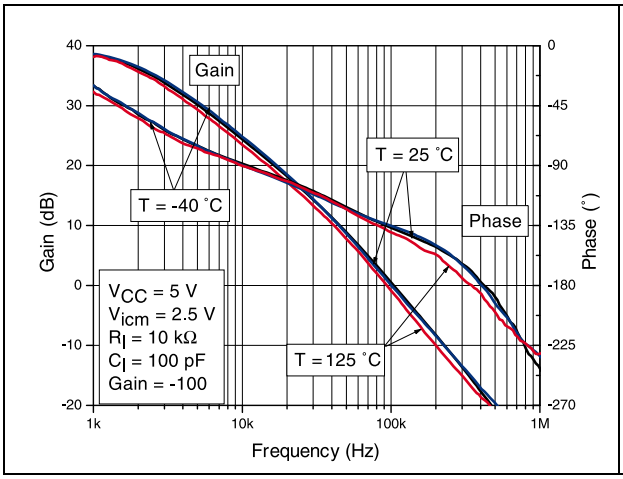


Figure 13. Closed-loop gain diagram vs. capacitive load

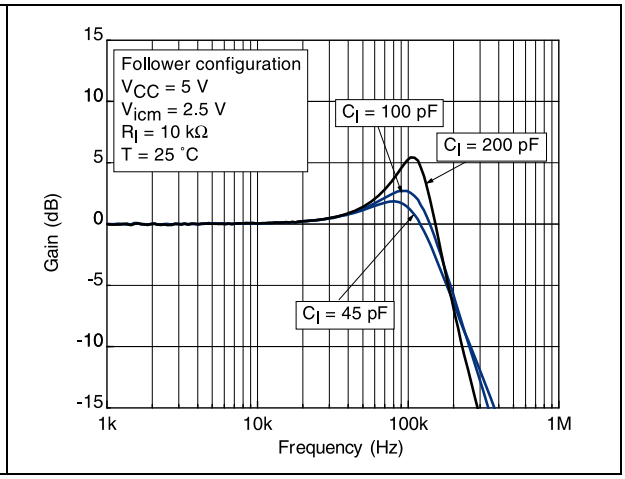


Figure 14. Positive slew rate

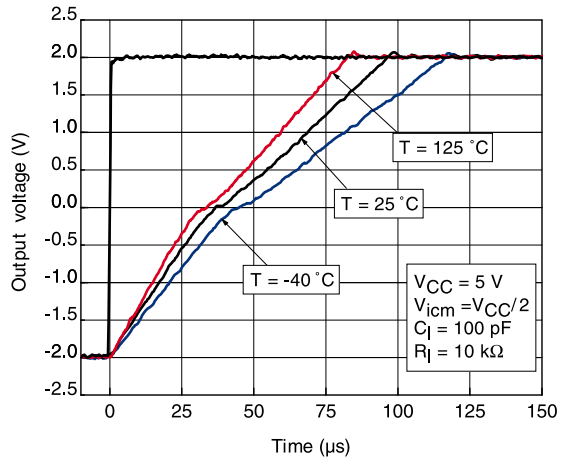


Figure 15. Negative slew rate

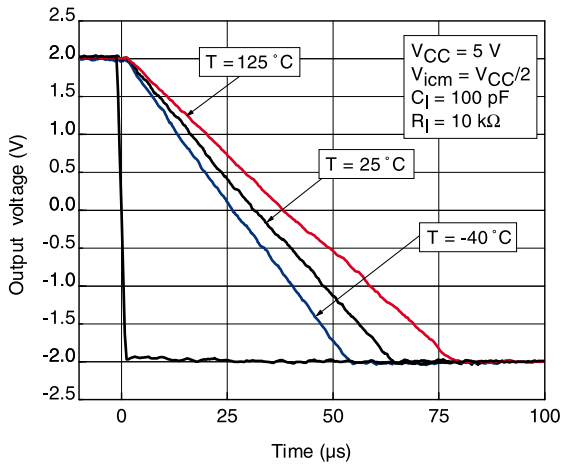


Figure 16. Slew rate vs. supply voltage

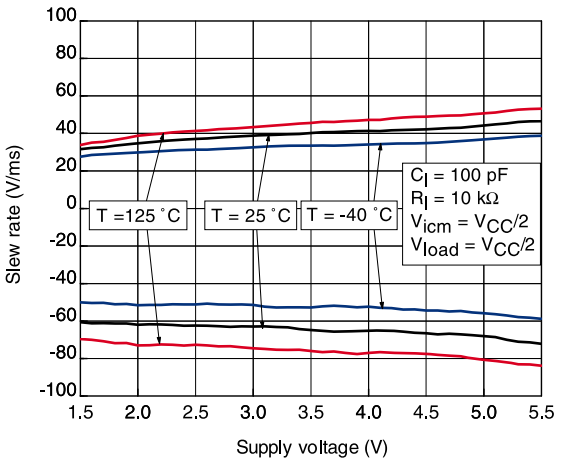


Figure 17. Noise vs. frequency

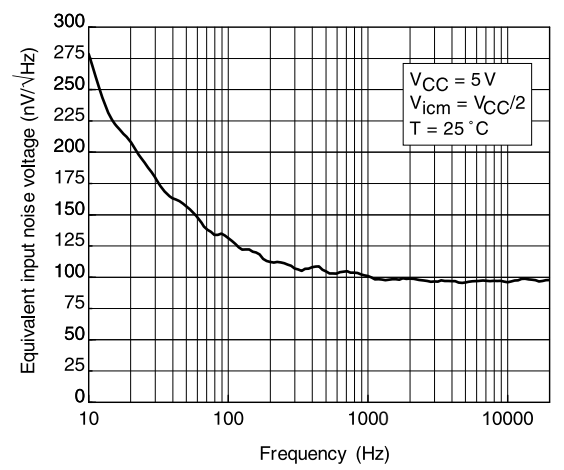


Figure 18. 0.1 Hz to 10 Hz noise

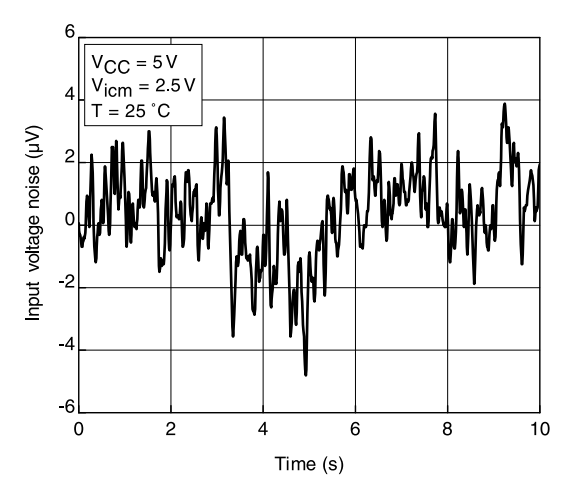


Figure 19. THD+N vs. frequency

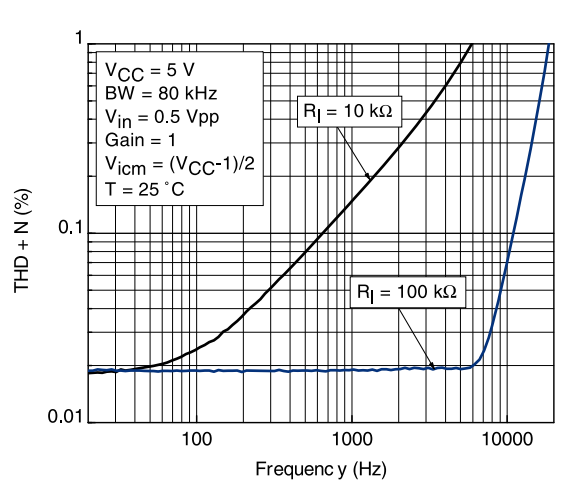


Figure 20. THD+N vs. output voltage

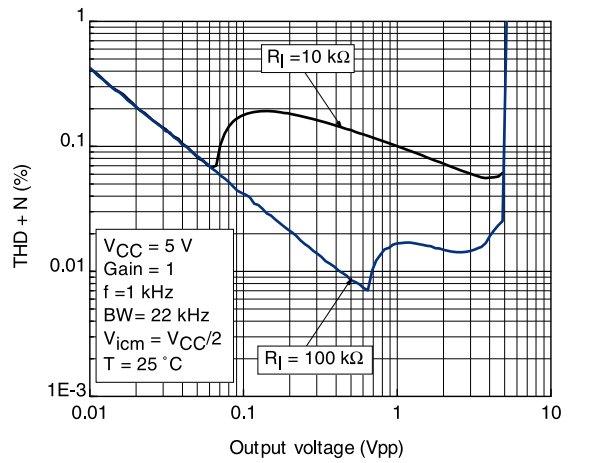
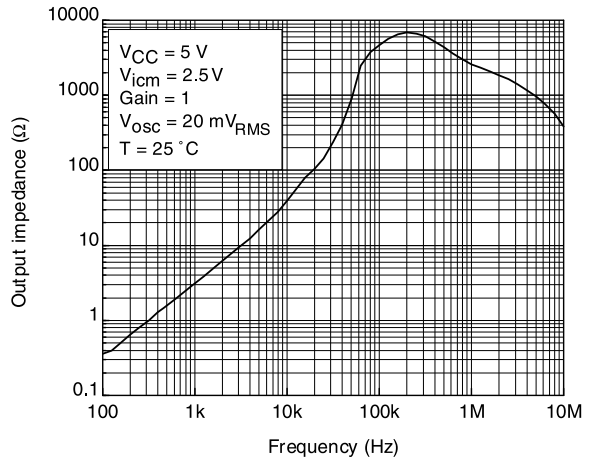


Figure 21. Output impedance vs. frequency in closed-loop configuration



4 Application information

4.1 Operating voltages

The OA1MPA, OA2MPA, and OA4MPA series of devices can operate from 1.5 V to 5.5 V. The parameters are fully specified for 1.8 V, 3.3 V, and 5 V power supplies. However, they are very stable in the full V_{CC} range and several characterization curves show OA1MPA, OA2MPA, and OA4MPA device characteristics at 1.5 V. In addition, the main specifications are guaranteed in the extended temperature range from -40 °C to +125 °C.

4.2 Rail-to-rail input

The OA1MPA, OA2MPA, and OA4MPA devices have a rail-to-rail input, and the input common mode range is extended from V_{CC-} - 0.1 V to V_{CC+} + 0.1 V.

4.3 Rail-to-rail output

The output levels of the OA1MPA, OA2MPA, and OA4MPA operational amplifiers can go close to the rails: to a maximum of 40 mV below the upper rail and to a maximum of 75 mV above the lower rail when a 10 kΩ resistive load is connected to $V_{CC}/2$.

4.4 Input offset voltage drift over temperature

The maximum input voltage drift over the temperature variation is defined as the offset variation related to offset value measured at 25 °C. The operational amplifier is one of the main circuits of the signal conditioning chain, and the amplifier input offset is a major contributor to the chain accuracy. The signal chain accuracy at 25 °C can be compensated during production at application level. The maximum input voltage drift over temperature enables the system designer to anticipate the effect of temperature variations.

The maximum input voltage drift over temperature is computed using *Equation 1*.

Equation 1

$$\frac{\Delta V_{io}}{\Delta T} = \max\left|\frac{V_{io}(T) - V_{io}(25°C)}{T - 25°C}\right|$$

with T = -40 °C and 125 °C.

The datasheet maximum value is guaranteed by a measurement on a representative sample size ensuring a C_{pk} (process capability index) greater than 1.33.

4.5 Long-term input offset voltage drift

To evaluate product reliability, two types of stress acceleration are used:

- Voltage acceleration, by changing the applied voltage
- Temperature acceleration, by changing the die temperature (below the maximum junction temperature allowed by the technology) with the ambient temperature.

The voltage acceleration has been defined based on JEDEC results, and is defined using *Equation 2*.

Equation 2

$$A_{FV} = e^{\beta \cdot (V_S - V_U)}$$

Where:

A_{FV} is the voltage acceleration factor

β is the voltage acceleration constant in 1/V, constant technology parameter ($\beta = 1$)

V_S is the stress voltage used for the accelerated test

V_U is the voltage used for the application

The temperature acceleration is driven by the Arrhenius model, and is defined in *Equation 3*.

Equation 3

$$A_{FT} = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_U} - \frac{1}{T_S}\right)}$$

Where:

A_{FT} is the temperature acceleration factor

E_a is the activation energy of the technology based on the failure rate

k is the Boltzmann constant (8.6173×10^{-5} eV.K^{-1})

T_U is the temperature of the die when V_U is used (K)

T_S is the temperature of the die under temperature stress (K)

The final acceleration factor, A_F, is the multiplication of the voltage acceleration factor and the temperature acceleration factor (*Equation 4*).

Equation 4

$$A_F = A_{FT} \times A_{FV}$$

A_F is calculated using the temperature and voltage defined in the mission profile of the product. The A_F value can then be used in *Equation 5* to calculate the number of months of use equivalent to 1000 hours of reliable stress duration.

Equation 5

$$Months = A_F \times 1000\ h \times 12\ months / (24\ h \times 365.25\ days)$$

To evaluate the op amp reliability, a follower stress condition is used where V_{CC} is defined as a function of the maximum operating voltage and the absolute maximum rating (as recommended by JEDEC rules).

The V_{io} drift (in µV) of the product after 1000 h of stress is tracked with parameters at different measurement conditions (see *Equation 6*).

Equation 6

$$V_{CC} = \max V_{op} \text{ with } V_{icm} = V_{CC}/2$$

The long term drift parameter (ΔV_{io}), estimating the reliability performance of the product, is obtained using the ratio of the V_{io} (input offset voltage value) drift over the square root of the calculated number of months (*Equation 7*).

Equation 7

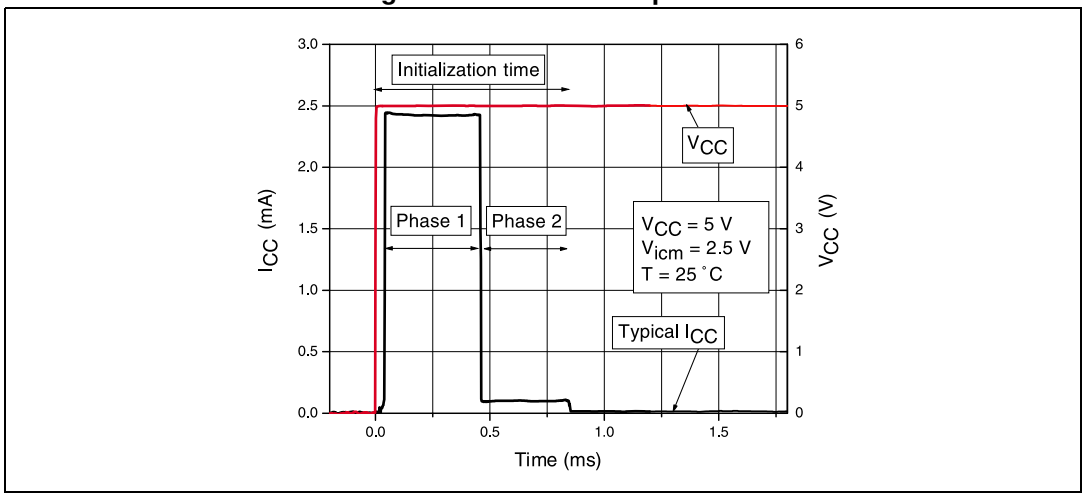
$$\Delta V_{io} = \frac{V_{io}drift}{\sqrt{(months)}}$$

where V_{io} drift is the measured drift value in the specified test conditions after 1000 h stress duration.

4.6 Initialization time

The OA1MPA, OA2MPA, and OA4MPA series of devices use a proprietary trimming topology that is initiated at each device power-up and allows excellent V_{io} performance to be achieved. The initialization time is defined as the delay after power-up which guarantees operation within specified performances. During this period, the current consumption (I_{CC}) and the input offset voltage (V_{io}) can be different to the typical ones.

Figure 22. Initialization phase



The initialization time is V_{CC} and temperature dependent. *Table 7* sums up the measurement results for different supply voltages and for temperatures varying from -40 °C to 125 °C.

Table 7. Initialization time measurement results

V_{CC} (V)	Temperature: -40 °C		Temperature: 25 °C		Temperature: 125 °C	
	T_{init} (ms)	I_{CC} phase 1 (mA)	T_{init} (ms)	I_{CC} phase 1 (mA)	T_{init} (ms)	I_{CC} phase 1 (mA)
1.8	37	0.33	3.2	0.40	0.35	0.46
3.3	2.9	1.4	0.95	1.3	0.34	1.2
5	2.4	3.2	0.85	2.4	0.31	2.9

4.7 PCB layouts

For correct operation, it is advised to add a 10 nF decoupling capacitors as close as possible to the power supply pins.

4.8 Macromodel

Accurate macromodels of the OA1MPA, OA2MPA, and OA4MPA devices are available on the STMicroelectronics' website at *www.st.com*. These model are a trade-off between accuracy and complexity (that is, time simulation) of the OA1MPA, OA2MPA, and OA4MPA op amp. They emulate the nominal performance of a typical device within the specified operating conditions mentioned in the datasheet. They also help to validate a design approach and to select the right op amp, *but they do not replace on-board measurements*.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.1 SC70-5 package information

Figure 23. SC70-5 package mechanical drawing

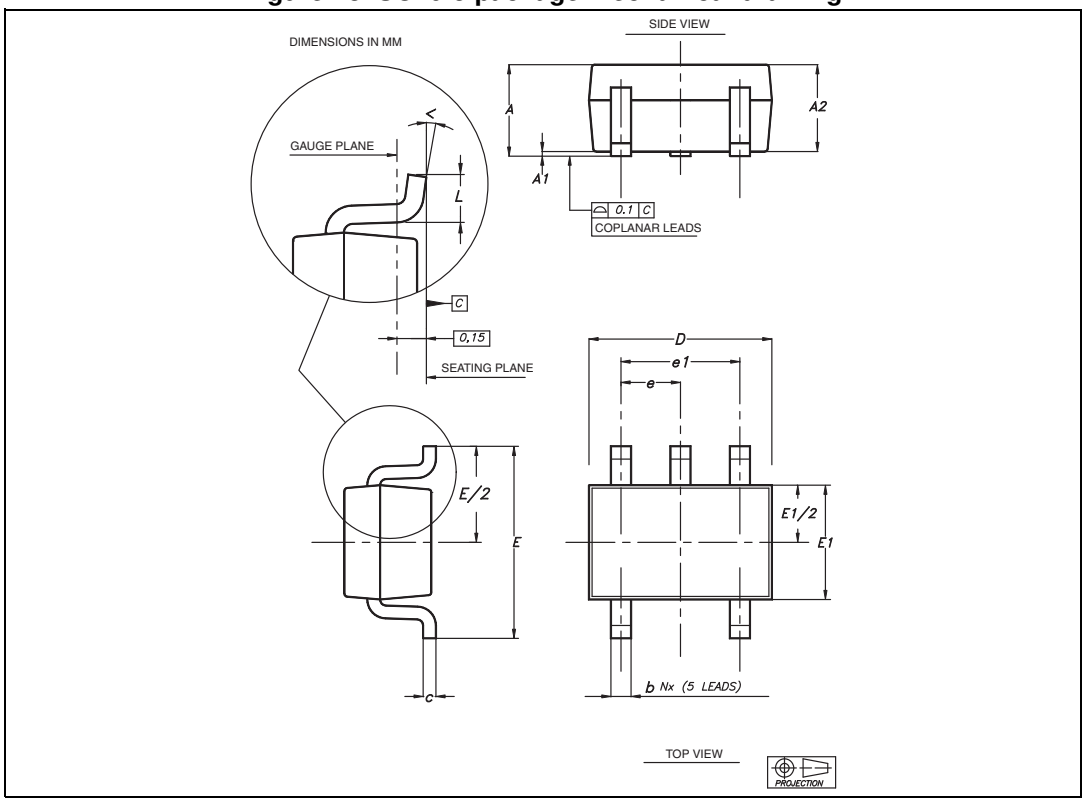


Table 8. SC70-5 package mechanical data

Symbol	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.032		0.043
A1	0		0.10			0.004
A2	0.80	0.90	1.00	0.032	0.035	0.039
b	0.15		0.30	0.006		0.012
c	0.10		0.22	0.004		0.009
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E1	1.15	1.25	1.35	0.045	0.049	0.053
e		0.65			0.025	
e1		1.30			0.051	
L	0.26	0.36	0.46	0.010	0.014	0.018
<	0°		8°	0°		8°

5.2 DFN8 2x2 package information

Figure 24. DFN8 2x2 package mechanical drawing

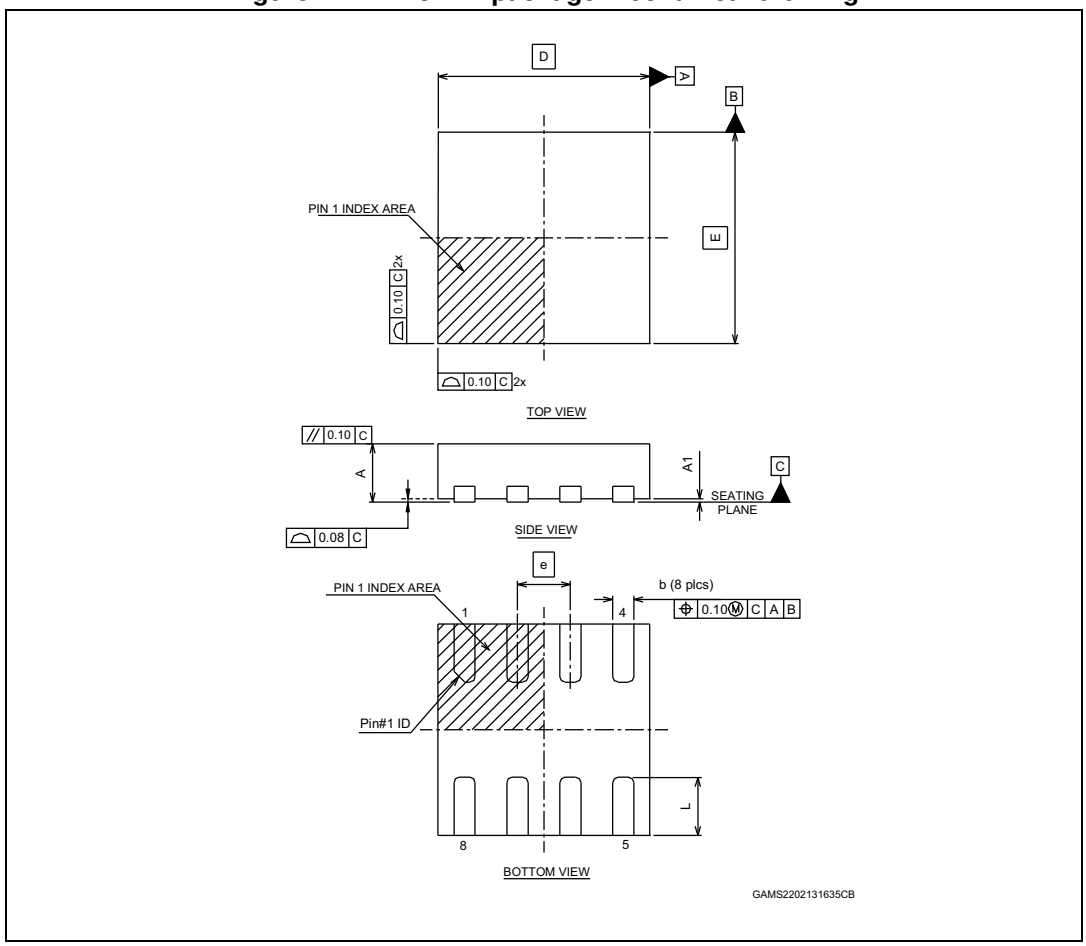


Table 9. DFN8 2x2 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D		2.00			0.079	
E		2.00			0.079	
e		0.50			0.020	
L	0.045	0.55	0.65	0.018	0.022	0.026
N	8			8		

5.3 MiniSO-8 package information

Figure 25. MiniSO-8 package mechanical drawing

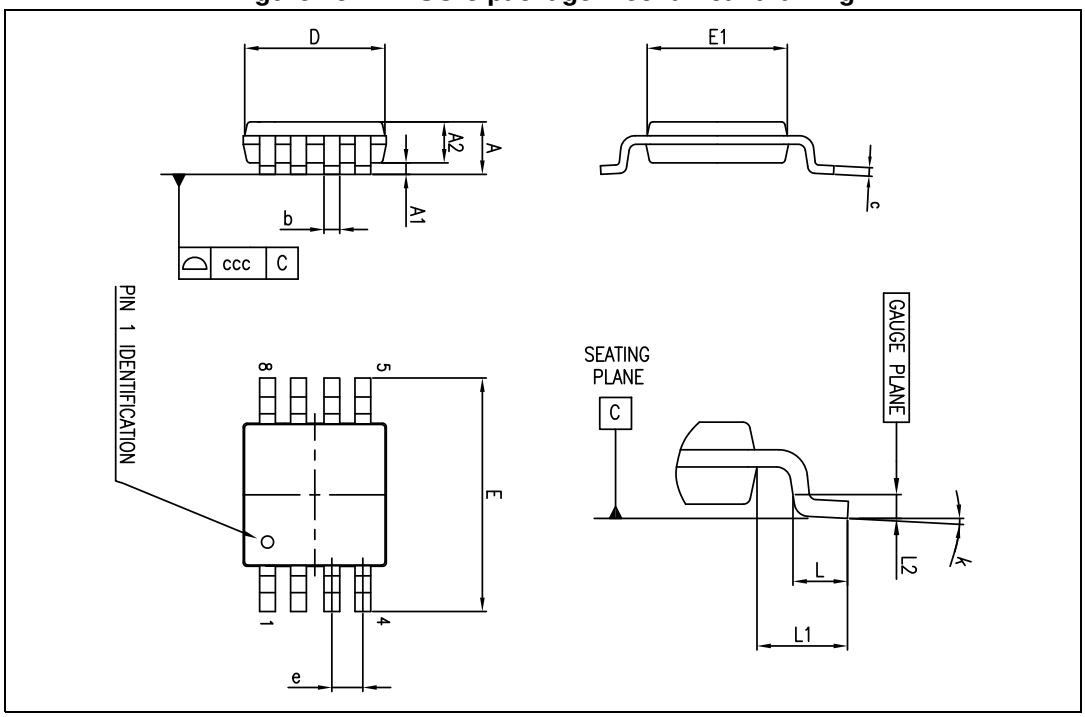


Table 10. MiniSO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0 °		8 °	0 °		8 °
ccc			0.10			0.004

5.4 QFN16 3x3 package information

Figure 26. QFN16 3x3 package mechanical drawing

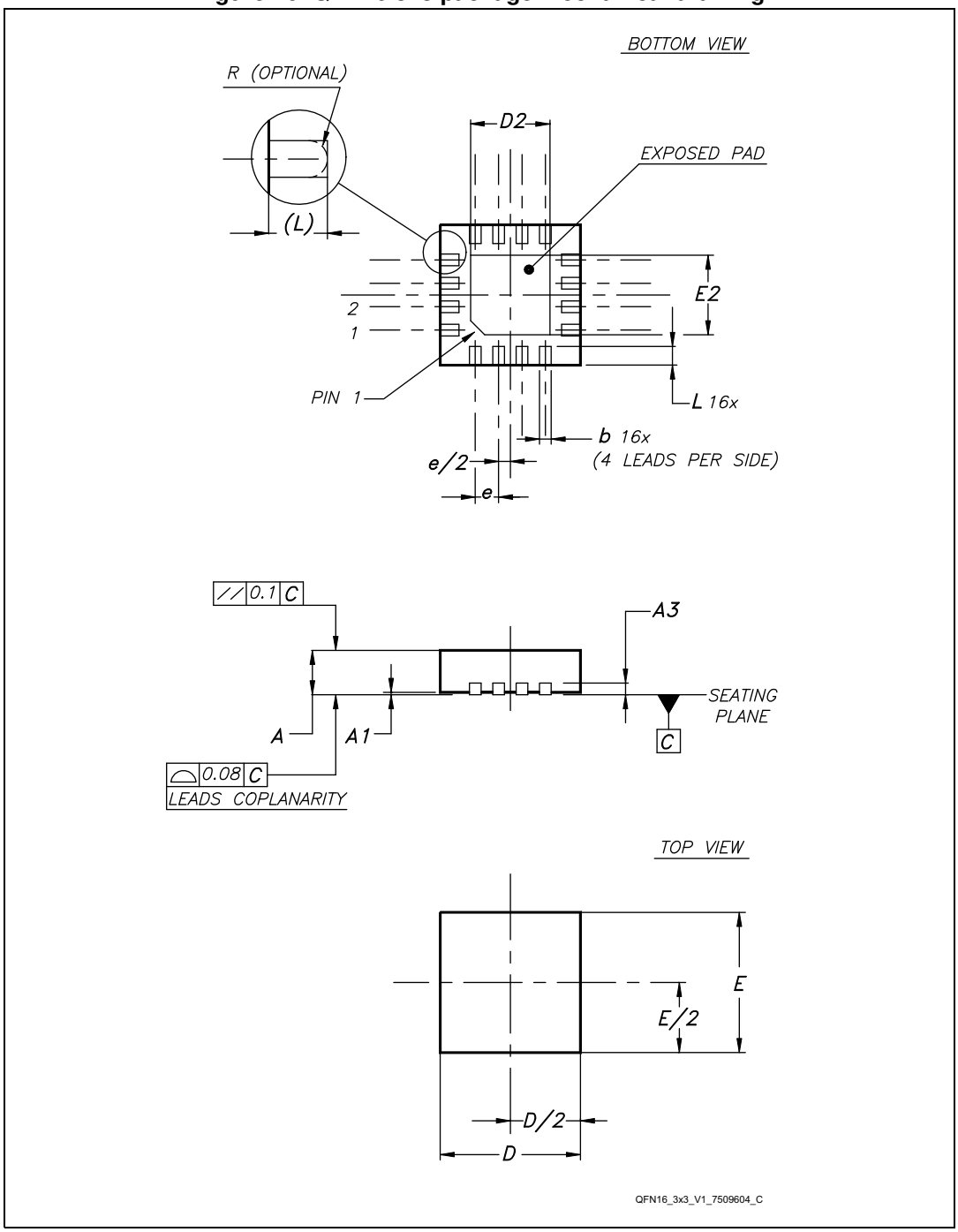
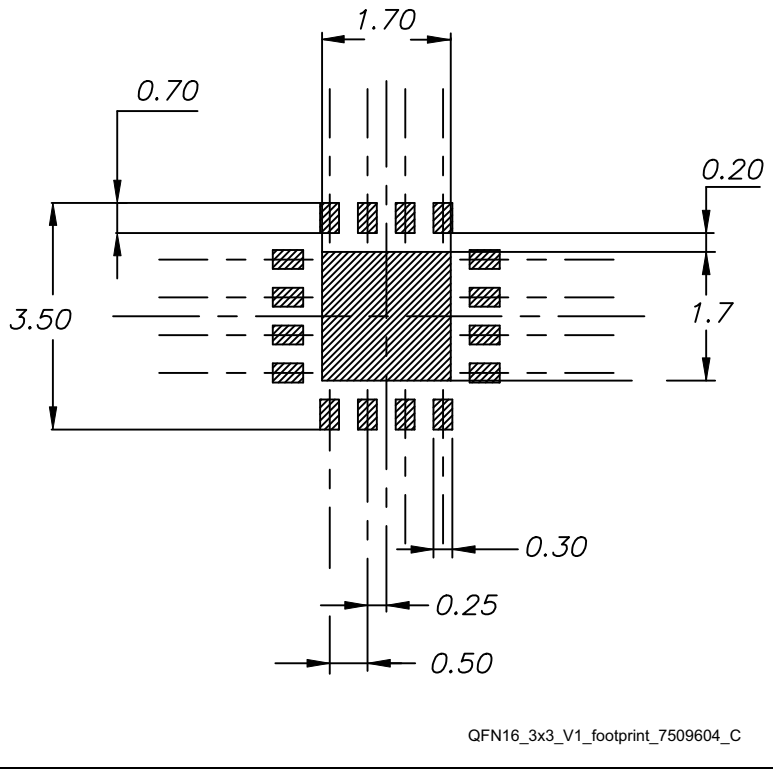


Table 11. QFN16 3x3 mm package mechanical data (pitch 0.5 mm)

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0		0.05	0		0.002
A3		0.20			0.008	
b	0.18		0.30	0.007		0.012
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	1.50		1.80	0.059		0.071
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.50		1.80	0.059		0.071
e		0.50			0.020	
L	0.30		0.50	0.012		0.020

Figure 27. QFN16 3x3 footprint recommendation



6 Revision history

Table 12. Document revision history

Date	Revision	Changes
28-Feb-2014	1	Initial release

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