SR2

6 pin Smart Reset™

Datasheet - production data



UDFN6 (1.6 x 1.3 mm)

Applications

- Wearable
- Activity tracker
- Smartwatch
- Smartglasses

Features

- Operating voltage 1.65 V to 5.5 V
- Low supply current 1.5 µA
- Integrated test mode
- Dual Smart Reset™ push-button inputs with fixed extended reset setup delay (t_{SRC}) from 0.5 s to 10 s in 0.5 s steps (typ.), option with internal pull-up resistor
- Push-button controlled reset pulse duration
  - Option 1: fully push-button controlled, no fixed or minimum pulse width guaranteed
  - Option 2: defined output reset pulse duration (t_{REC}), factory-programmed
- No power-on reset
- Single reset output
  - Active low or active high
  - Push-pull or open drain with optional pull-up resistor
- Fixed Smart Reset™ input logic voltage levels
- Operating temperature: - 40 °C to +85 °C
- UDFN6 package: 1.6 mm x 1.3 mm
- ECOPACK®2 (RoHS compliant, Halogen-Free)

This is information on a product in full production. www.st.com

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1 Description

The Smart Reset™ devices provide a useful feature that ensures inadvertent short reset push-button closures do not cause system resets. This is done by implementing extended Smart Reset™ input delay time (t_{SRC}) and combined push-button inputs, which together ensures a safe reset and eliminates the need for a specific dedicated reset button.

This reset configuration provides versatility and allows the application to distinguish between a software generated interrupt and a hard system reset. When the input push-button are connected to microcontroller interrupt inputs, and are closed for a short time, the processor can only be interrupted. If the system still does not respond properly, continuing to keep the push-button closed for the extended setup time t_{SRC} causes a hard reset of the processor through the reset output.

The SR2 has two combined delayed Smart Reset™ inputs ($\overline{SR0}$, $\overline{SR1}$) with preset delayed Smart Reset™ setup time (t_{SRC}). The reset output is asserted after both of the Smart Reset™ inputs were held active for the selected t_{SRC} delay time. Depending on selected option the $\overline{RST}$ output remains asserted either until at least one $\overline{SR}$ input goes to inactive logic level (i.e. neither fixed nor minimum reset pulse width is set) or the output reset pulse duration is fixed for t_{REC} (i.e. factory-programmed). The reset output, $\overline{RST}$, is active low or active high, push-pull or open drain with optional pull-up resistor. The device fully operates over a broad V_{CC} range 1.65 V to 5.5 V. Below 1.575 V typ. the inputs are ignored and outputs are deasserted; the deasserted reset output levels are then valid down to 1.0 V.

1.1 Test mode

After pull of $\overline{SR0}$ up to V_{TEST} or more (V_{CC} + 1.4 V, max.) we start counting initial shorten $t_{SRC-INI}$ (42 ms, typ.). After $t_{SRC-INI}$ expires, the $\overline{RST}$ output either goes down for t_{REC} (if t_{REC} option is used) or stays low as long as overvoltage on $\overline{SR0}$ in detected (if t_{REC} option is not used). This is a feedback and a user knows that the device is locked in the test mode. Each time both $\overline{SR}$ inputs are connected to ground in test mode a shorten $t_{SRC-SHORT}$ (21 ms, typ.) is used instead of long t_{SRC} (0.5 s -10 s). Return from to normal mode is possible by a new startup of the device (i.e. V_{CC} goes to 0 V and back to its original state). In this way the device can be quickly tested without repeating test mode triggering. Advantage of this solution is pretty high glitch immunity, feedback to user about entry to the test mode and testability within full V_{CC} range.

Figure 1. Logic diagram

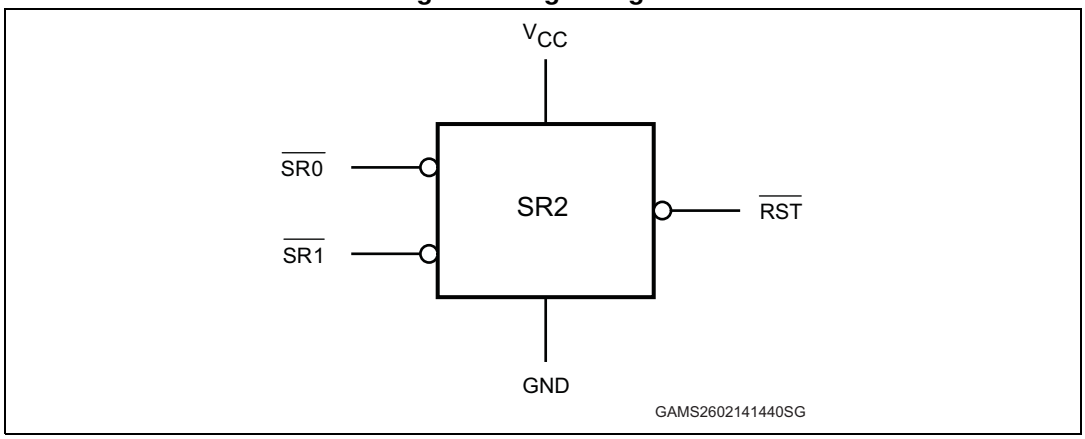


Figure 2. Pin connections (top view)

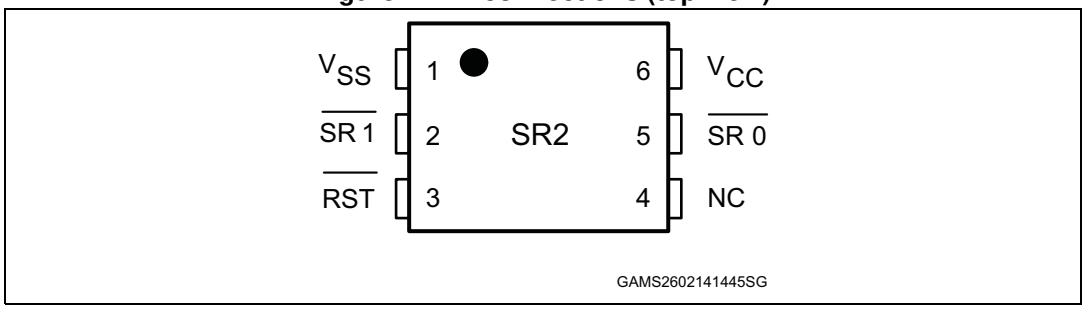
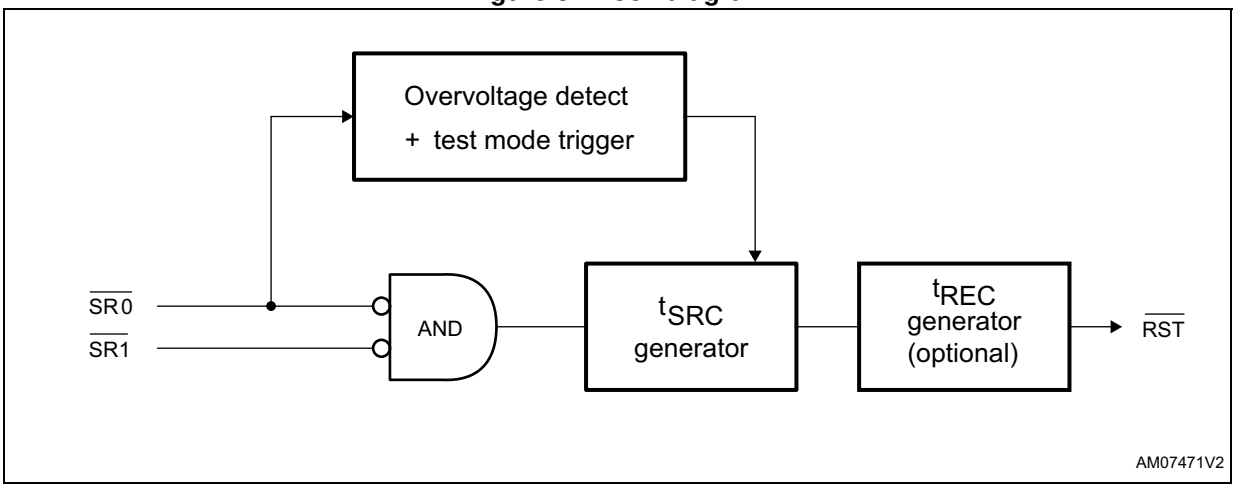


Table 1. Signal names

Pin	Name	Type	Description
1	V_{SS}	Supply ground	Ground
2	$\overline{SR1}$	Input	Secondary push-button Smart Reset™ input. Active low. Optional pull-up resistor
3	$\overline{RST}$	Output	Reset output (open drain with optional pull-up resistor, active low) (push-pull – active low or active high)
4	NC	-	Not connected (not bonded; should be connected to V_{SS})
5	$\overline{SR0}$	Input	Primary push-button Smart Reset™ input. Active low. Optional pull-up resistor
6	V_{CC}	Supply voltage	Positive supply voltage for the device. A 0.1 µF decoupling ceramic capacitor is recommended to be connected between V_{CC} and V_{SS} pins, as close to the SR2 device as possible

Figure 3. Block diagram



2 Pin descriptions

2.1 Power supply (V_{CC})

This pin is used to provide power to the Smart Reset™ device. A 0.1 µF ceramic decoupling capacitor is recommended to be connected between the V_{CC} and V_{SS} pins, as close to the SR2 device as possible.

2.2 Ground (V_{SS})

Ground pin for the device.

2.3 Smart Reset™ input ($\overline{SR0}$)

Push-button Smart Reset™ input is active low with optional pull-up resistor. Both $\overline{SR}$ inputs need to be asserted simultaneously for at least t_{SRC} to assert the reset output ($\overline{RST}$). By connecting a voltage higher than V_{CC} to the $\overline{SR0}$ the device enters a test mode (see *Section 1: Description on page 3* for more information).

2.4 Smart Reset™ input ($\overline{SR1}$)

Push-button Smart Reset™ input is active low with optional pull-up resistor. Both $\overline{SR}$ inputs need to be asserted simultaneously for at least t_{SRC} to assert the reset output ($\overline{RST}$).

2.5 Reset output ($\overline{RST}$)

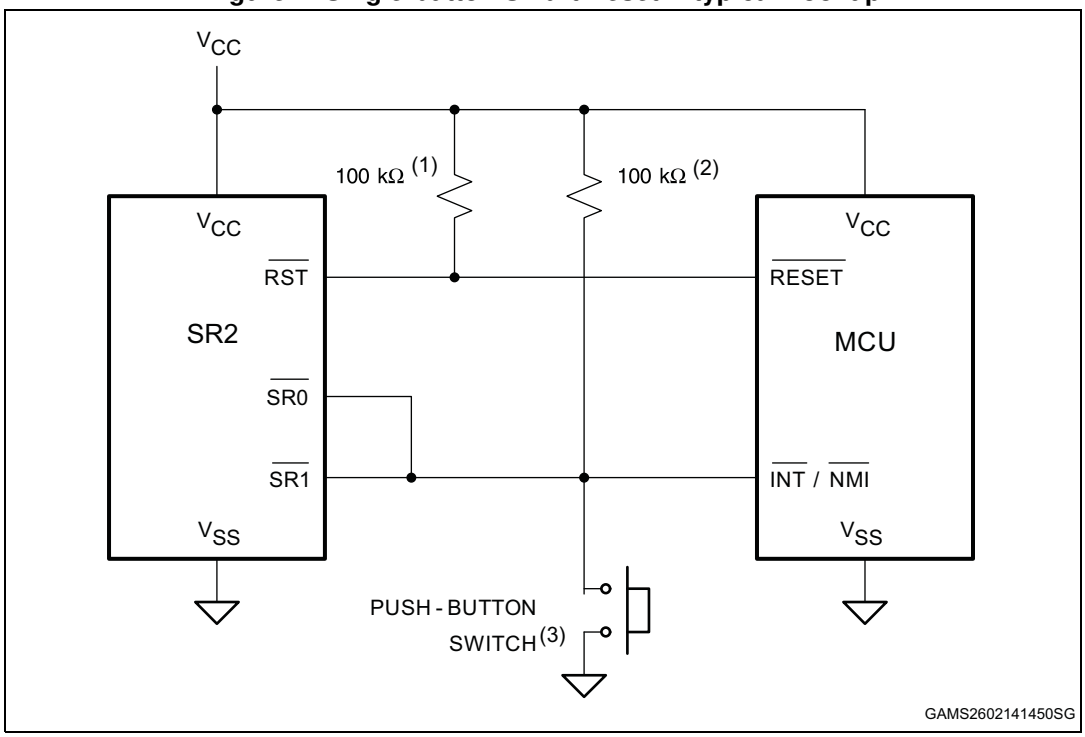
$\overline{RST}$ is active low or active high, push-pull or open drain reset output with optional internal pull-up resistor. Output reset pulse width is optional as follows:

- Neither fixed nor minimum output reset pulse duration (releasing the push-button while reset output is active, causes the output to deassert);
- Fixed, factory-programmed output reset pulse duration for t_{REC} independent on Smart Reset™ input state.

If V_{CC} drops below 1.575 V, the $\overline{RST}$ output is deasserted and its state is guaranteed down to 1 V (see *Figure 8*).

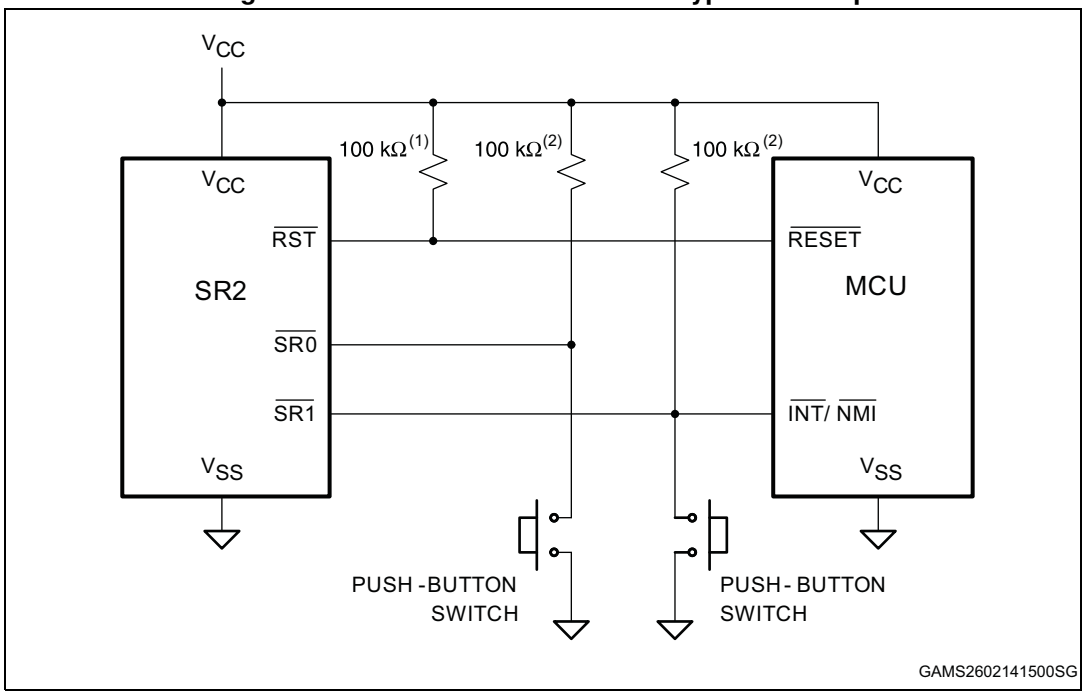
3 Typical application diagram

Figure 4. Single-button Smart Reset™ typical hookup



1. External pull-up resistor requested if the reset output ($\overline{RST}$) is open drain type without internal pull-up.
2. External pull-up resistor requested if the Smart Reset™ inputs ($\overline{SR0}$ and $\overline{SR1}$) have no internal pull-up.
3. When only one Smart Reset™ input push-button is used, tie both the $\overline{SR}$ inputs together.

Figure 5. Dual-button Smart Reset™ typical hookup



1. External pull-up resistor requested if the reset output ($\overline{RST}$) is open drain type without internal pull-up.
2. External pull-up resistor requested if the Smart Reset™ inputs ($\overline{SR0}$ and $\overline{SR1}$) have no internal pull-up.

4 Timing waveforms

Figure 6. Option without t_{REC}

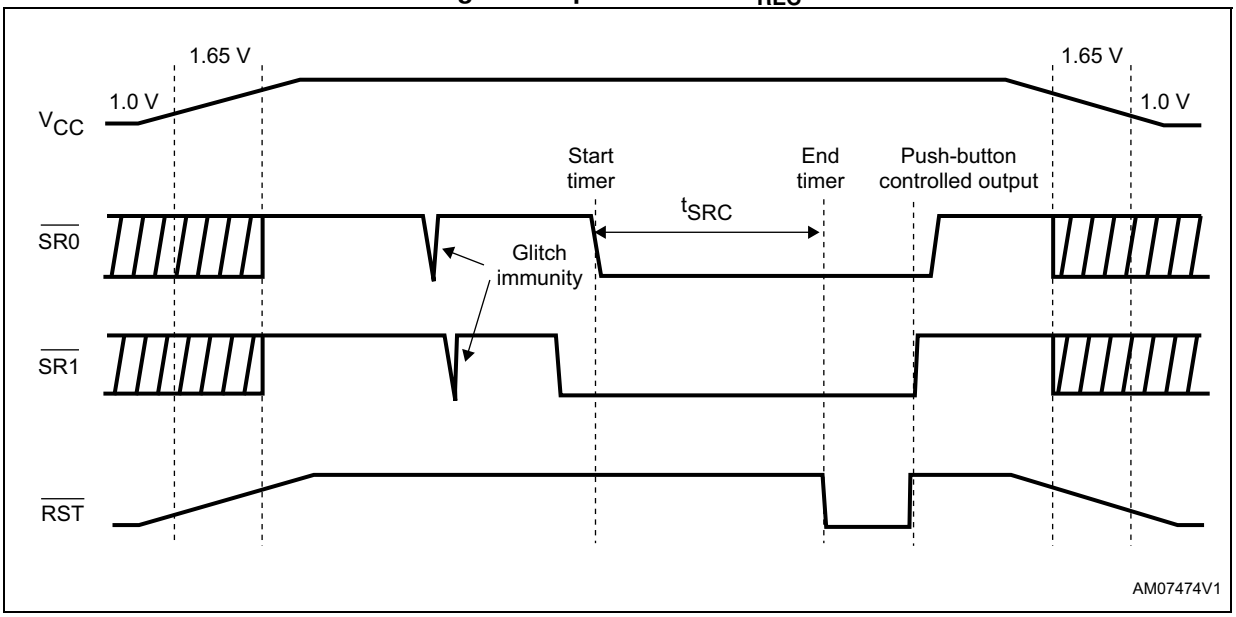


Figure 7. Option with t_{REC}

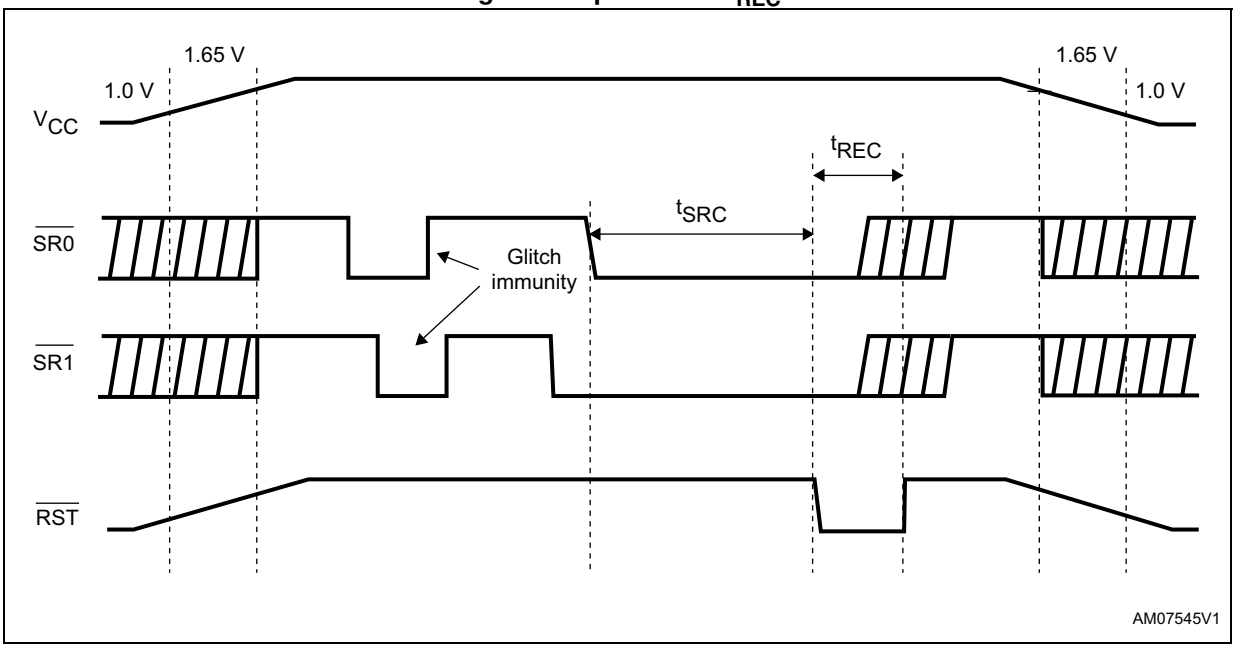
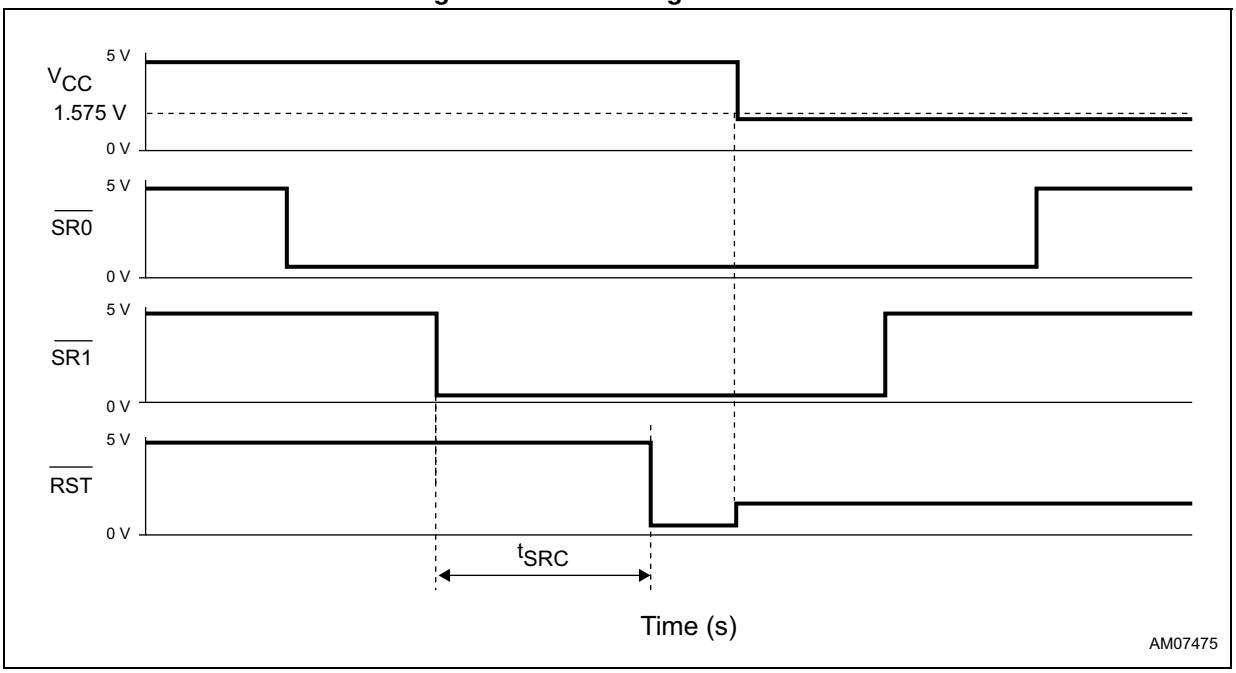


Figure 8. Undervoltage condition



1. If undervoltage occurs (V_{CC} drops below 1.575 V typ.) while reset output is active, the reset output is released and goes inactive.

5 Typical operating characteristics

Figure 9. Supply current (I_{CC}) vs. temperature (T_A)

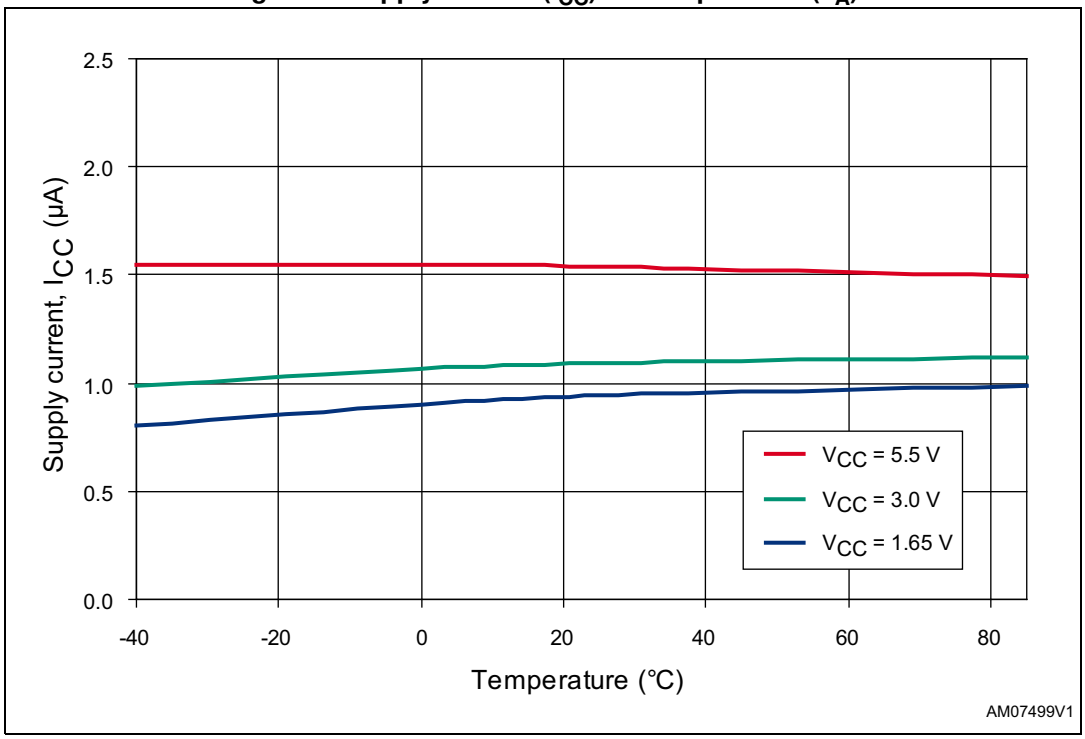


Figure 10. Smart Reset™ delay (t_{SRC}) vs. temperature (T_A), t_{SRC} = 7.5 s (typ.)

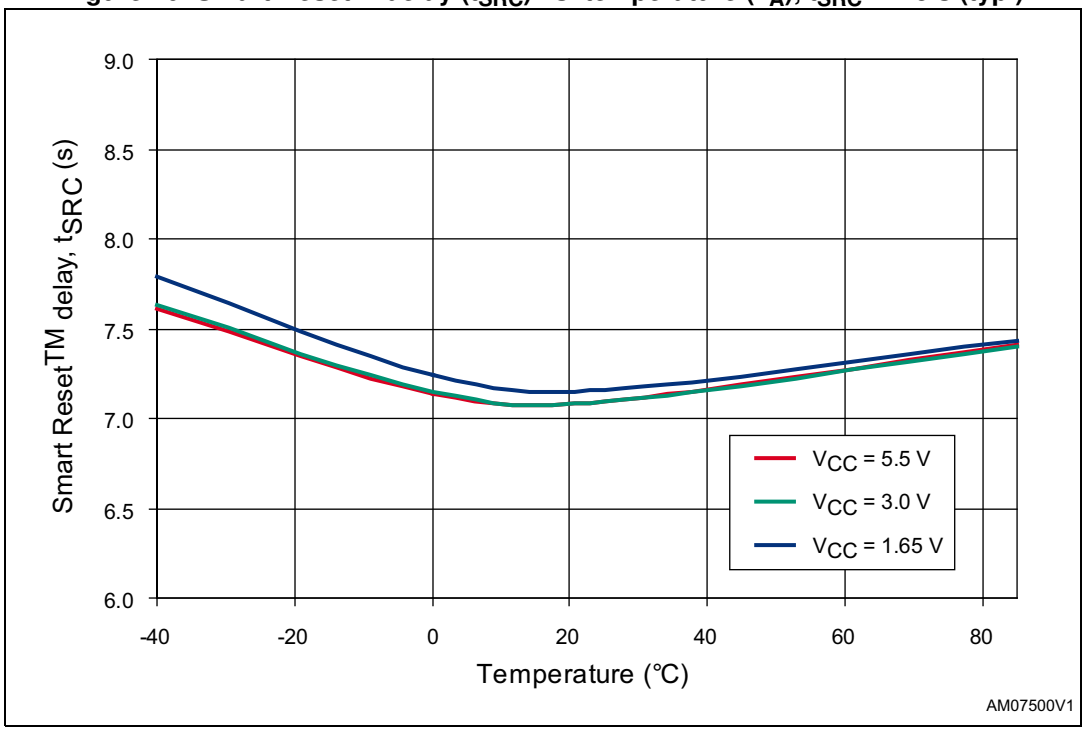


Figure 11. Test mode entry voltage (V_{TEST}) vs. temperature (T_A)

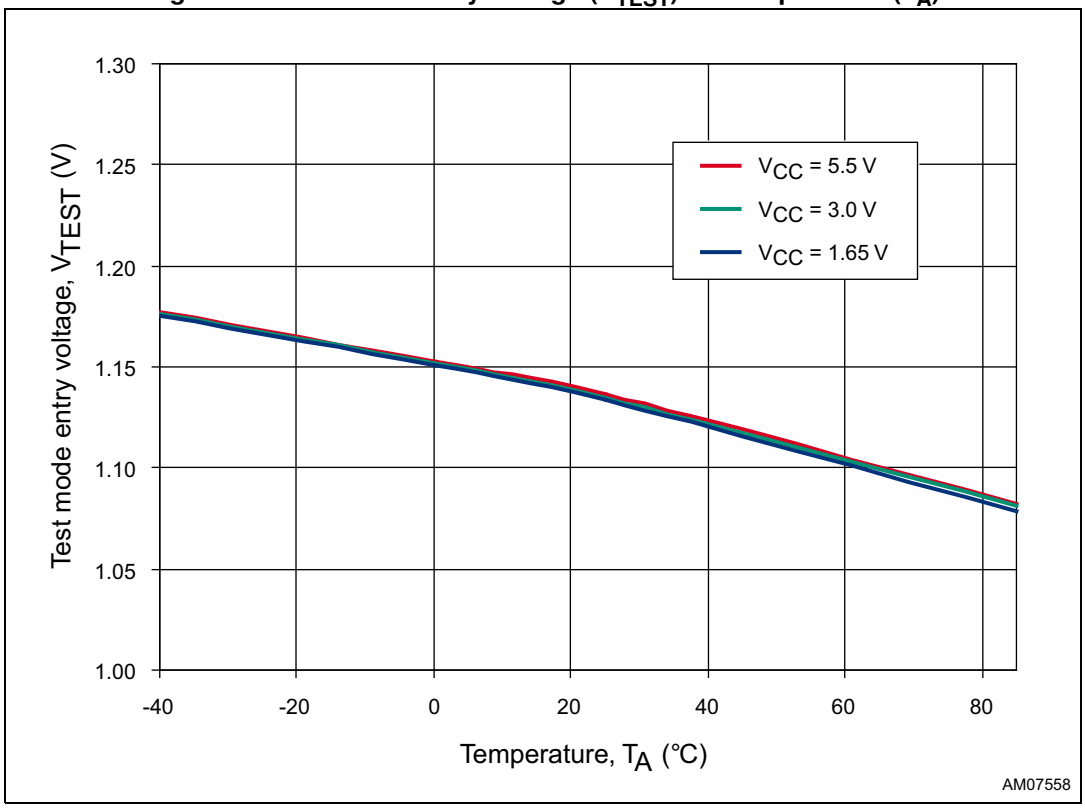
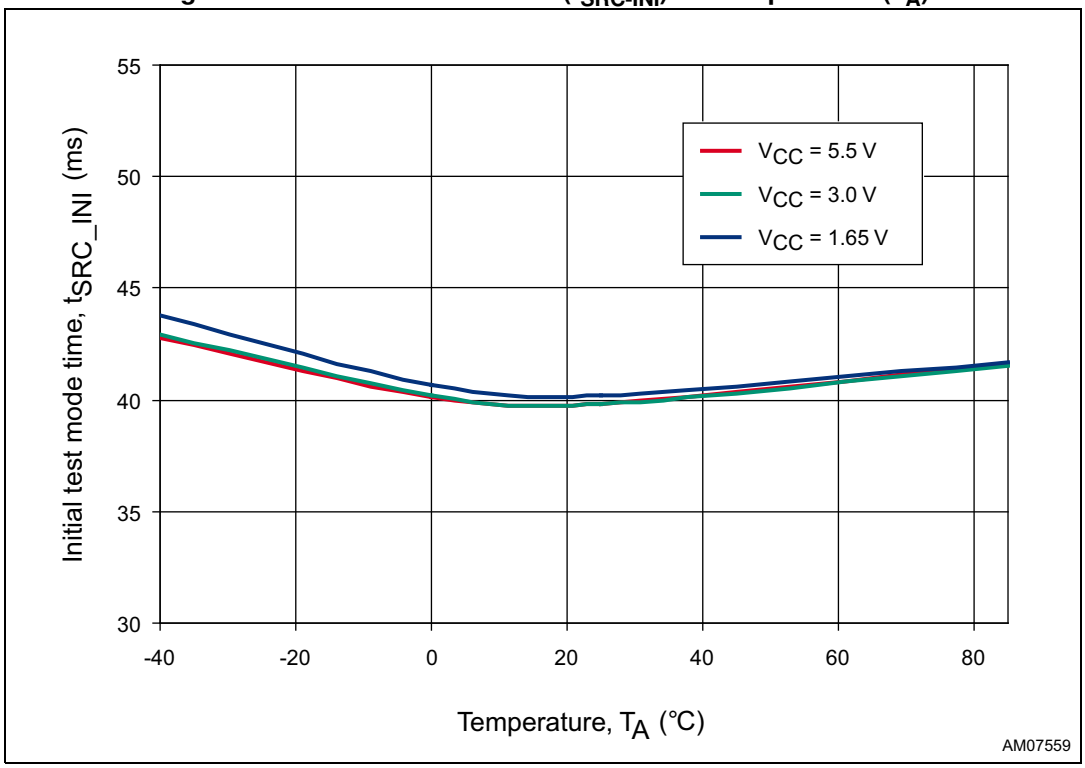


Figure 12. Initial test mode time ($t_{SRC-INI}$) vs. temperature (T_A)



6 Maximum ratings

Stressing the device above the rating listed in *Table 2: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Table 3: Operating and measurement conditions* of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics™ SURE program and other relevant quality documents.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature (V_{CC} off)	-55 to +150	°C
T_{SLD}(1)	Lead solder temperature for 10 seconds	260	°C
V_{IO}	Input or output voltage	-0.3 to 5.5(2)	V
V_{CC}	Supply voltage	-0.3 to 7	V
ESD			
V_{HBM}	Electrostatic discharge protection, human body model (JESD22-A114-B level 2)	2	kV
V_{RCDM}	Electrostatic discharge protection, charged device model, all pins	1	kV
V_{MM}	Electrostatic discharge protection, machine model, all pins (JESD22-A115-A level A)	200	V
	Latch-up (V_{CC} pin, $\overline{SR0}$ reset input pin)	EIA/JESD78	-

1. Reflow at peak temperature of 260 °C. The time above 255 °C must not exceed 30 seconds.
2. For push-pull $\overline{RST}$ output type only from -0.3 V to V_{CC} +0.3 V.

7 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in *Table 4: DC and AC characteristic* that follow, are derived from tests performed under the measurement conditions summarized in *Table 3: Operating and measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 3. Operating and measurement conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	1.65 to 5.5	V
T_A	Ambient operating temperature	-40 to +85	°C

Table 4. DC and AC characteristic

Symbol	Parameter	Test conditions[1]	Min.	Typ.[2]	Max.	Unit
V_{CC}	Supply voltage[3]		1.65		5.5	V
I_{CC}	Supply current (inputs in their inactive state, t_{SRC} counter is not running)	V_{CC} = 3.0 V		1.1	2.5	µA
		V_{CC} = 5.0 V		1.5	3.0	µA
V_{OL}	Reset output voltage low	$V_{CC} \geq$ 4.5 V, sinking 3.2 mA			0.3	V
		$V_{CC} \geq$ 3.3 V, sinking 2.5 mA			0.3	V
		$V_{CC} \geq$ 1.65 V, sinking 1 mA			0.3	V
V_{OH}	Reset output voltage high (push-pull output only)	$V_{CC} \geq$ 4.5 V, I_{SOURCE} = 0.8 mA	0.8 V_{CC}			V
		$V_{CC} \geq$ 2.7 V, I_{SOURCE} = 0.5 mA	0.8 V_{CC}			V
		$V_{CC} \geq$ 1.65 V, I_{SOURCE} = 0.25 mA	0.8 V_{CC}			V
t_{REC}	Reset timeout delay, factory-programmed	(device option)	240	360	480	ms
R_{PUO}	Internal output pull-up resistor on $\overline{RST}$	(device option)		65		kΩ
I_{LO}	Output leakage current	$V_{\overline{RST}}$ = 5.5 V, open drain device option without output pull-up resistor	-0.1		0.1	µA
Smart Reset™						
t_{SRC}	Smart Reset™ delay	T_A = -40 to +85 °C	0.8 x t_{SRC}	t_{SRC}[4]	1.2 x t_{SRC}	s
		T_A = 25 °C	0.9 x t_{SRC}		1.1 x t_{SRC}	
V_{IL}	$\overline{SR0}$, $\overline{SR1}$ input voltage low		V_{SS} -0.3		0.3	V
V_{IH}	$\overline{SR0}$, $\overline{SR1}$ input voltage high		0.85		5.5	V
I_{LI}	$\overline{SR0}$, $\overline{SR1}$ input leakage current		-0.1		0.1	µA
	Input glitch immunity[5]	$\overline{SR0}$ and $\overline{SR1}$ asserted		t_{SRC}		s
Test mode						
V_{TEST}	Test mode entry voltage		V_{CC} +0.9	V_{CC} +1.1	V_{CC} +1.4	V
$t_{SRC-INI}$	Initial test mode time		28	42	56	ms
$t_{SRC-SHORT}$	Shorten Smart Reset™ delay		16.8	21	25.2	ms

1. Valid for ambient operating temperature T_A = -40 to +85 °C, V_{CC} = 1.65 to 5.5 V.
2. Typical values are at 25 °C and V_{CC} = 3.3 V unless otherwise noted.
3. Reset outputs are deasserted below 1.575 V typ. and remain deasserted down to V_{CC} = 1 V.
4. Factory-programmable in the range of 0.5 s to 10 s typ. in 0.5 s steps (see *Table 7* for available delays).
5. Input glitch immunity is equal to t_{SRC}, when both inputs ($\overline{SR0}$ and $\overline{SR1}$) are low. Otherwise infinite.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 13. Package outline for UDFN6 1.6 x 1.3 x 0.55 mm, 0.40 mm pitch

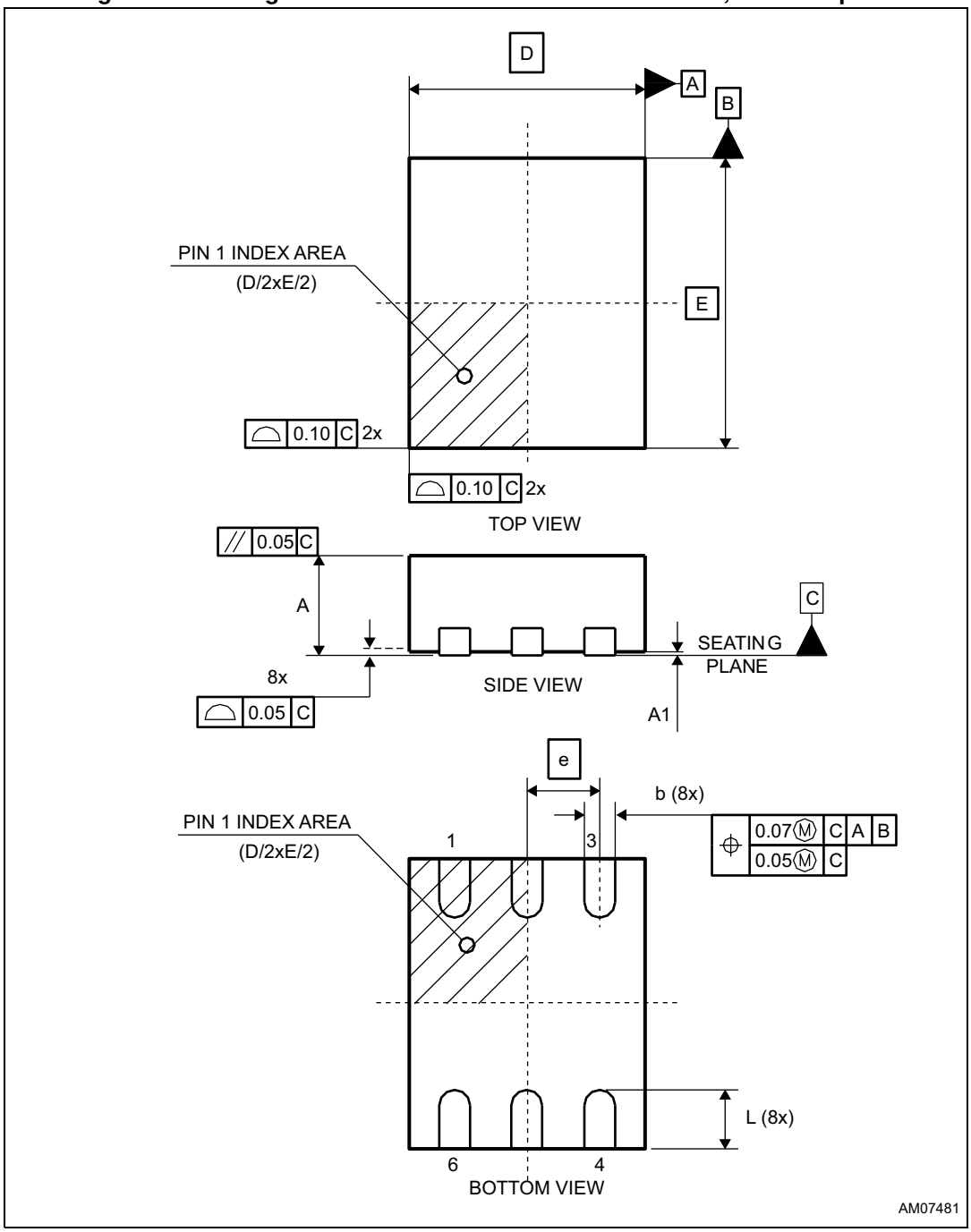


Table 5. Mechanical data for UDFN6 1.6 x 1.3 x 0.55 mm, 0.40 mm pitch

Symbol	Dimensions						Note
	Drawing (millimeters)			Drawing (inches)			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
A	0.50	0.55	0.60	0.020	0.022	0.024	
A1	0.00	0.02	0.05	0.0000	0.0008	0.0020	
b	0.15	0.20	0.25	0.006	0.008	0.010	
D	1.30 BSC			0.051 BSC			
E	1.60 BSC			0.063 BSC			
e	0.40 BSC			0.016 BSC			
L	0.250	0.325	0.400	0.0098	0.0128	0.0157	
N	6			6			

Figure 14. Footprint recommendation for UDFN6 1.6 x 1.3 x 0.55 mm, 0.40 mm pitch

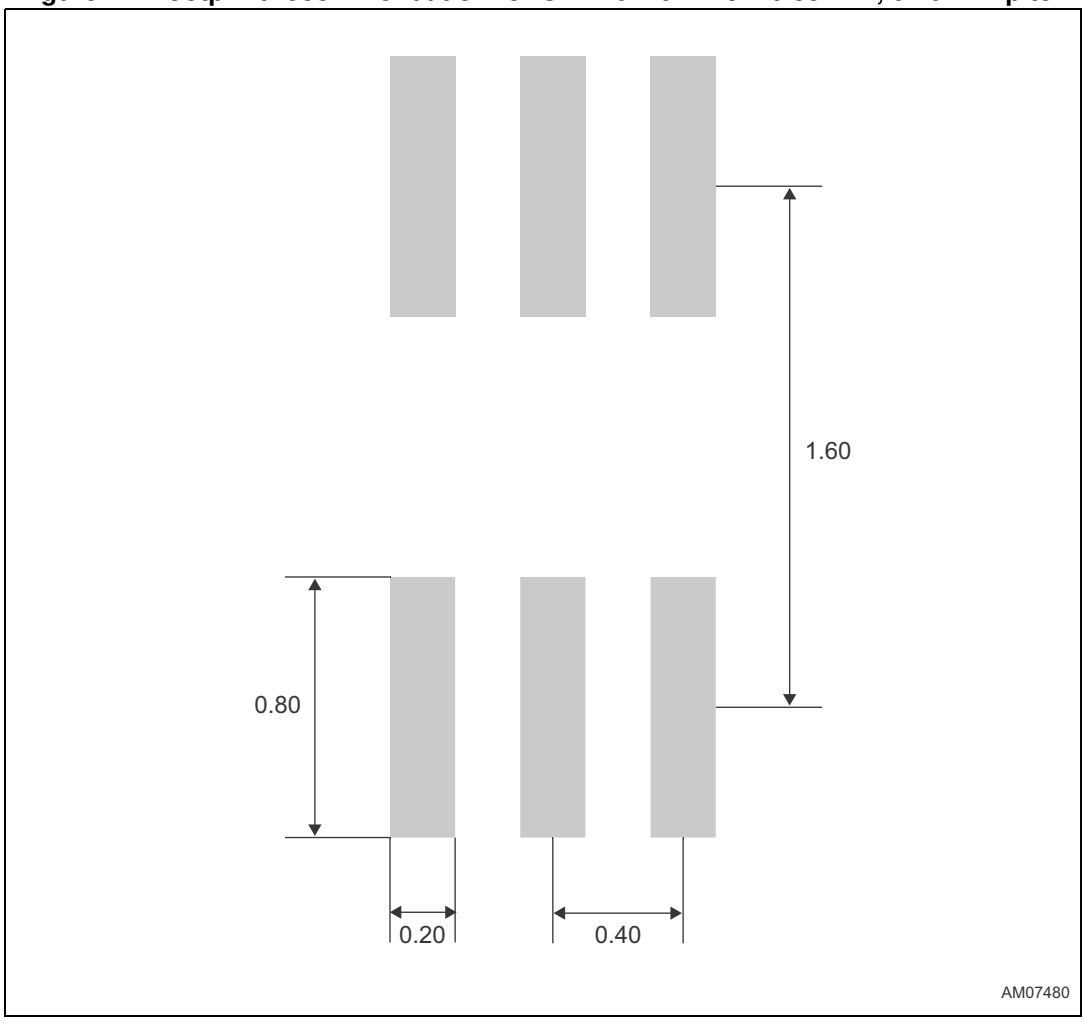
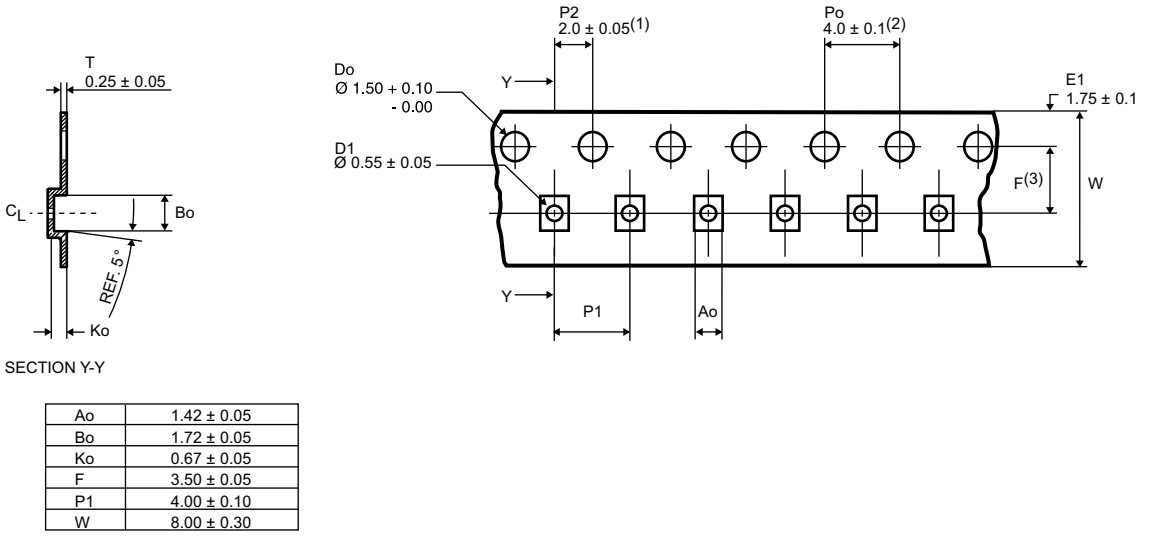


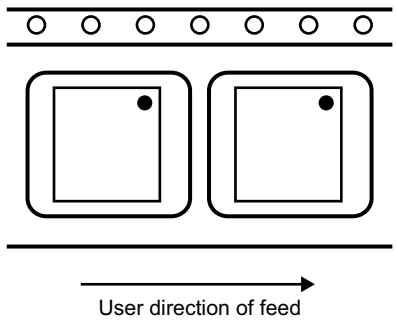
Figure 15. Carrier tape for UDFN6 1.6 x 1.3 x 0.55 mm



Ao	1.42 ± 0.05
Bo	1.72 ± 0.05
Ko	0.67 ± 0.05
F	3.50 ± 0.05
P1	4.00 ± 0.10
W	8.00 ± 0.30

1. Measured from centreline of sprocket hole to centreline of pocket.
2. Cumulative tolerance of 10 sprocket holes is ± 0.20.
3. Measured from centreline of sprocket hole to centreline of pocket.
4. Other material available.
5. Typical SR of formed tape max. 10^9 Ω/SQ.
6. All dimensions in millimeters unless otherwise stated.

Figure 16. Pin 1 orientation



9 Part numbering

Table 6. Ordering information scheme

Example: SR2 H A R U

Device type

SR2

Smart Reset™ set up delay (t_{SRC})(1)

H = factory programmable t_{SRC} = 4.0 s, no pull-up
L = factory programmable t_{SRC} = 6.0 s, no pull-up
P = factory programmable t_{SRC} = 7.5 s, no pull-up
U = factory programmable t_{SRC} = 10.0 s, no pull-up

Outputs type

A = open drain, no pull-up, active low

Reset timeout period (t_{REC})

B = factory programmable t_{REC} = 360 ms (typ.)
R = push-button controlled

Package

DL = UDFN6

1. Smart Reset™ delay (t_{SRC}) is available from 0.5 s to 10 s in 0.5 s steps (typ.). Minimum order quantities may apply. Contact local sales office for availability.

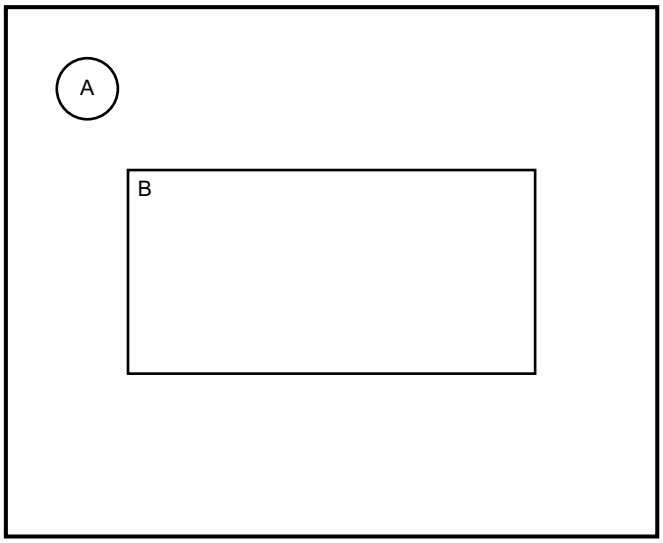
10 Package marking information

Table 7. Package marking

Part number	t_{SRC} (s)	Smart Reset™ inputs(1)	Output type(2)	t_{REC} option (ms)(3)	Package	Topmark
SR2HARU	4.0	AL	OD, AL	No t_{REC}	UDFN6	HA
SR2LABU	6.0	AL	OD, AL	360	UDFN6	LC
SR2LARU	6.0	AL	OD, AL	No t_{REC}	UDFN6	LA
SR2PARU	7.5	AL	OD, AL	No t_{REC}	UDFN6	PA
SR2UABU	10.0	AL	OD, AL	360	UDFN6	UC
SR2UARU	10.0	AL	OD, AL	No t_{REC}	UDFN6	UA

1. AL = active low.
2. OD = open drain, AL = active low.
3. No t_{REC} = push-button controlled reset pulse width.

Figure 17. Package marking (top view)



A = dot (pin 1 reference)
B = marking area (topmark)

AM07546

11 Revision history

Table 8. Document revision history

Date	Revision	Changes
10-Mar-2014	1	Initial release
13-May-2014	2	Modified: t_{REC} values *Table 4 on page 15* Updated: *Table 6 on page 19*

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