TSX3702

Datasheet

Micropower dual CMOS voltage comparators



D
SO8
(plastic micropackage)



P
TSSOP8
(thin shrink small outline package)



S
MiniSO8
(plastic package)



DFN8 2x2 mm
(plastic micropackage)

Product status link
TSX3702

Related products	
See TSX393	for open drain output products

Features

- Low supply current: 5 µA typ. per comparator
- Wide single supply range 2.7 V to 16 V or dual supplies (±1.35 V to ±8 V)
- Extremely low input bias current: 1 pA typ.
- Input common-mode voltage range includes ground
- Push-pull output
- High input impedance: 10^{12} Ω typ
- Fast response time: 2.7 µs typ. for 5 mV overdrive
- ESD tolerance: 4 kV HBM, 200 V MM

Applications

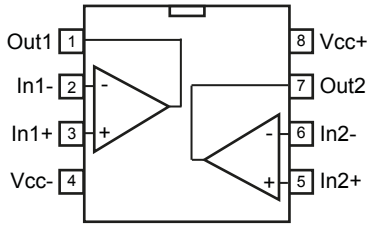
- Automotive
- Industrial

Description

The TSX3702 is a micropower CMOS dual voltage comparator which exhibits a very low current consumption of 5 µA typical per comparator. This device was designed as the improvement of the TS3702: it shows a lower current consumption, a better input offset voltage, and an enhanced ESD tolerance. The TSX3702 is fully specified over a wide temperature range and is proposed in automotive grade for the SO8 package. It is fully compatible with the TS3702 CMOS comparator and is available with similar packages. New tiny packages (MiniSO8 and DFN8 2x2 mm) are also proposed for the TSX3702 thus allowing even more integration on applications.

1 Package pin connections

Figure 1. **Pin connections top view**



2 Absolute maximum ratings

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter		Value	Unit
V_{CC} +	Supply voltage(1)		18	V
V_{id}	Differential input voltage(2)		±18	
V_{in}	Input voltage		-0.3 to 18	
V_o	Output voltage		18	
I_o	Output current		20	mA
I_F	Forward current in ESD protection diodes on inputs(3)		50	
T_j	Maximum junction temperature		150	°C
R_{thja}	Thermal resistance junction to ambient(4)	SO8	125	°C/W
		TSSOP8	120	
		MiniSO8	190	
		DFN8 2x2	57	
T_{stg}	Storage temperature range		-65 to 150	°C
ESD	HBM: human body model(5)		4000	V
	MM: machine model(6)		200	
	CDM: charged device model(7)		1500	
	Latch-up immunity		200	mA

1. *All voltage values, except differential voltage, are with respect to network ground terminal.*
2. *Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.*
3. *Guaranteed by design*
4. *Short-circuits can cause excessive heating and destructive dissipation. Values are typical.*
5. *According to JEDEC standard JESD22-A114F*
6. *According to JEDEC standard JESD22-A115A*
7. *According to ANSI/ESD STM5.3.1*

3 Operating conditions

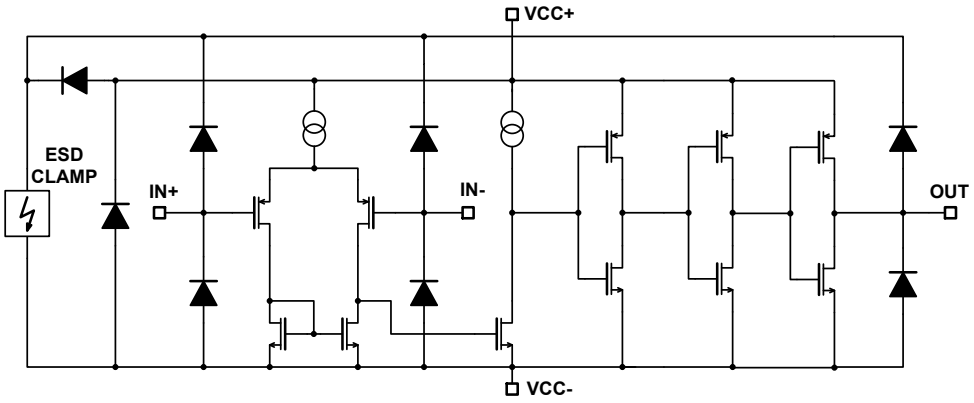
Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}^+	Supply voltage	2.7 to 16	V
V_{icm} (1)	Common mode input voltage range	0 to V_{CC}^+ - 1.5	
	$T_{min} \leq T_{amb} \leq T_{max}$	0 to V_{CC}^+ - 2	
T_{oper}	Operating free-air temperature range	-40 to 125	°C

1. *The output state is guaranteed as long as one input remains with this common mode input voltage range, and the other input remains between -0.3 V and 16 V (meaning that one input can be driven above VCC+).*

4 Schematic diagram

Figure 2. **Schematic diagram (one operator)**



5 Electrical characteristics

Table 3. V_{CC}^+ = 3 V, V_{CC}^- = 0 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage(1)	V_{icm} = 0 V	-5	0.1	5	mV
		$T_{min} \le T_{amb} \le T_{max}$	-6		6	
I_{io}	Input offset current (2)	$V_{icm} = V_{CC}/2$		1	10	pA
		$T_{min} \le T_{amb} \le T_{max}$			600	
I_{ib}	Input bias current(2)	$V_{icm} = V_{CC}/2$		1	10	
		$T_{min} \le T_{amb} \le T_{max}$			1200	
CMR	Common-mode rejection ratio	V_{icm} = 0 to max V_{icm}	58	73		dB
		$T_{min} \le T_{amb} \le T_{max}$	55			
SVR	Supply voltage rejection ratio	V_{CC}^+ = 3 V to 5 V, $V_{icm} = V_{CC}/2$	69	88		
		$T_{min} \le T_{amb} \le T_{max}$	69			
V_{OH}	High-level output voltage drop	V_{id} = 1 V, I_{OH} = 4 mA		300	400	mV
		$T_{min} \le T_{amb} \le T_{max}$			600	
V_{OL}	Low-level output voltage	V_{id} = -1 V, I_{OL} = 4 mA		300	400	
		$T_{min} \le T_{amb} \le T_{max}$			600	
I_{CC}	Supply current per comparator	No load, outputs low		5	6	µA
		$T_{min} \le T_{amb} \le T_{max}$			7	
		No load, outputs high		8	9	
		$T_{min} \le T_{amb} \le T_{max}$			11	
t_{PLH}	Response time low to high	V_{icm} = 0 V, f = 10 kHz, R_L = 5.1 kΩ, C_L = 50 pF, overdrive = 5 mV		2.4		µs
		Overdrive = 100 mV		0.5	0.6	
		$T_{min} \le T_{amb} \le T_{max}$			0.77	
t_{PHL}	Response time high to low	V_{icm} = 0 V, f = 10 kHz, R_L = 5.1 kΩ, C_L = 50 pF, overdrive = 5 mV		2.0		
		Overdrive = 100 mV		0.45	0.6	
		$T_{min} \le T_{amb} \le T_{max}$			0.65	
t_r	Rise time	f = 10 kHz, C_L = 50 pF, R_L = 5.1 kΩ, overdrive 50 mV		39		ns
t_f	Fall time	f = 10 kHz, C_L = 50 pF, R_L = 5.1 kΩ, overdrive 50 mV		39		

1. *The specified offset voltage is the maximum value required to drive the output up to 2.5 V or down to 0.3 V.*
2. *Guaranteed by design*

Table 4. V_{CC}^+ = 5 V, V_{CC}^- = 0 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (1)	$V_{icm} = V_{CC}/2$	-5	0.1	5	mV
		$T_{min} \le T_{amb} \le T_{max}$	-6		6	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{io}	Input offset current (2)	$V_{icm} = V_{CC}/2$		1	10	pA
		$T_{min} \le T_{amb} \le T_{max}$			600	
I_{ib}	Input bias current (2)	$V_{icm} = V_{CC}/2$		1	10	
		$T_{min} \le T_{amb} \le T_{max}$			1200	
CMR	Common-mode rejection ratio	V_{icm} = 0 to max V_{icm}	66	85		dB
		$T_{min} \le T_{amb} \le T_{max}$	65			
SVR	Supply voltage rejection ratio	V_{CC}^+ = 5 V to 10 V, $V_{icm} = V_{CC}/2$	71	89		
		$T_{min} \le T_{amb} \le T_{max}$	70			
V_{OH}	High-level output voltage drop	V_{id} = 1 V, I_{OH} = 4 mA		180	250	mV
		$T_{min} \le T_{amb} \le T_{max}$			400	
V_{OL}	Low-level output voltage	V_{id} = -1 V, I_{OL} = 4 mA		180	250	
		$T_{min} \le T_{amb} \le T_{max}$			400	
I_{CC}	Supply current per comparator	No load, outputs low		5	8	µA
		$T_{min} \le T_{amb} \le T_{max}$			9	
		No load, outputs high		9	10	
		$T_{min} \le T_{amb} \le T_{max}$			11	
t_{PLH}	Response time low to high	V_{icm} = 0 V, f = 10 kHz, R_L = 5.1 kΩ, C_L = 50 pF, overdrive = 5 mV		2.4		µs
		Overdrive = 10 mV		1.5		
		Overdrive = 20 mV		0.9		
		Overdrive = 40 mV		0.6		
		Overdrive = 100 mV		0.35	0.55	
		$T_{min} \le T_{amb} \le T_{max}$			0.6	
		TTL input (3)		0.45	0.6	
		$T_{min} \le T_{amb} \le T_{max}$			0.65	
t_{PHL}	Response time high to low	V_{icm} = 0 V, f = 10 kHz, R_L = 5.1 kΩ, C_L = 50 pF, overdrive = 5 mV		2.8		
		Overdrive = 10 mV		1.8		
		Overdrive = 20 mV		1.0		
		Overdrive = 40 mV		0.7		
		Overdrive = 100 mV		0.46	0.6	
		$T_{min} \le T_{amb} \le T_{max}$			0.7	
		TTL input (3)		0.30	0.40	
		$T_{min} \le T_{amb} \le T_{max}$			0.50	
t_r	Rise time	f = 10 kHz, C_L = 50 pF, R_L = 5.1 kΩ, overdrive 50 mV		30		ns
t_f	Fall time	f = 10 kHz, C_L = 50 pF, R_L = 5.1 kΩ, overdrive 50 mV		30		

1. *The specified offset voltage is the maximum value required to drive the output up to 4.5 V or down to 0.3 V.*
2. *Guaranteed by design*
3. *A step from 0 V to 3 V is applied on one input while the other is fixed at 1.4 V. Response time is the time interval between the application of the input voltage step and the moment the output voltage reaches 50 % of its final value.*

Table 5. V_{CC}^{+} = 16 V, V_{CC}^{-} = 0 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (1)	$V_{icm} = V_{CC}/2$	-5	0.1	5	mV
		$T_{min} \le T_{amb} \le T_{max}$	-6		6	
I_{io}	Input offset current (2)	$V_{icm} = V_{CC}/2$		1	10	pA
		$T_{min} \le T_{amb} \le T_{max}$			600	
I_{ib}	Input bias current (2)	$V_{icm} = V_{CC}/2$		1	10	
		$T_{min} \le T_{amb} \le T_{max}$			1200	
CMR	Common-mode rejection ratio	V_{icm} = 0 to max V_{icm}	72	90		dB
		$T_{min} \le T_{amb} \le T_{max}$	70			
SVR	Supply voltage rejection ratio	V_{CC}^{+} = 5 V to 16 V, $V_{icm} = V_{CC}/2$	73	90		
		$T_{min} \le T_{amb} \le T_{max}$	72			
V_{OH}	High-level output voltage drop	V_{id} = 1 V, I_{OH} = 4 mA		90	150	mV
		$T_{min} \le T_{amb} \le T_{max}$			250	
V_{OL}	Low-level output voltage	V_{id} = -1 V, I_{OL} = 4 mA		90	150	
		$T_{min} \le T_{amb} \le T_{max}$			250	
I_{CC}	Supply current per comparator	No load, outputs low		7	9	µA
		$T_{min} \le T_{amb} \le T_{max}$			10	
		No load, outputs high		11	13	
		$T_{min} \le T_{amb} \le T_{max}$			14	
t_{PLH}	Response time low to high	V_{icm} = 0 V, f = 10 kHz, R_L = 5.1 kΩ, C_L = 50 pF, overdrive = 5 mV		2.2		µs
		Overdrive = 10 mV		1.4		
		Overdrive = 20 mV		0.9		
		Overdrive = 40 mV		0.6		
		Overdrive = 100 mV		0.34	0.55	
		$T_{min} \le T_{amb} \le T_{max}$			0.60	
t_{PHL}	Response time high to low	V_{icm} = 0 V, f = 10 kHz, R_L = 5.1 kΩ, C_L = 50 pF, overdrive = 5 mV		2.4		
		Overdrive = 10 mV		1.6		
		Overdrive = 20 mV		1.0		
		Overdrive = 40 mV		0.7		
		Overdrive = 100 mV		0.55	0.70	
		$T_{min} \le T_{amb} \le T_{max}$			0.75	
t_r	Rise time	f = 10 kHz, C_L = 50 pF, R_L = 5.1 kΩ, overdrive 50 mV		11		ns
t_f	Fall time	f = 10 kHz, C_L = 50 pF, R_L = 5.1 kΩ, overdrive 50 mV		11		

1. *The specified offset voltage is the maximum value required to drive the output up to 4.5 V or down to 0.3 V.*
2. *Guaranteed by design*

Figure 3. Current consumption vs. supply voltage, output high

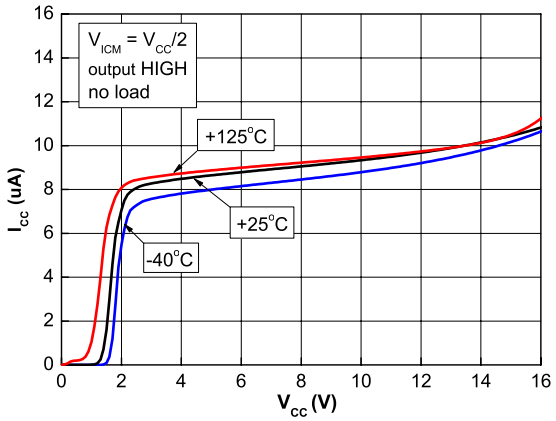


Figure 4. Current consumption vs. supply voltage, output low

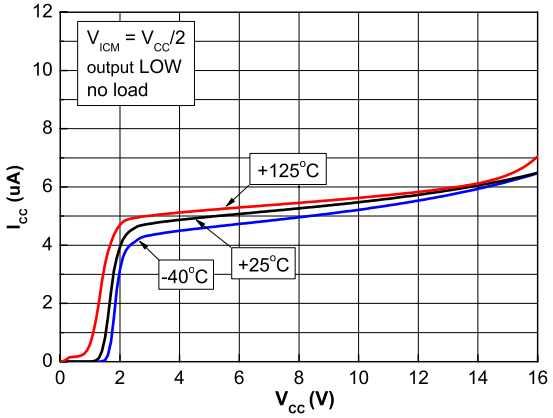


Figure 5. Current consumption vs. input common-mode voltage, output high

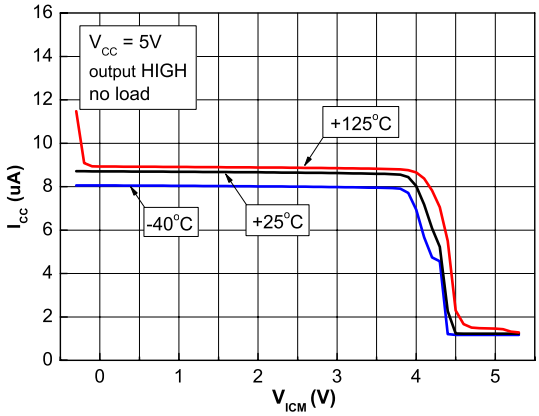


Figure 6. Current consumption vs. common-mode voltage, output low

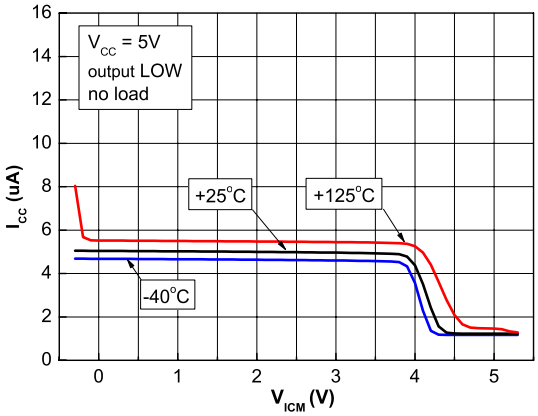


Figure 7. Output voltage drop vs. output source current, V_{CC} = 5 V

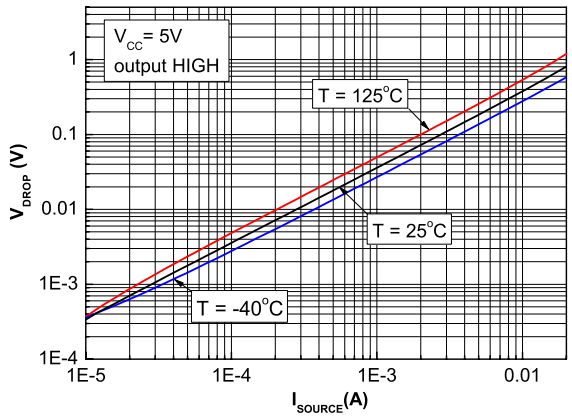


Figure 8. Output voltage drop vs. output source current, V_{CC} = 12 V

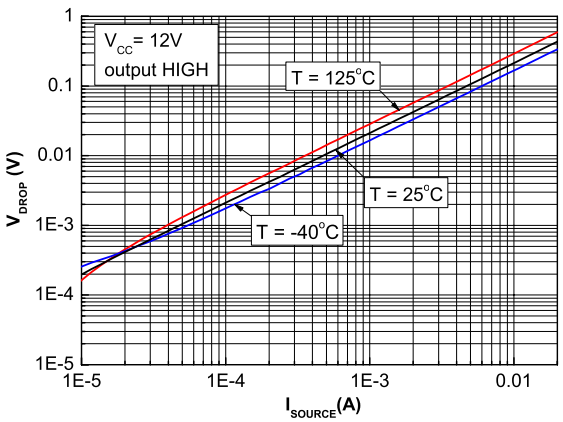


Figure 9. Output voltage drop vs. output sink current, V_{CC} = 5 V

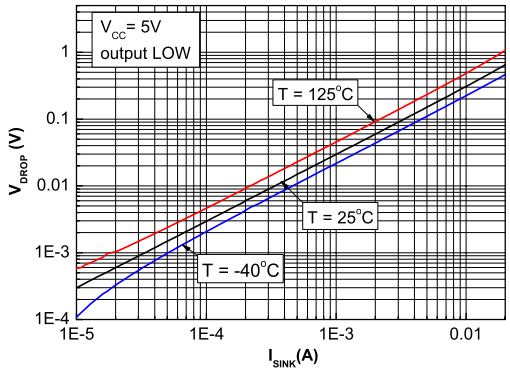


Figure 10. Output voltage drop vs. output sink current, V_{CC} = 12 V

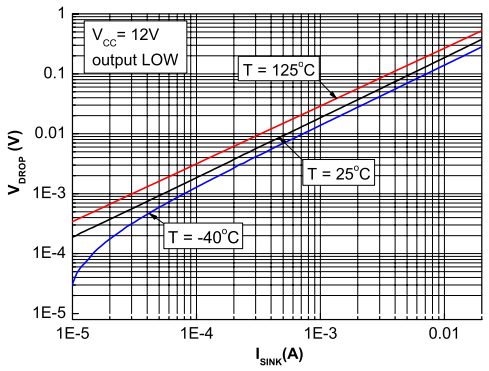


Figure 11. Input offset voltage distribution, V_{CC} = 5 V

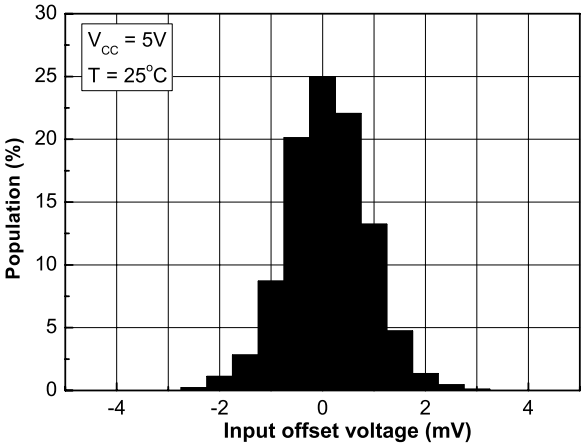


Figure 12. Input current versus input voltage, V_{CC} = 5 V

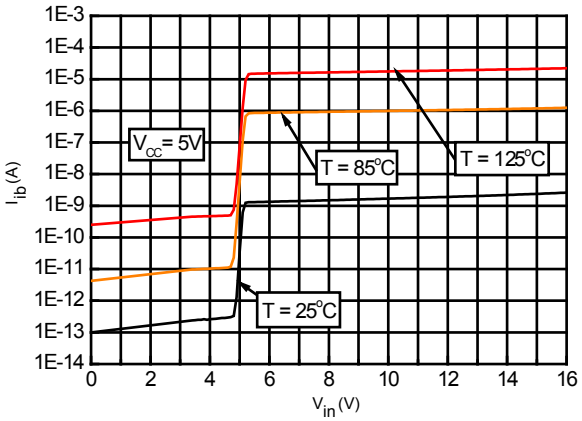


Figure 13. Propagation delay t_{PLH} vs. input signal overdrive, V_{CC} = 5 V

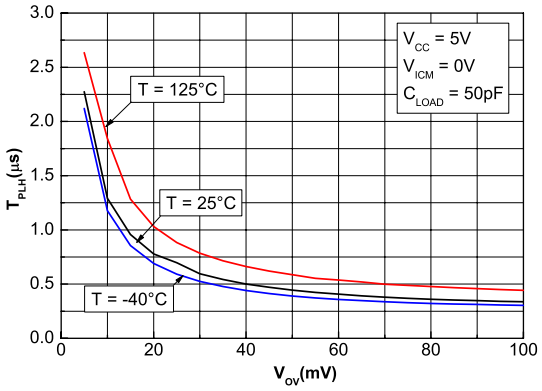


Figure 14. Propagation delay t_{PHL} vs. input signal overdrive, V_{CC} = 5 V

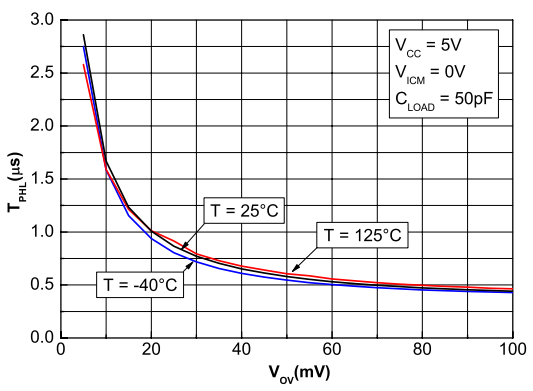


Figure 15. Propagation delay t_{PLH} vs. supply voltage, V_{CC} = 5 V

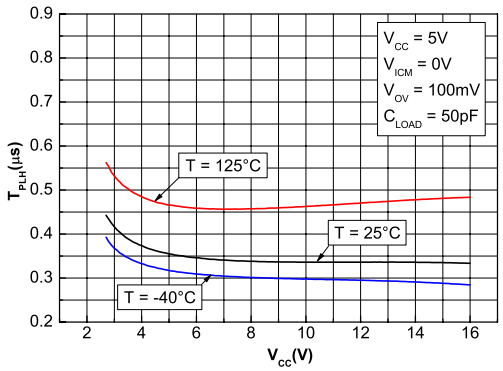
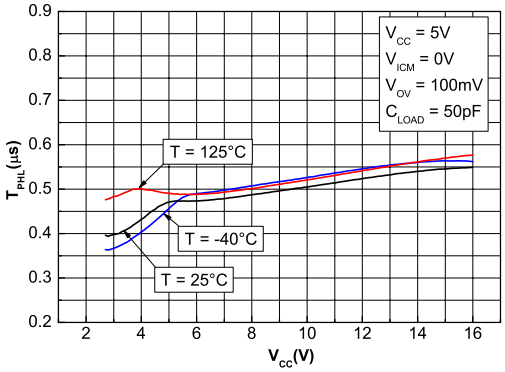


Figure 16. Propagation delay t_{PHL} vs. supply voltage, V_{CC} = 5 V



6 Application information (input voltages)

The ESD strategy used in the TSX3702 (and shown in Figure 2. Schematic diagram (one operator) allows input voltages from -0.3 V up to 16 V to be applied regardless of the V_{CC}+ voltage. When $V_{IN} > V_{CC}$+ a leakage current goes from the input through the protection diode to the ESD clamp. This current is about 0.2 nA at 25 °C and about 250 nA at 125 °C. For a detailed input characteristic see Section 5 Figure 12. The device is designed to prevent phase reversal.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 SO8 package information

Figure 17. SO8 package outline

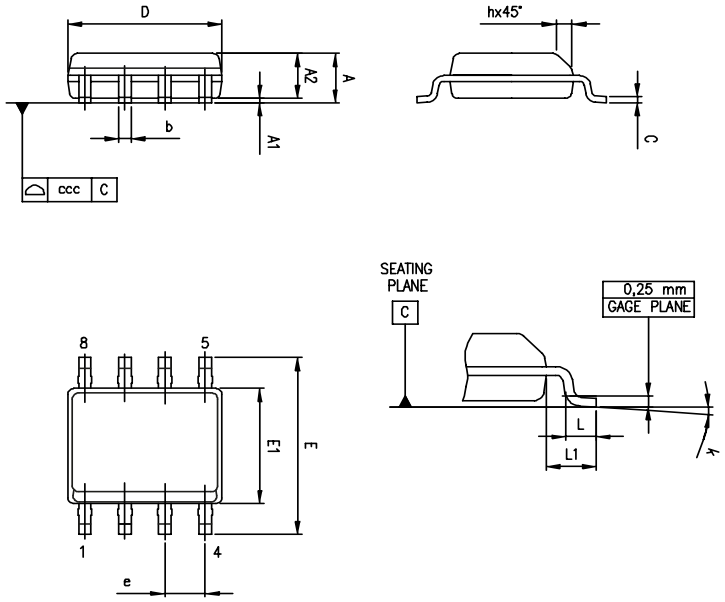


Table 6. SO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	0°		8°	0°		8°
ccc			0.10			0.004

7.2 TSSOP8 package information

Figure 18. **TSSOP8 package outline**

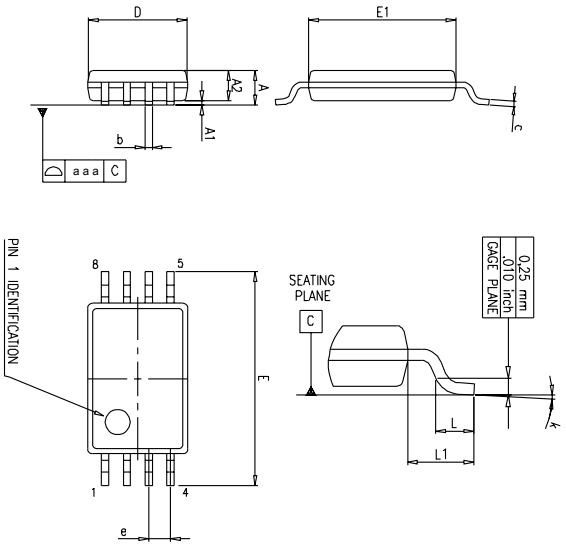


Table 7. **TSSOP8 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa		0.10			0.004	

7.3 DFN8 2x2 package information

Figure 19. **DFN8 2x2 package outline**

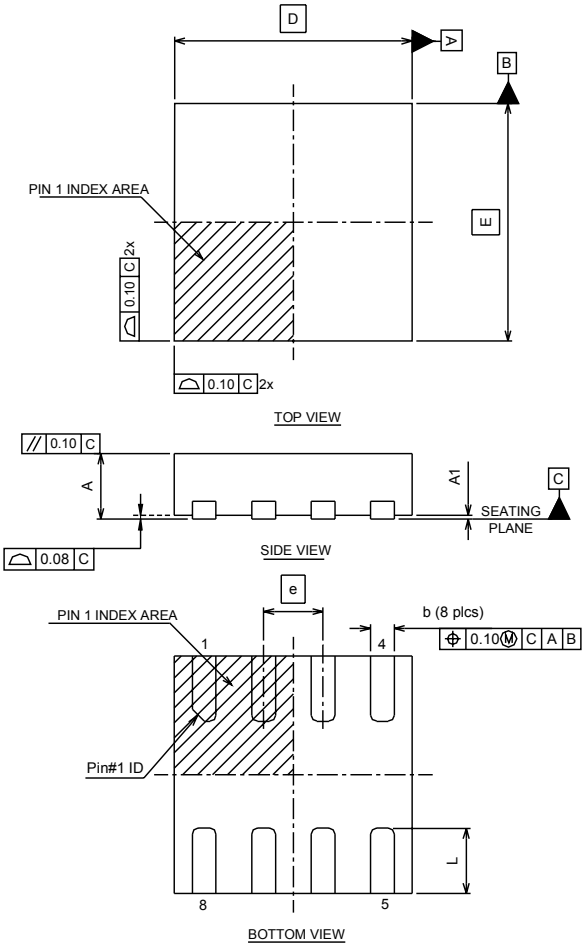
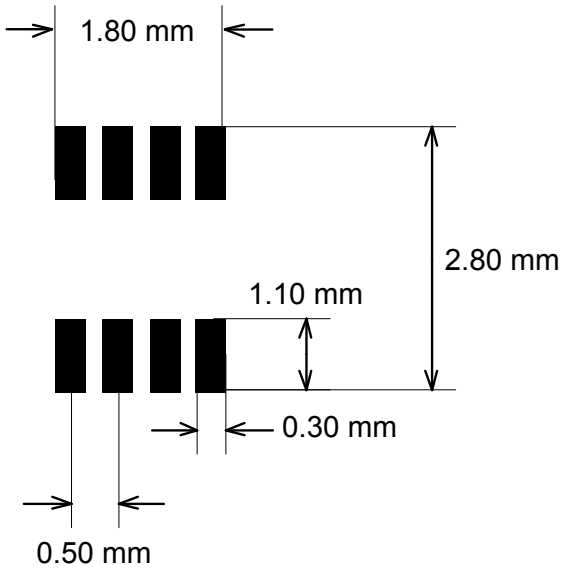


Table 8. **DFN8 2x2 mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.15	0.20	0.25	0.006	0.008	0.010
D		2.00			0.079	
E		2.00			0.079	
e		0.50			0.020	
L	0.045	0.55	0.65	0.018	0.022	0.026
N	8					

Figure 20. **DFN8 2x2 recommended footprint**



7.4 MiniSO8 package information

Figure 21. **MiniSO8 package outline**

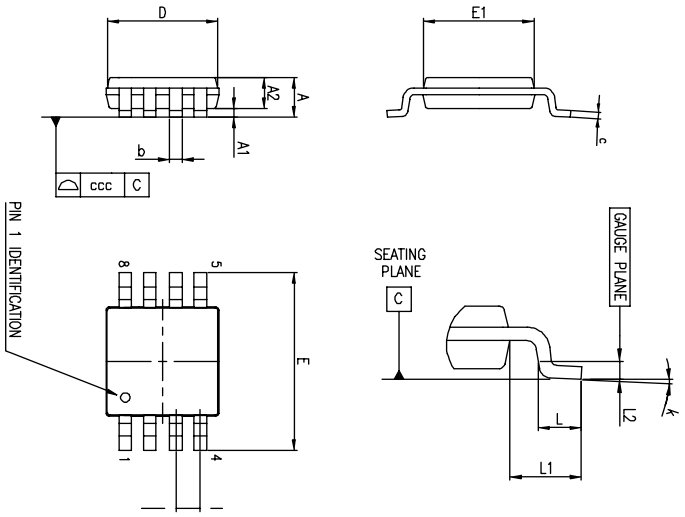


Table 9. **MiniSO8 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.0006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

8 Ordering information

Table 10. Order codes

Order code	Temperature range	Package	Packing	Marking
TSX3702IDT	-40 °C, 125 °C	SO8	Tape and reel	SX3702
TSX3702IPT		TSSOP8		S3702
TSX3702IST		MiniSO8		K532
TSX3702IQ2T		DFN8 2x2		K5J
TSX3702IYDT(1)		SO8 (automotive grade)		SX3702Y

1. *Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.*

Revision history

Table 11. **Document revision history**

Date	Revision	Changes
18-Apr-2014	1	Initial release.
13-Feb-2015	2	Table 1: Absolute maximum ratings (AMR): removed footnote associated with Vin. Table 2: Operating conditions: added footnote concerning Vicm. Figure 2: Schematic diagram (one operator): updated Table 6: added "L1"
06-Jun-2016	3	Table 3, Table 4, and Table 5: updated several values (I_{io}, I_{ib}, t_{PLH}, and t_{PHL}) and conditions (V_{OH}, V_{OL}, and CMR) Table 10: updated marking of order code TSX3702IPT (now SX3702 instead of 5X3702), updated automotive order code footnote.
15-May-2017	4	Updated automotive footnote in Table 10. Order codes.
02-Sep-2019	5	Updated Section 7.3 DFN8 2x2 package information.
20-Jan-2023	6	Updated figure on the cover page.

Contents

1 Package pin connections 2
2 Absolute maximum ratings 3
3 Operating conditions 4
4 Schematic diagram 5
5 Electrical characteristics 6
6 Application information (input voltages) 12
7 Package information 13
7.1 SO8 package information 13
7.2 TSSOP8 package information 14
7.3 DFN8 2x2 package information 15
7.4 MiniSO8 package information 17
8 Ordering information 18
Revision history 19

List of figures

Figure 1. Pin connections top view . . . 2
Figure 2. Schematic diagram (one operator) . . . 5
Figure 3. Current consumption vs. supply voltage, output high . . . 9
Figure 4. Current consumption vs. supply voltage, output low . . . 9
Figure 5. Current consumption vs. input common-mode voltage, output high . . . 9
Figure 6. Current consumption vs. common-mode voltage, output low . . . 9
Figure 7. Output voltage drop vs. output source current, V_{CC} = 5 V . . . 9
Figure 8. Output voltage drop vs. output source current, V_{CC} = 12 V . . . 9
Figure 9. Output voltage drop vs. output sink current, V_{CC} = 5 V . . . 10
Figure 10. Output voltage drop vs. output sink current, V_{CC} = 12 V . . . 10
Figure 11. Input offset voltage distribution, V_{CC} = 5 V . . . 10
Figure 12. Input current versus input voltage, V_{CC} = 5 V . . . 10
Figure 13. Propagation delay t_{PLH} vs. input signal overdrive, V_{CC} = 5 V . . . 10
Figure 14. Propagation delay t_{PHL} vs. input signal overdrive, V_{CC} = 5 V . . . 10
Figure 15. Propagation delay t_{PLH} vs. supply voltage, V_{CC} = 5 V . . . 11
Figure 16. Propagation delay t_{PHL} vs. supply voltage, V_{CC} = 5 V . . . 11
Figure 17. SO8 package outline . . . 13
Figure 18. TSSOP8 package outline . . . 14
Figure 19. DFN8 2x2 package outline . . . 15
Figure 20. DFN8 2x2 recommended footprint . . . 16
Figure 21. MiniSO8 package outline . . . 17

List of tables

Table 1. Absolute maximum ratings (AMR) . . . 3
Table 2. Operating conditions . . . 4
Table 3. V_{CC}^{+} = 3 V, V_{CC}^{-} = 0 V, T_{amb} = 25 °C (unless otherwise specified) . . . 6
Table 4. V_{CC}^{+} = 5 V, V_{CC}^{-} = 0 V, T_{amb} = 25 °C (unless otherwise specified) . . . 6
Table 5. V_{CC}^{+} = 16 V, V_{CC}^{-} = 0 V, T_{amb} = 25 °C (unless otherwise specified) . . . 8
Table 6. SO8 package mechanical data . . . 13
Table 7. TSSOP8 package mechanical data . . . 14
Table 8. DFN8 2x2 mechanical data . . . 15
Table 9. MiniSO8 package mechanical data . . . 17
Table 10. Order codes . . . 18
Table 11. Document revision history . . . 19

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2023 STMicroelectronics – All rights reserved