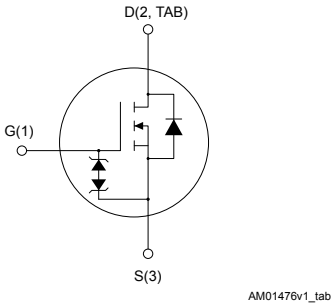
# STB14NK60ZT4, STP14NK60ZFP

Datasheet

## N-channel 600 V, 0.45 Ω typ., 13.5 A SuperMESH Power MOSFETs in D²PAK and TO-220FP packages




D²PAK TO-220FP




## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|---|---|---|---|
| STB14NK60ZT4 | 600 V | 0.5 Ω | 13.5 A |
| STP14NK60ZFP | | | |

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

## Applications

- Switching applications

## Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

| Product status links |
|---|
| STB14NK60ZT4 |
| STP14NK60ZFP |

| Product summary | |
|---|---|
| **Order code** | **STB14NK60ZT4** |
| **Marking** | B14NK60Z |
| **Package** | D²PAK |
| **Packing** | Tape and reel |
| **Order code** | **STP14NK60ZFP** |
| **Marking** | P14NK60ZFP |
| **Package** | TO-220FP |
| **Packing** | Tube |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | $D^2PAK$ | TO-220FP | |
| $V_{DS}$ | Drain-source voltage | 600 | | V |
| $V_{DGR}$ | Drain-gate voltage ($R_{GS}$ = 20 kΩ) | 600 | | V |
| $V_{GS}$ | Gate-source voltage | ±30 | | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 13.5 | 13.5(1) | A |
| | Drain current (continuous) at $T_C$ = 100 °C | 8.5 | 8.5(1) | |
| $I_{DM}$(2) | Drain current (pulsed) | 54 | 54(1) | A |
| $P_{TOT}$ | Total power dissipation at $T_C$ = 25 °C | 160 | 40 | W |
| ESD | Gate-source human body model (C = 100 pF, R = 1.5 kΩ) | 4 | | kV |
| dv/dt(3) | Peak diode recovery voltage slope | 4.5 | | V/ns |
| $V_{ISO}$ | Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, $T_C$ = 25 °C) | | 2.5 | kV |
| $T_{stg}$ | Storage temperature range | -55 to 150 | | °C |
| $T_J$ | Operating junction temperature range | | | |

1. *Limited by maximum junction temperature.*
2. *Pulse width is limited by safe operating area.*
3. *$I_{SD}$ ≤ 13.5 A, di/dt ≤ 200 A/µs, $V_{DD}$ ≤ $V_{(BR)DSS}$.*

**Table 2. Thermal data**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | $D^2PAK$ | TO-220FP | |
| $R_{thJC}$ | Thermal resistance, junction-to-case | 0.78 | 3.1 | °C/W |
| $R_{thJA}$ | Thermal resistance, junction-to-ambient | 62.5 | | °C/W |

**Table 3. Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width is limited by $T_J$ max.) | 12 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 300 | mJ |

# 2 Electrical characteristics

$T_C$ = 25 °C unless otherwise specified.

**Table 4. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 V | 600 | - | - | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0 V, $V_{DS}$ = 600 V | - | - | 1 | µA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 600 V, $T_C$ = 125 °C(1) | - | - | 50 | |
| $I_{GSS}$ | Gate body leakage current | $V_{GS}$ = ±30 V, $V_{DS}$ = 0 V | - | - | ±10 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 100 µA | 3.00 | 3.75 | 4.50 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 6 A | - | 0.45 | 0.5 | Ω |

1. *Specified by design, not tested in production.*

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 25 V, f = 1 MHz, $V_{GS}$ = 0 V | - | 2220 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 240 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 57 | - | pF |
| $C_{oss\ eq.}$(1) | Equivalent output capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 0 to 480 V | - | 122 | - | pF |
| $Q_g$ | Total gate charge | $V_{DD}$ = 480 V, $I_D$ = 12 A, $V_{GS}$ = 0 to 10 V (see the Figure 17. Test circuit for gate charge behavior) | - | 75 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 13.2 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 38.6 | - | nC |

1. *$C_{oss\ eq.}$ is defined as the constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$.*

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 300 V, $I_D$ = 6 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see the Figure 16. Test circuit for resistive load switching times and Figure 21. Switching time waveform) | - | 26 | - | ns |
| $t_r$ | Rise time | | - | 18 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 62 | - | ns |
| $t_f$ | Fall time | | - | 13 | - | ns |
| $t_{r(Voff)}$ | Off-voltage rise time | $V_{DD}$ = 480 V, $I_D$ = 12 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see the Figure 18. Test circuit for inductive load switching and diode recovery times) | - | 12 | - | ns |
| $t_f$ | Fall time | | - | 9.5 | - | ns |
| $t_c$ | Cross-over time | | - | 22 | - | ns |

**Table 7. Source-drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | - | 12 | A |
| $I_{SDM}$(1) | Source-drain current (pulsed) | | - | - | 48 | A |
| $V_{SD}$(2) | Forward on voltage | $I_{SD}$ = 12 A, $V_{GS}$ = 0 V | - | - | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 12 A, di/dt = 100 A/µs, | - | 490 | - | ns |
| $Q_{rr}$ | Reverse recovery charge | $V_{DD}$ = 50 V | - | 4.7 | - | µC |
| $I_{RRM}$ | Reverse recovery current | (see the Figure 18. Test circuit for inductive load switching and diode recovery times) | - | 19.3 | - | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 12 A, di/dt = 100 A/µs, | - | 664 | - | ns |
| $Q_{rr}$ | Reverse recovery charge | $V_{DD}$ = 50 V, $T_J$ = 150 °C | - | 6.8 | - | µC |
| $I_{RRM}$ | Reverse recovery current | (see the Figure 18. Test circuit for inductive load switching and diode recovery times) | - | 20.5 | - | A |

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area for D²PAK**

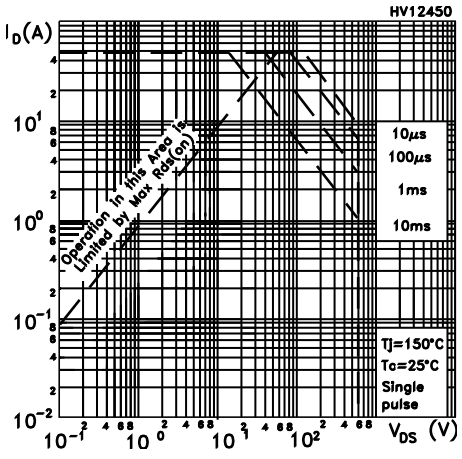



**Figure 2. Normalized transient thermal impedance for D²PAK**

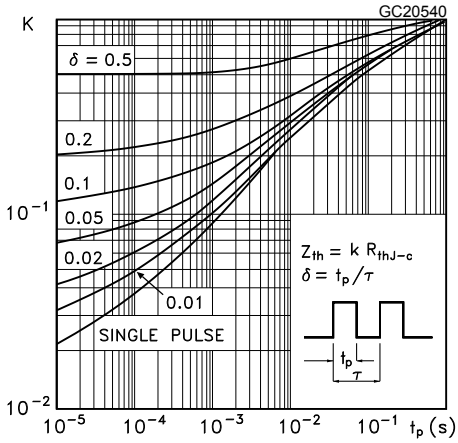



**Figure 3. Safe operating area for TO-220FP**

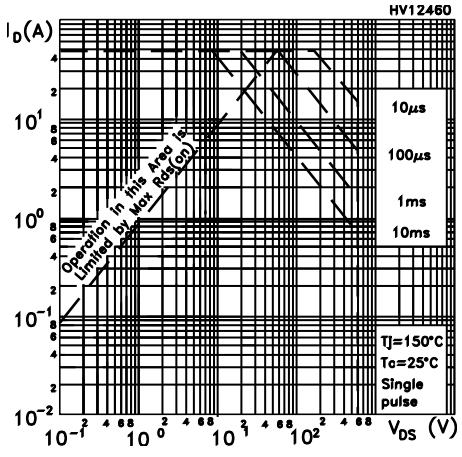



**Figure 4. Normalized transient thermal impedance for TO-220FP**

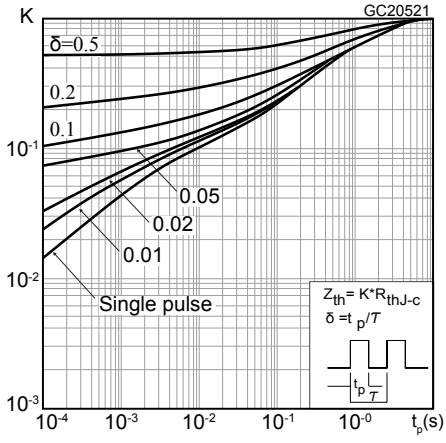



**Figure 5. Typical output characteristics**

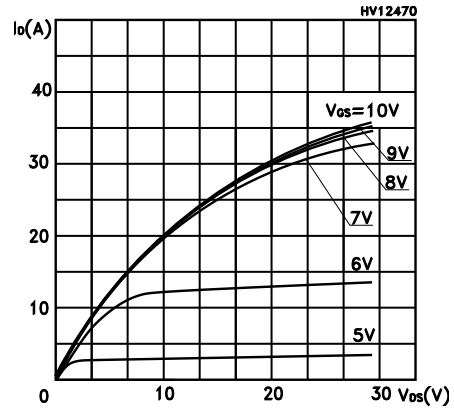



**Figure 6. Typical transfer characteristics**

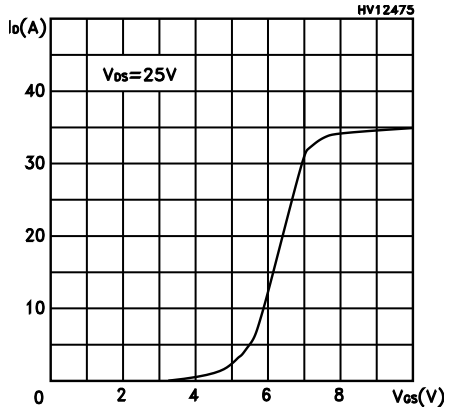


**Figure 7. Typical transconductance characteristics**

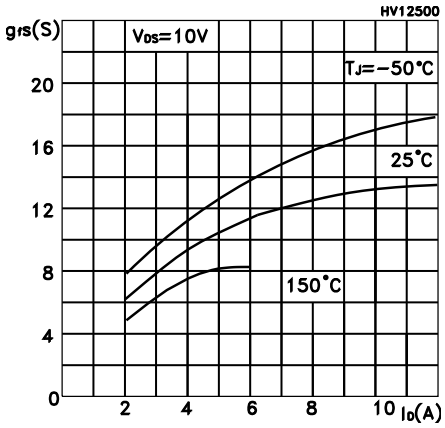



**Figure 8. Typical drain-source on-resistance**

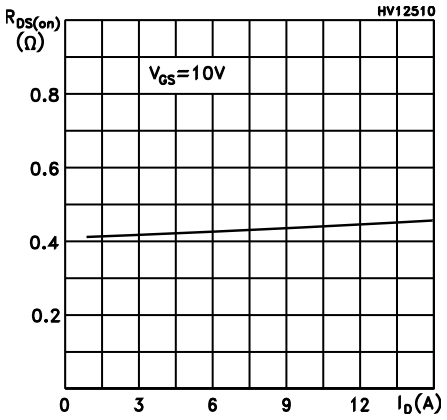



**Figure 9. Typical gate charge characteristics**

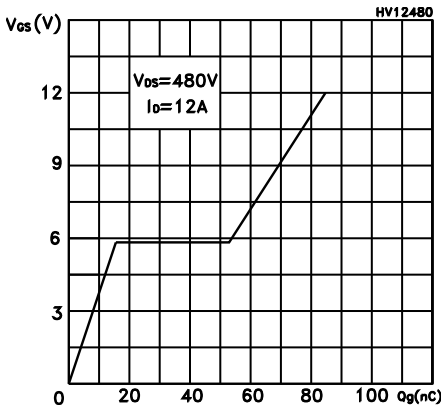



**Figure 10. Typical capacitance characteristics**

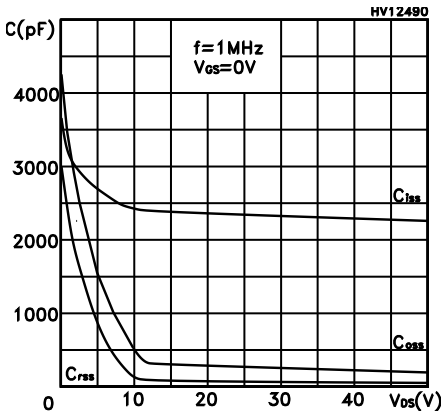



**Figure 11. Normalized gate threshold vs temperature**

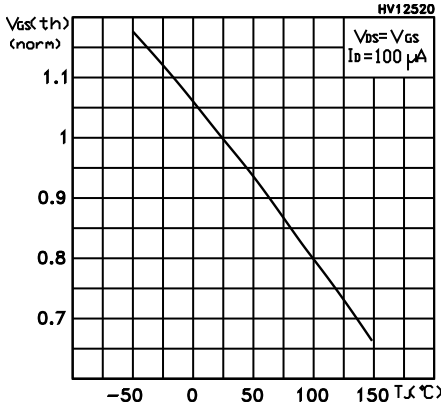



**Figure 12. Normalized on-resistance vs temperature**

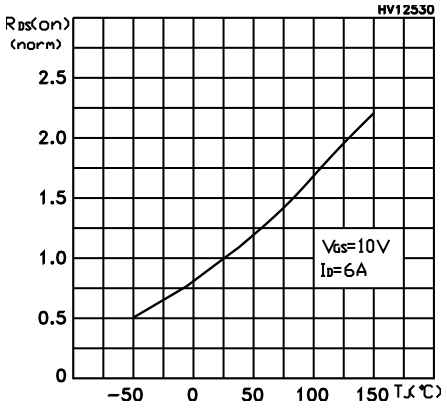


**Figure 13.** Typical reverse diode forward characteristics

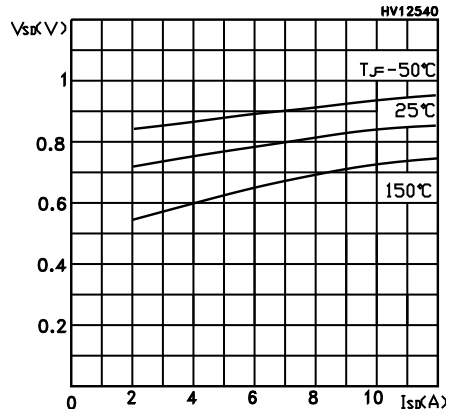



**Figure 14.** Normalized breakdown voltage vs temperature

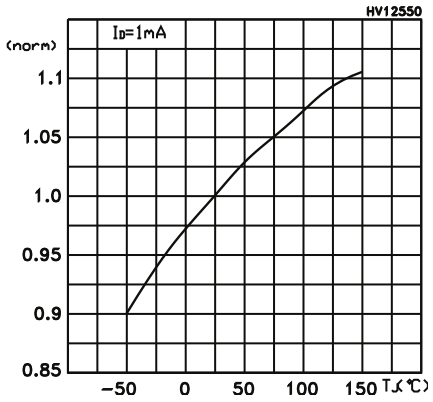
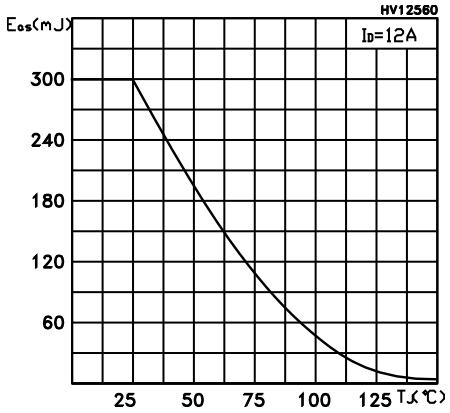
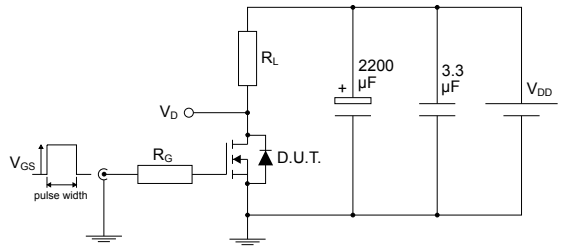



**Figure 15.** Maximum avalanche energy vs temperature



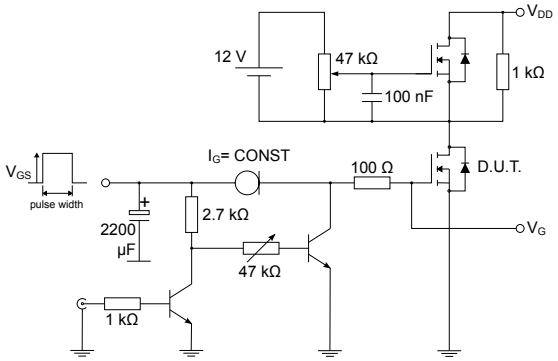
# 3 Test circuits

**Figure 16. Test circuit for resistive load switching times**



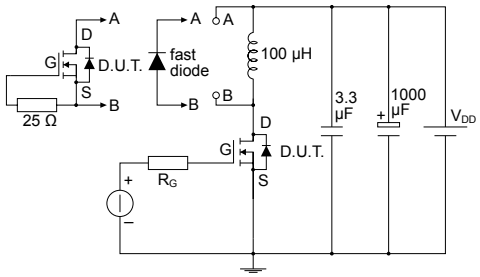

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**Figure 17. Test circuit for gate charge behavior**



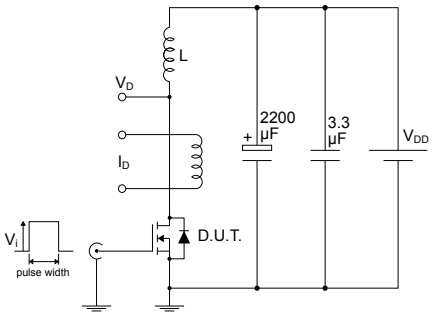

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**Figure 18. Test circuit for inductive load switching and diode recovery times**



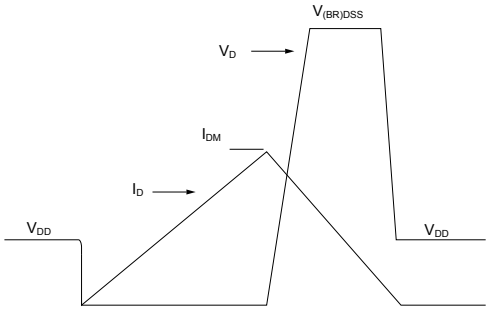

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**Figure 19. Unclamped inductive load test circuit**



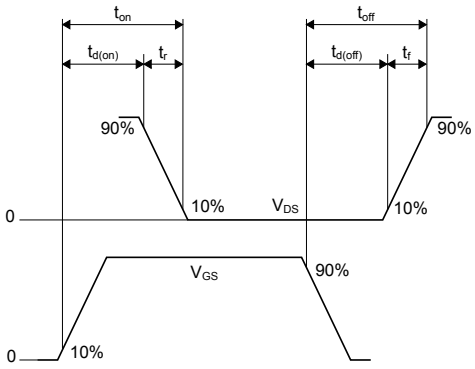

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**Figure 20. Unclamped inductive waveform**




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**Figure 21. Switching time waveform**



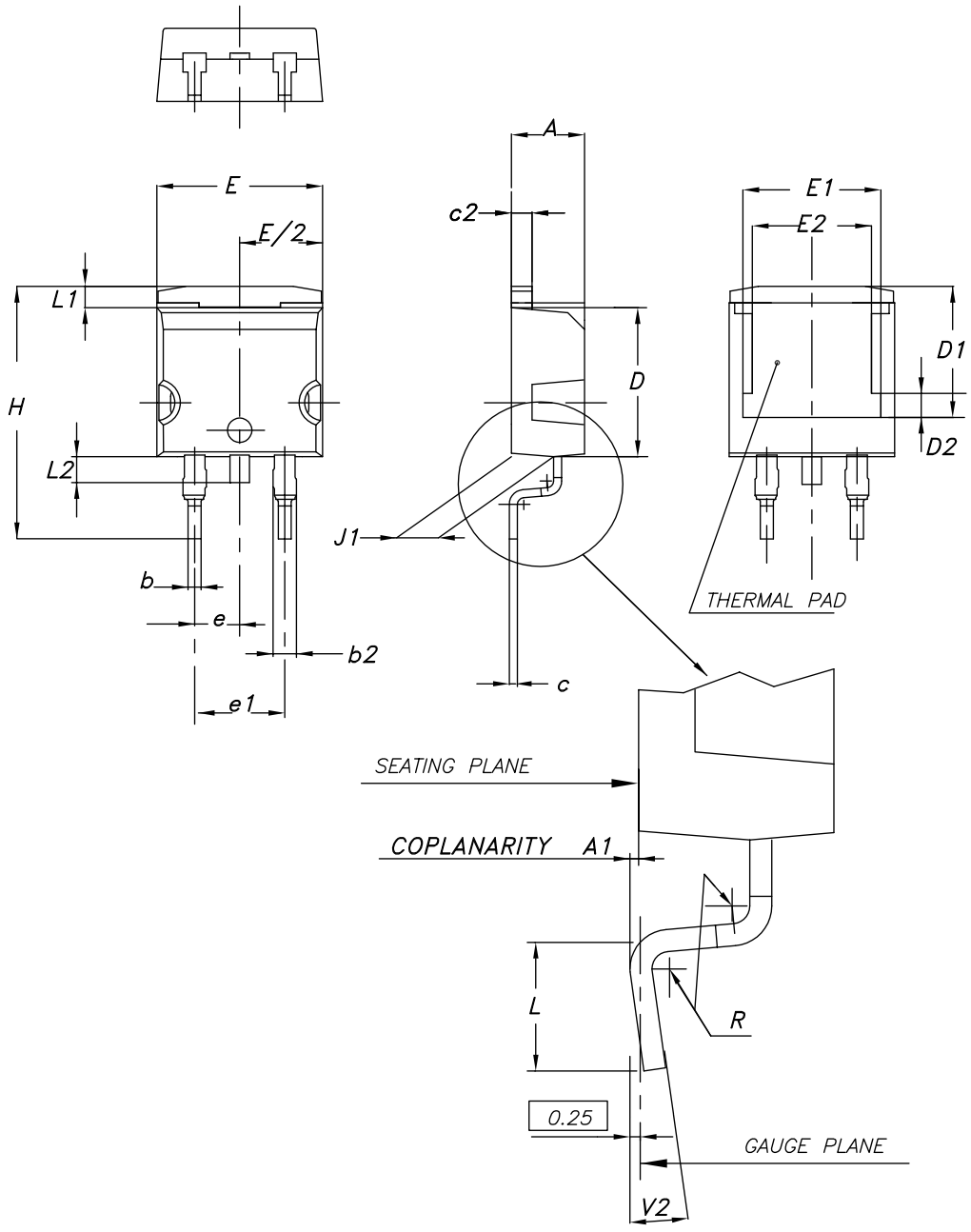

AM01473v1

# 4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 4.1 D²PAK (TO-263) type A2 package information

Figure 22. **D²PAK (TO-263) type A2 package outline**

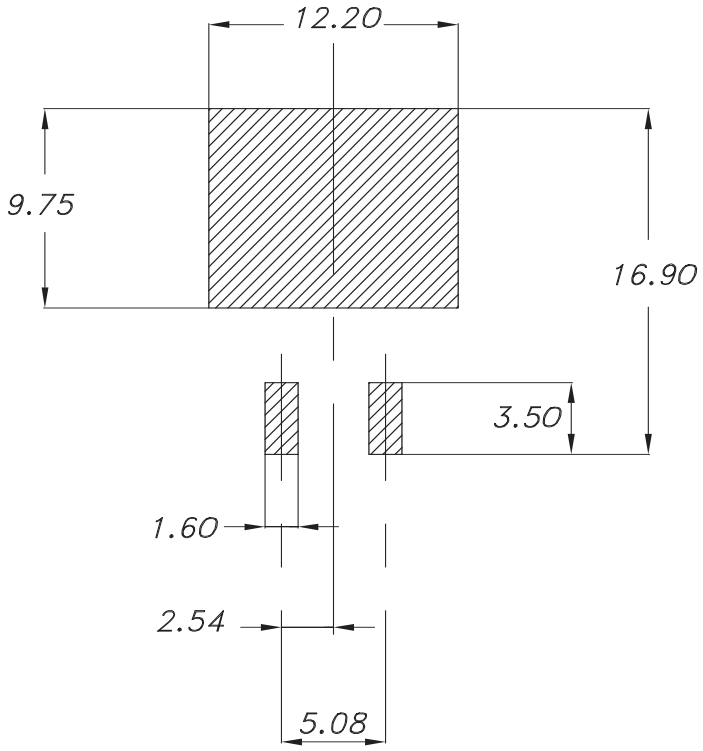



0079457_A2_27

Table 8. **D²PAK (TO-263) type A2 package mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| A1 | 0.03 | | 0.23 |
| b | 0.70 | | 0.93 |
| b2 | 1.14 | | 1.70 |
| c | 0.45 | | 0.60 |
| c2 | 1.23 | | 1.36 |
| D | 8.95 | | 9.35 |
| D1 | 7.50 | 7.75 | 8.00 |
| D2 | 1.10 | 1.30 | 1.50 |
| E | 10.00 | | 10.40 |
| E1 | 8.70 | 8.90 | 9.10 |
| E2 | 7.30 | 7.50 | 7.70 |
| e | | 2.54 | |
| e1 | 4.88 | | 5.28 |
| H | 15.00 | | 15.85 |
| J1 | 2.49 | | 2.69 |
| L | 2.29 | | 2.79 |
| L1 | 1.27 | | 1.40 |
| L2 | 1.30 | | 1.75 |
| R | | 0.40 | |
| V2 | 0° | | 8° |

Figure 23. D²PAK (TO-263) recommended footprint (dimensions are in mm)



## 4.2 TO-220FP type B package information

Figure 24. **TO-220FP type B package outline**

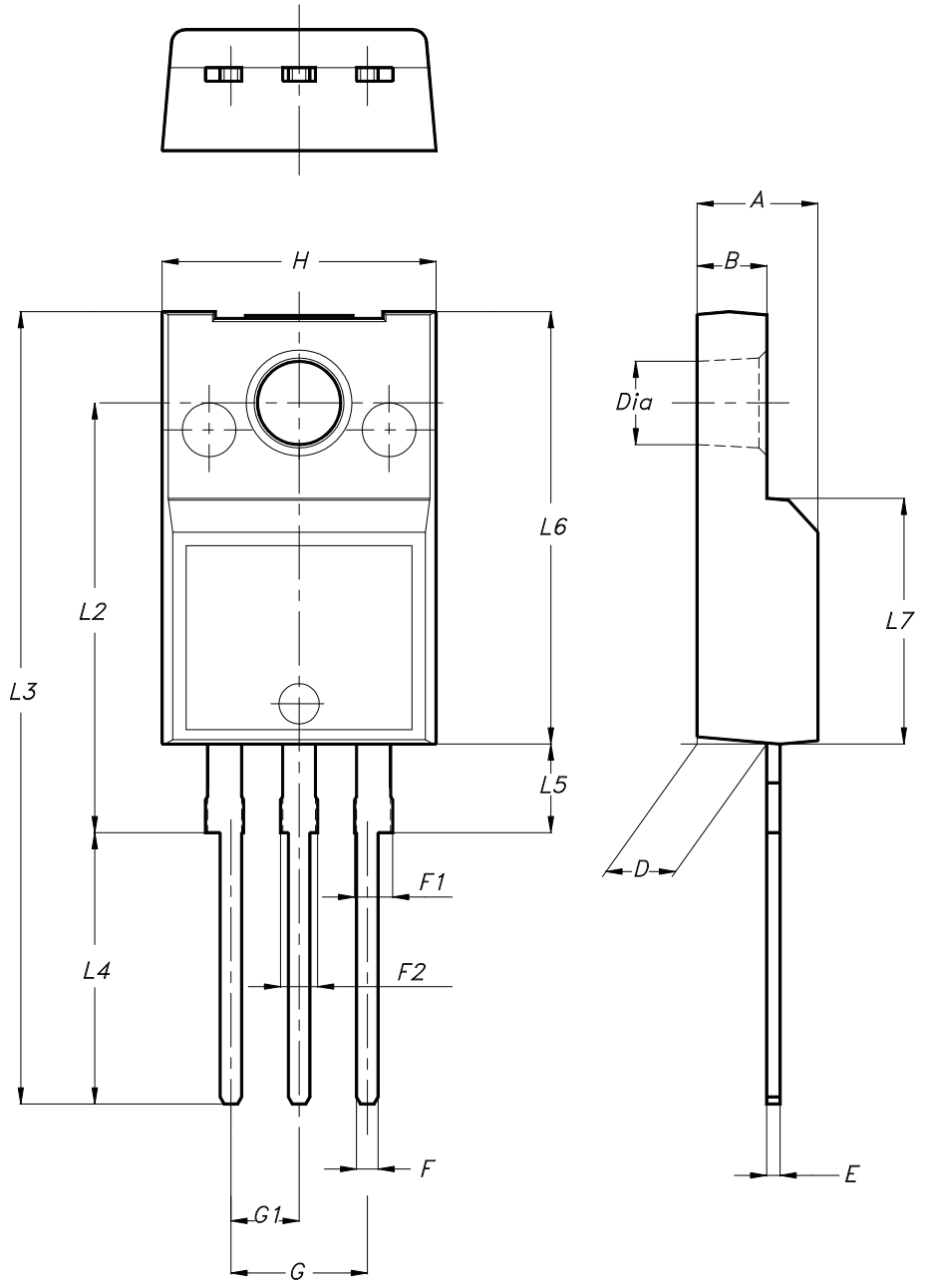
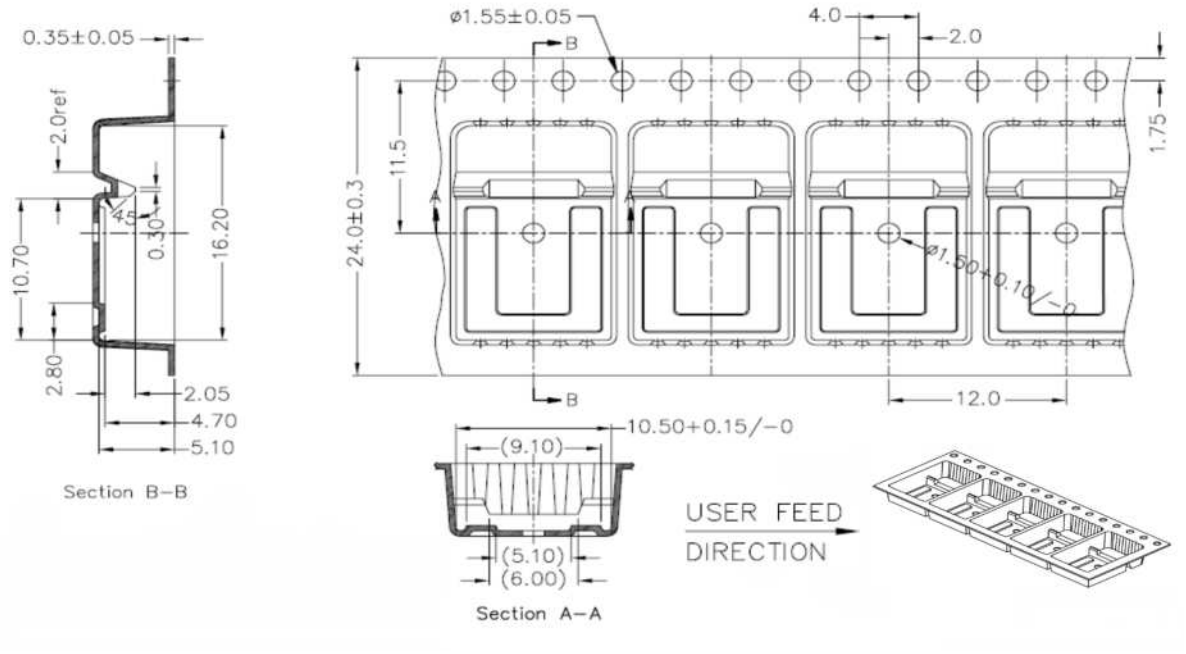


Table 9. **TO-220FP type B package mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| B | 2.50 | | 2.70 |
| D | 2.50 | | 2.75 |
| E | 0.45 | | 0.70 |
| F | 0.75 | | 1.00 |
| F1 | 1.15 | | 1.70 |
| F2 | 1.15 | | 1.70 |
| G | 4.95 | | 5.20 |
| G1 | 2.40 | | 2.70 |
| H | 10.00 | | 10.40 |
| L2 | | 16.00 | |
| L3 | 28.60 | | 30.60 |
| L4 | 9.80 | | 10.60 |
| L5 | 2.90 | | 3.60 |
| L6 | 15.90 | | 16.40 |
| L7 | 9.00 | | 9.30 |
| Dia | 3.00 | | 3.20 |

## 4.3 D²PAK packing information

Figure 25. D²PAK tape drawing (dimensions are in mm)




DM01095771_2

## Revision history

Table 10. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 06-May-2014 | 1 | Initial release. Part numbers previously included in datasheet DocID8984. |
| 22-Jul-2025 | 2 | Updated Section 4: Package information.<br>Minor text changes. |

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