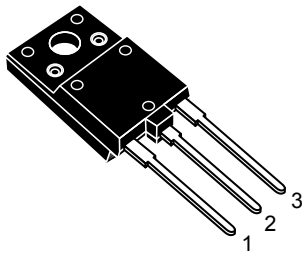
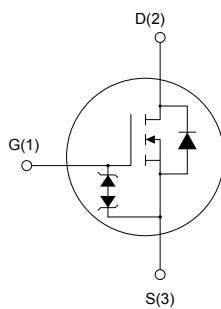


N-channel 1050 V, 6 Ω typ., 1.5 A MDmesh K5 Power MOSFET in a TO-3PF package



TO-3PF



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Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STFW2N105K5	1050 V	8 Ω	1.5 A	30 W

- Very low FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.



Product status link

[STFW2N105K5](#)

Product summary

Order code	STFW2N105K5
Marking	2N105K5
Package	TO-3PF
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	2	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	1.3	
$I_{DM}^{(1)}$	Drain current pulsed	6	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	30	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$, $T_C = 25\text{ }^{\circ}\text{C}$)	3.5	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_J	Operating junction temperature range	-55 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		$^{\circ}\text{C}$

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 1.5\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DS(peak)} \leq V_{(BR)DSS}$.
3. $V_{DD} \leq 840\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	4.2	$^{\circ}\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	50	$^{\circ}\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{Jmax.}$)	0.5	A
E_{AS}	Single-pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	90	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	1050	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 1050\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 1050\text{ V}$ $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$	-	-	50	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$	-	-	± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 0.75\text{ A}$	-	6	8	Ω

1. Specified by design, not tested in production.

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$	-	115	-	pF
C_{oss}	Output capacitance		-	15	-	pF
C_{rss}	Reverse transfer capacitance		-	0.4	-	pF
$C_{o(tr)}^{(1)}$	Time-related equivalent capacitance	$V_{DS} = 0\text{ to }840\text{ V}$, $V_{GS} = 0\text{ V}$	-	17	-	pF
$C_{o(er)}^{(2)}$	Energy-related equivalent capacitance		-	6	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	20	-	Ω
Q_g	Total gate charge	$V_{DD} = 840\text{ V}$, $I_D = 1.5\text{ A}$ $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 14. Test circuit for gate charge behavior)	-	10	-	nC
Q_{gs}	Gate-source charge		-	1.5	-	nC
Q_{gd}	Gate-drain charge		-	8	-	nC

1. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.

2. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 525\text{ V}$, $I_D = 0.75\text{ A}$ $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see the Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	14.5	-	ns
t_r	Rise time		-	8.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	35	-	ns
t_f	Fall time		-	38.5	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	1.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	6	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 1.5 \text{ A}$, $V_{GS} = 0 \text{ V}$	-	-	1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 1.5 \text{ A}$, $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$ (see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	326	-	ns
Q_{rr}	Reverse recovery charge		-	1.19	-	μC
I_{RRM}	Reverse recovery current		-	7.3	-	A
t_{rr}	Reverse recovery time	$I_{SD} = 1.5 \text{ A}$, $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$, $T_J = 150 \text{ }^\circ\text{C}$ (see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	525	-	ns
Q_{rr}	Reverse recovery charge		-	1.83	-	μC
I_{RRM}	Reverse recovery current		-	7	-	A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

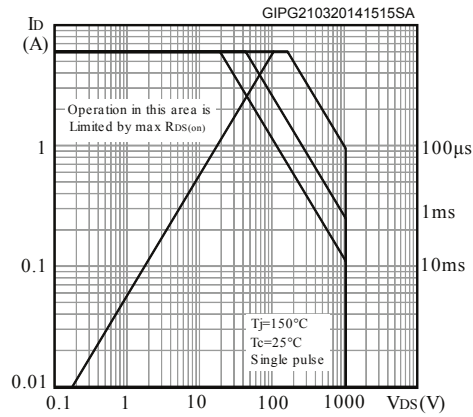
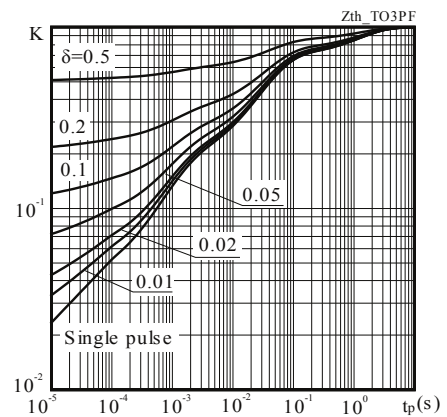
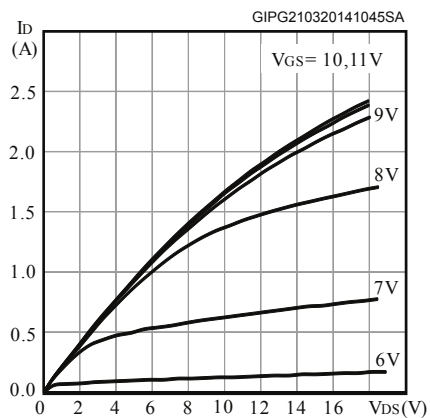
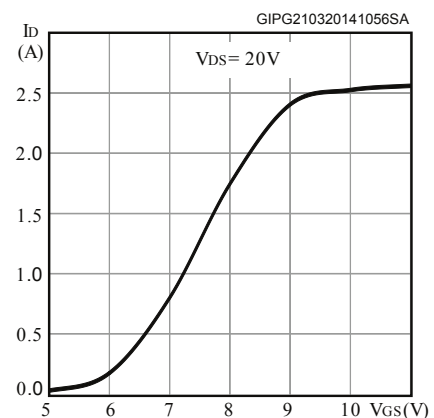
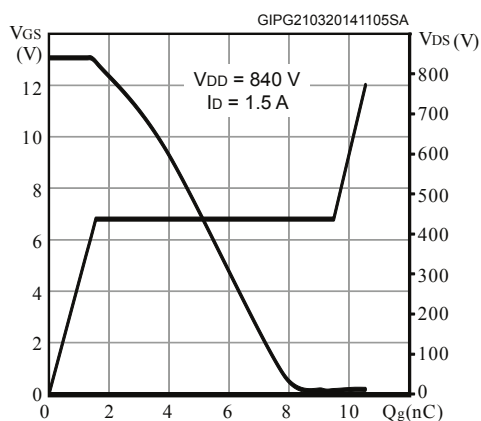
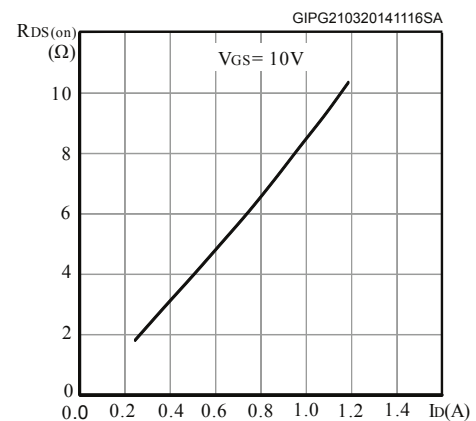
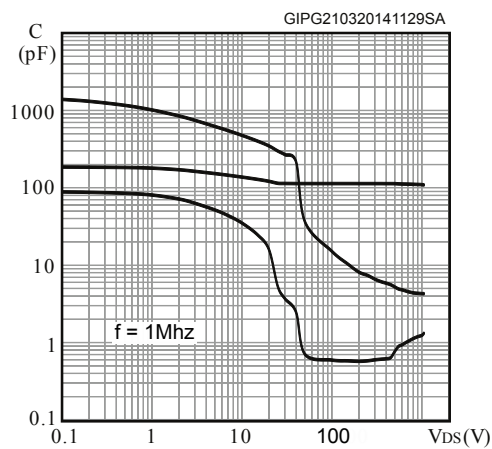
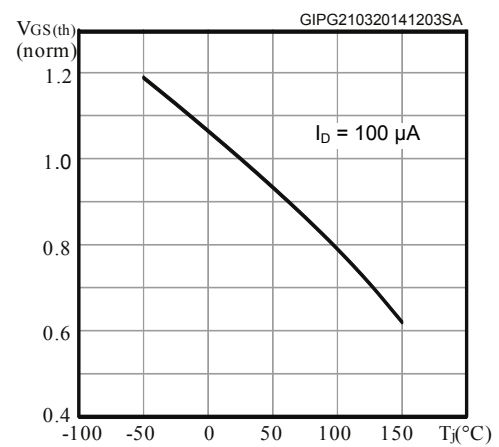
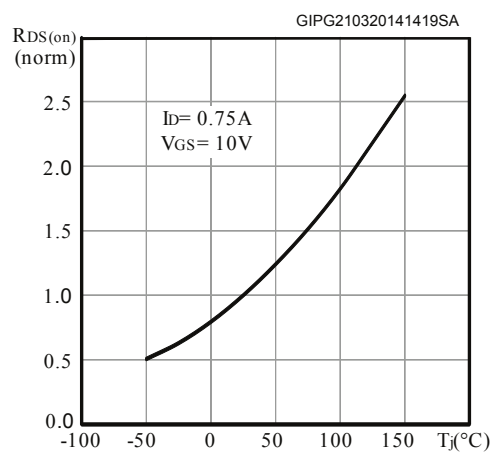
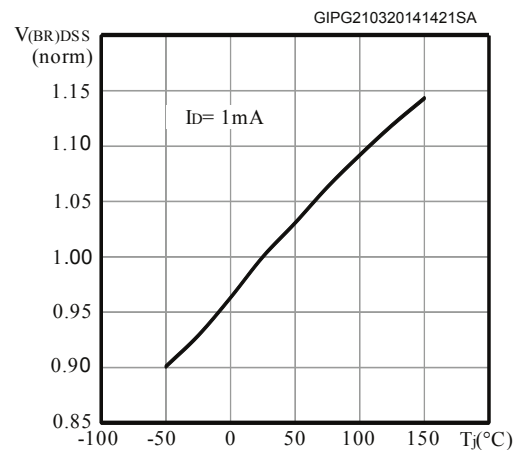
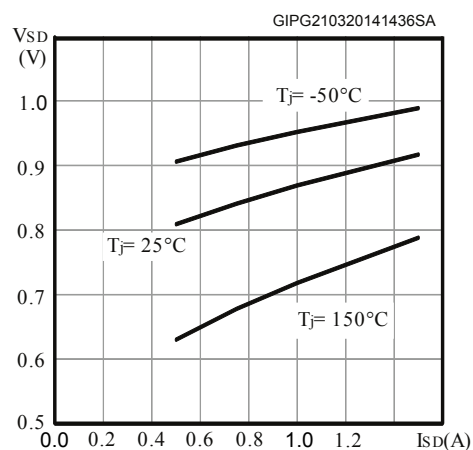
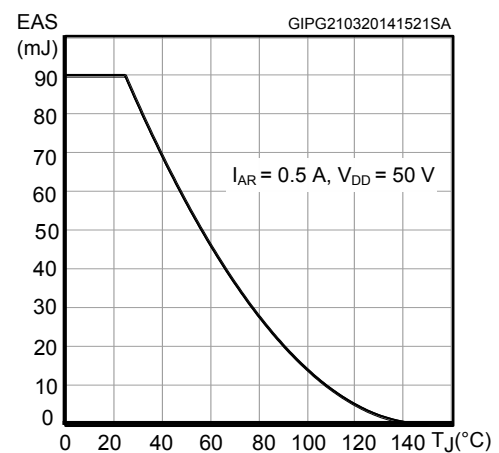
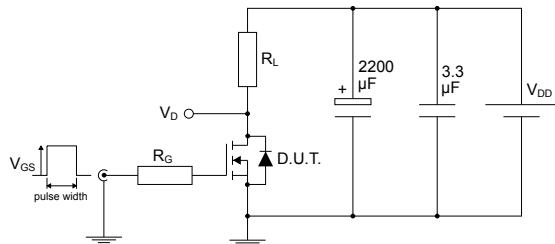
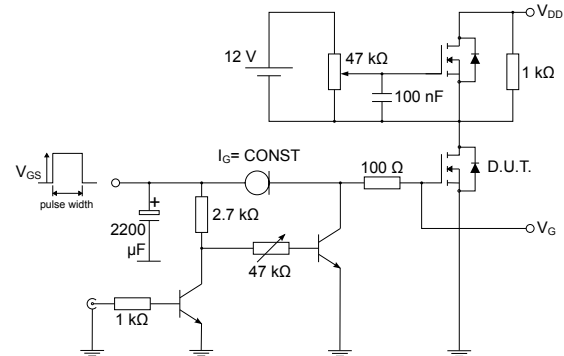
Figure 1. Safe operating area

Figure 2. Normalized transient thermal impedance

Figure 3. Typical output characteristics

Figure 4. Typical transfer characteristics

Figure 5. Typical gate charge characteristics

Figure 6. Typical drain-source on-resistance


Figure 7. Typical capacitance characteristics

Figure 8. Normalized gate threshold vs temperature

Figure 9. Normalized on-resistance vs temperature

Figure 10. Normalized breakdown voltage vs temperature

Figure 11. Typical reverse diode forward characteristics

Figure 12. Maximum avalanche energy vs temperature


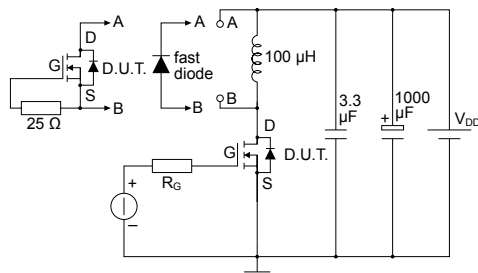
3 Test circuits

Figure 13. Test circuit for resistive load switching times


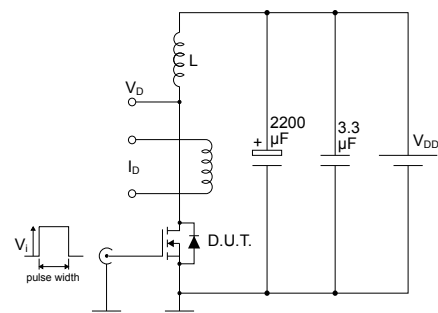
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Figure 14. Test circuit for gate charge behavior


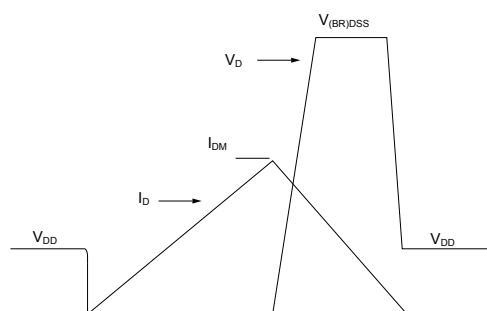
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Figure 15. Test circuit for inductive load switching and diode recovery times


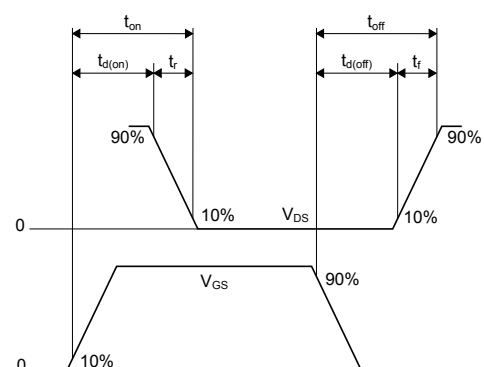
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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


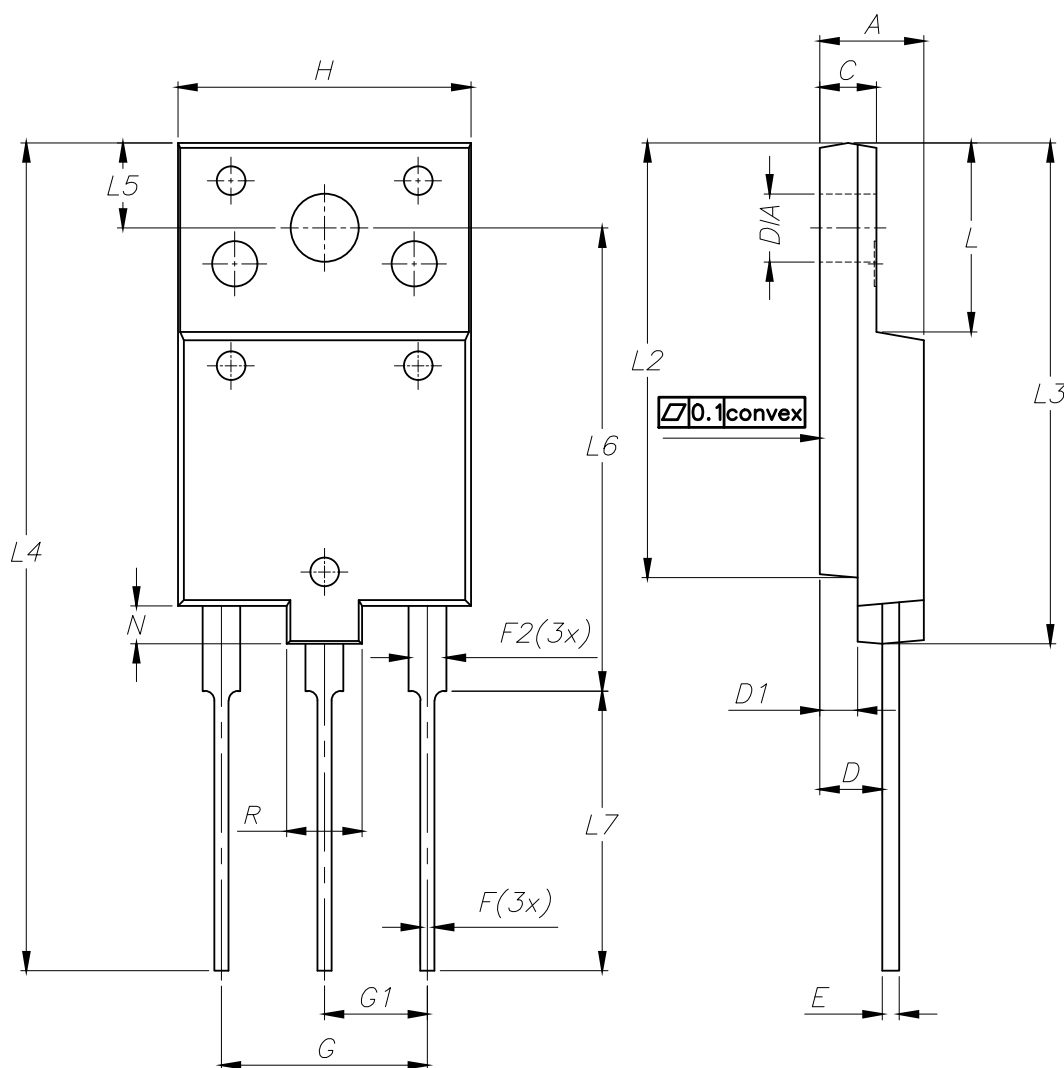
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-3PF type A package information

Figure 19. TO-3PF type A package outline



7627132_type_A_9

Table 8. TO-3PF type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	5.30		5.70
C	2.80		3.20
D	3.10		3.50
D1	1.80		2.20
E	0.80		1.00
F	0.65		0.85
F2	1.80		2.20
G	10.80		11.00
G1	5.35	5.45	5.55
H	15.30		15.70
L	9.80	10.00	10.20
L2	22.80		23.20
L3	26.30		26.70
L4	43.60		44.00
L5	4.30		4.70
L6	24.30		24.70
L7	14.60		15.00
N	1.80		2.20
R	3.80		4.20
Dia	3.40		3.80

Revision history

Table 9. Document revision history

Date	Revision	Changes
08-May-2014		First release.
25-Mar-2026	1	Updated Section 4.1: TO-3PF type A package information . Minor text changes.

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