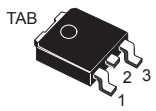
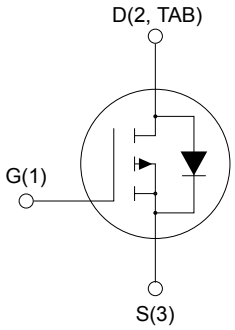
P-channel -100 V, 0.36 Ω typ., -10 A STripFET F6 Power MOSFET in a DPAK package



DPAK



AM11258v1

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD10P10F6	-100 V	0.18 Ω	-10 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Product status link
STD10P10F6

Product summary	
Order code	STD10P10F6
Marking	10P10F6
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	-100	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	-10	A
I_D	Drain current (continuous) at T_C = 100 °C	-7.5	A
I_{DM} (1)	Drain current (pulsed)	-40	A
P_{TOT}	Total power dissipation at T_C=25 °C	40	W
T_{stg}	Storage temperature range	- 55 to 175	°C
T_J	Operating junction temperature range		

1. *Pulse width limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	3.75	°C/W
R_{thJB} (1)	Thermal resistance, junction-to-board	50	°C/W

1. *When mounted on FR-4 board of 1inch², 2oz Cu t < 10 s.*

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = -250 µA	-100			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = -100 V			-1	µA
		V_{GS} = 0 V, V_{DS} = -100 V, T_C = 125 °C(1)			-10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = -250 µA	-2		-4	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = -10 V, I_D = -5 A		0.136	0.18	Ω

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = -80 V, f = 1 MHz, V_{GS} = 0 V	-	864	-	pF
C_{oss}	Output capacitance		-	45	-	pF
C_{rss}	Reverse transfer capacitance		-	25	-	pF
Q_g	Total gate charge	V_{DD} = -80 V, I_D = -10 A, V_{GS} = -10 V (see Figure 13. Gate charge test circuit)	-	16.5	-	nC
Q_{gs}	Gate-source charge		-	3.5	-	nC
Q_{gd}	Gate-drain charge		-	3.8	-	nC

Table 5. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = -80 V, I_D = -5 A, R_G = 4.7 Ω, V_{GS} = -10 V (see Figure 12. Switching times test circuit for resistive load)	-	10.5	-	ns
t_r	Rise time		-	4.8	-	ns
$t_{d(off)}$	Turn-off delay time		-	24	-	ns
t_f	Fall time		-	4.5	-	ns

Table 6. Source drain-diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = -5 A, V_{GS} = 0 V	-		-1.1	V
t_{rr}	Reverse recovery time	I_{SD} = -10 A, di/dt = 100 A/µs, V_{DD} = -80 V (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	26.5		ns
Q_{rr}	Reverse recovery charge		-	36.5		nC
I_{RRM}	Reverse recovery current		-	-2.7		A

1. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Note: For the P-channel Power MOSFET, current and voltage polarities are reversed.

Figure 1. Safe operating area

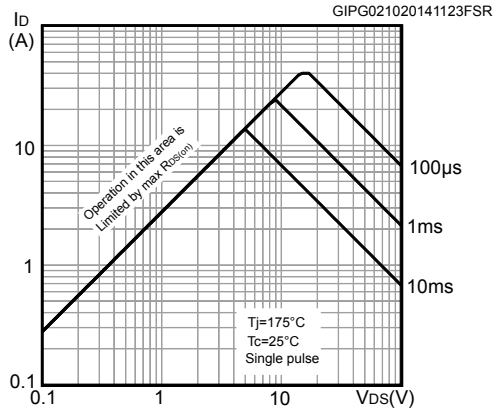


Figure 2. Normalized transient thermal impedance

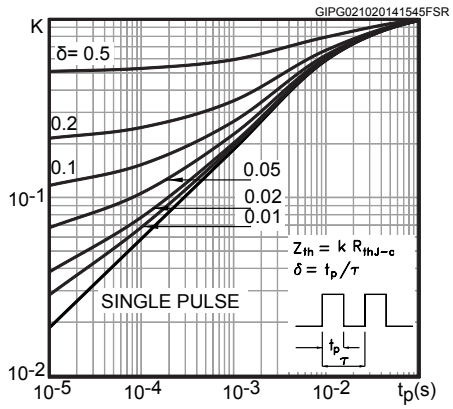


Figure 3. Typical output characteristics

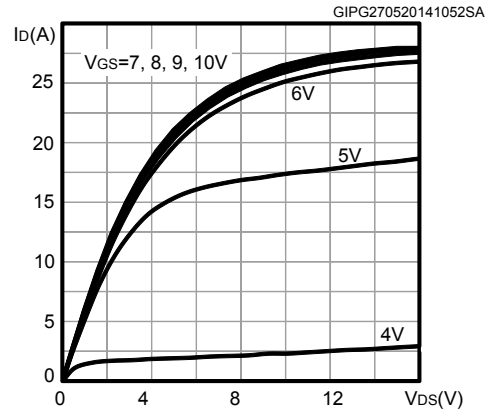


Figure 4. Typical transfer characteristics

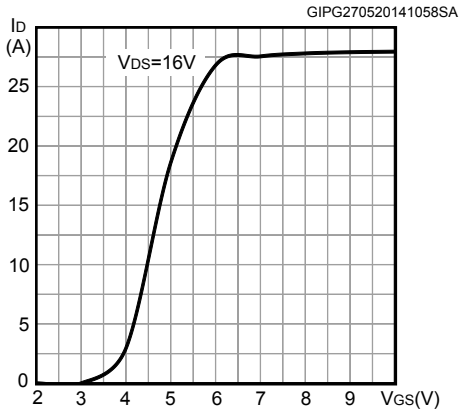


Figure 5. Typical gate charge characteristics

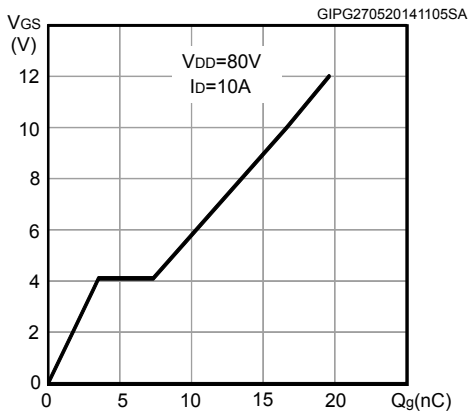


Figure 6. Typical drain-source on-resistance

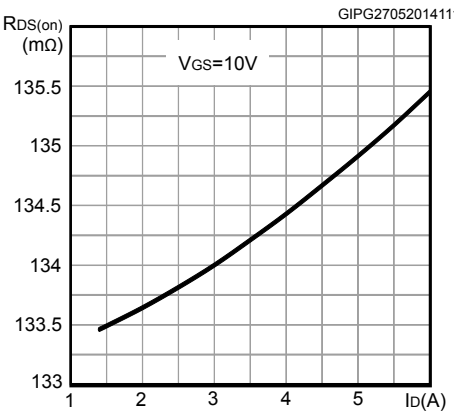


Figure 7. Typical capacitance characteristics

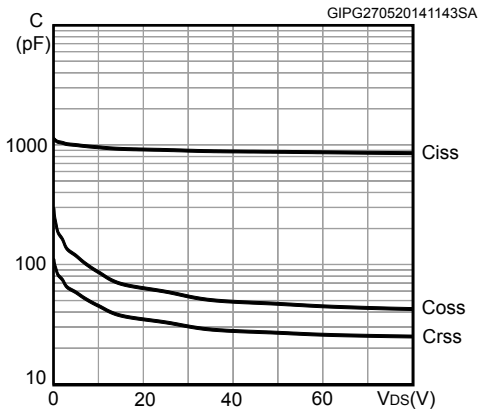


Figure 8. Normalized gate threshold vs temperature

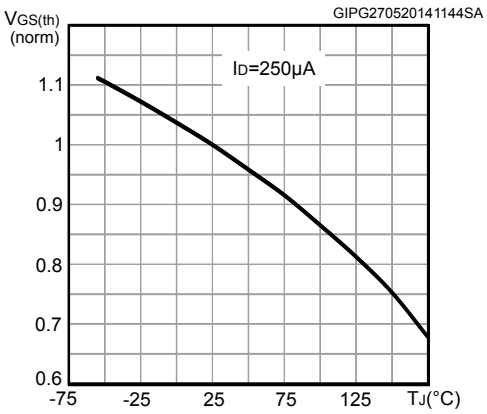


Figure 9. Normalized on-resistance vs temperature

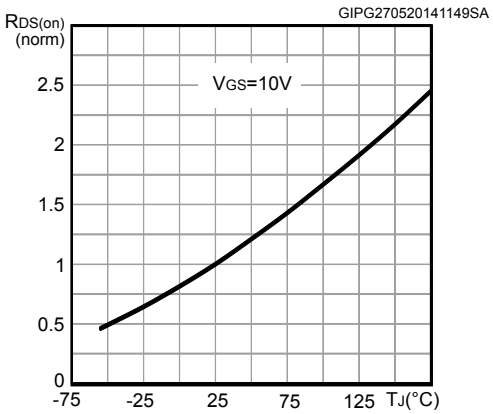


Figure 10. Normalized breakdown voltage vs temperature

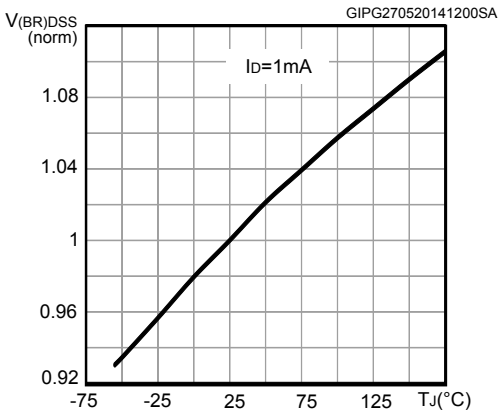
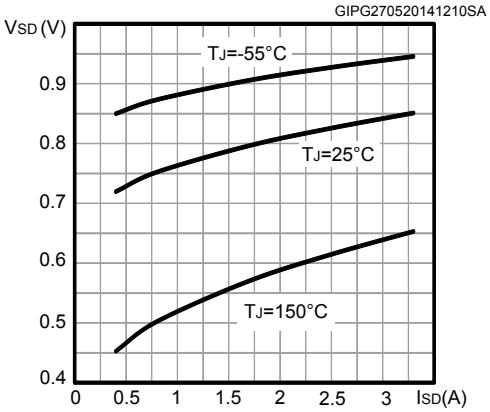


Figure 11. Typical reverse diode forward characteristics



3 Test circuits

Figure 12. Switching times test circuit for resistive load

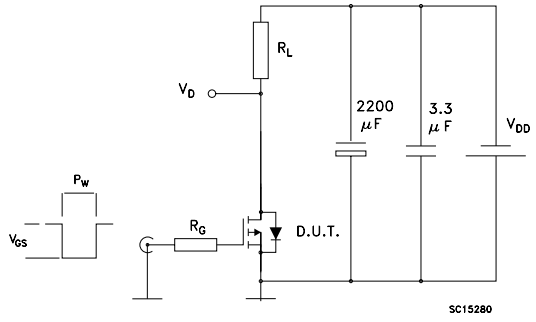


Figure 13. Gate charge test circuit

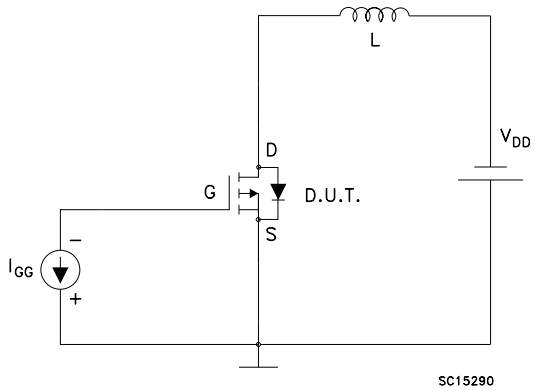
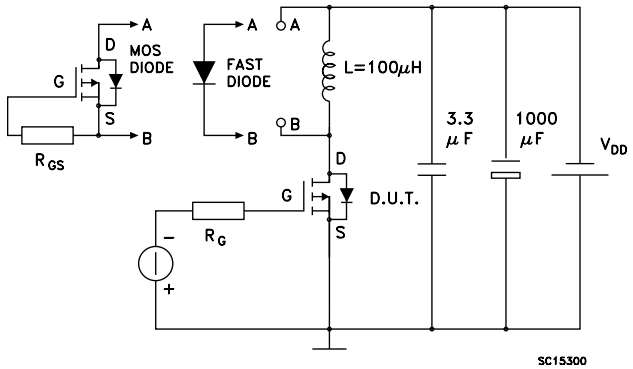


Figure 14. Test circuit for inductive load switching and diode recovery times

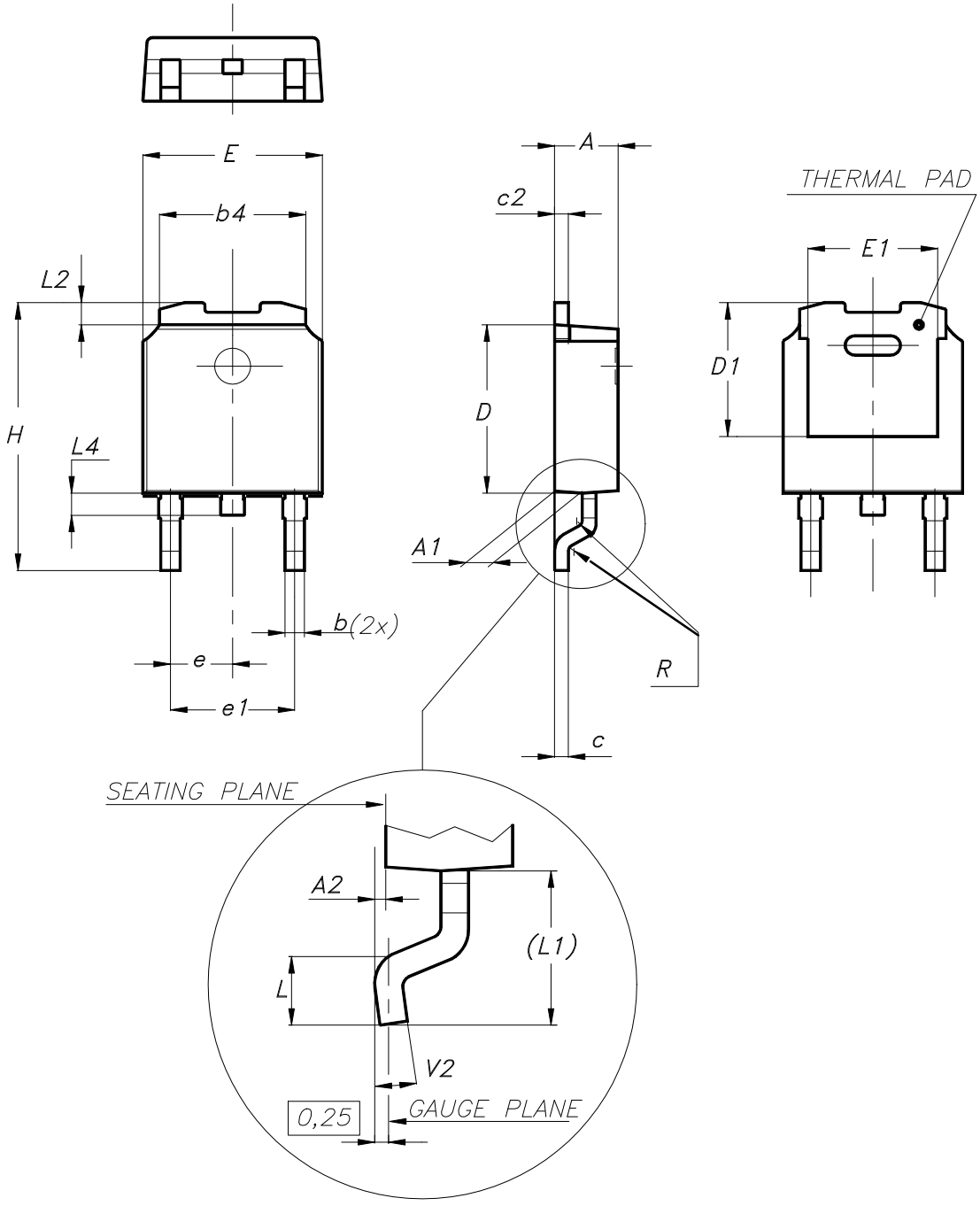


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 15. DPAK (TO-252) type A package outline



0068772_A_30

Table 7. **DPAK (TO-252) type A mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type A2 package information

Figure 16. **DPAK (TO-252) type A2 package outline**

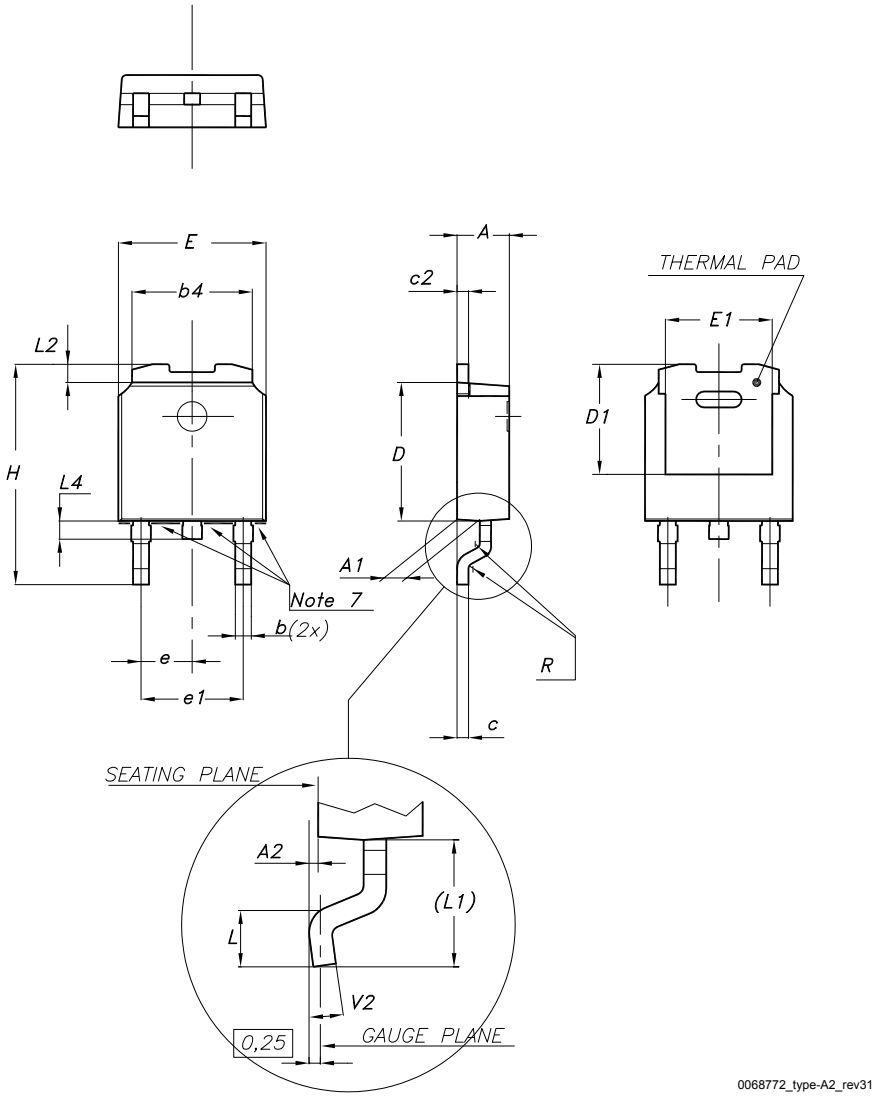
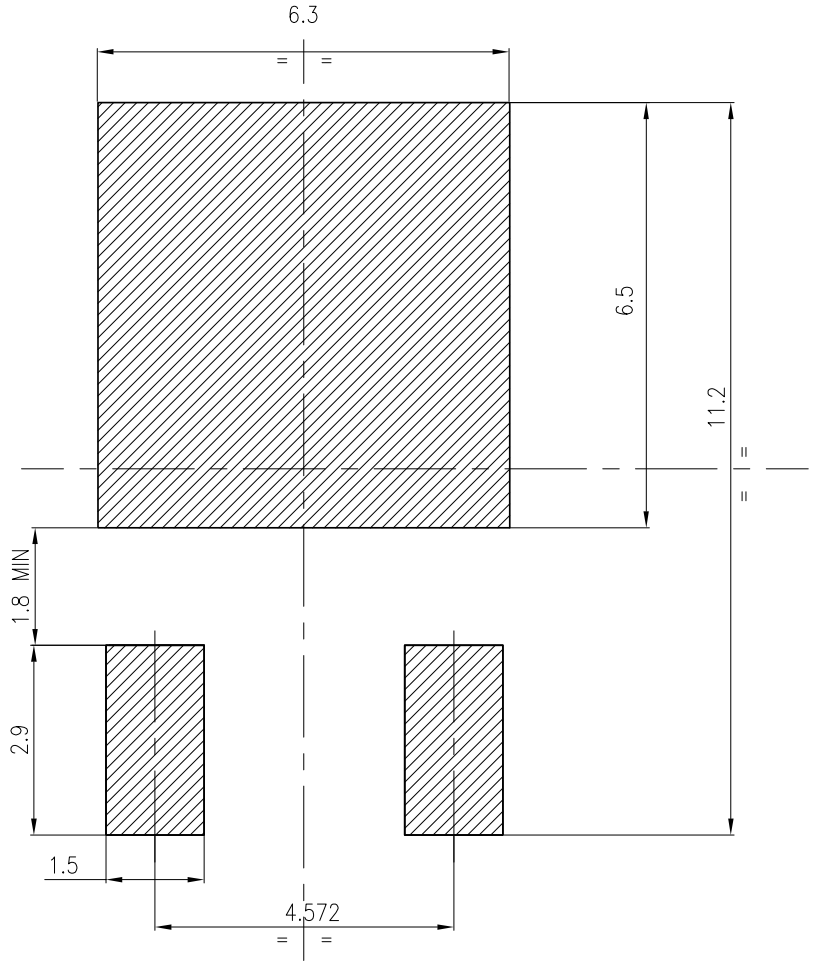


Table 8. **DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 17. **DPAK (TO-252) recommended footprint (dimensions are in mm)**



4.3 DPAK (TO-252) packing information

Figure 18. **DPAK (TO-252) tape outline**

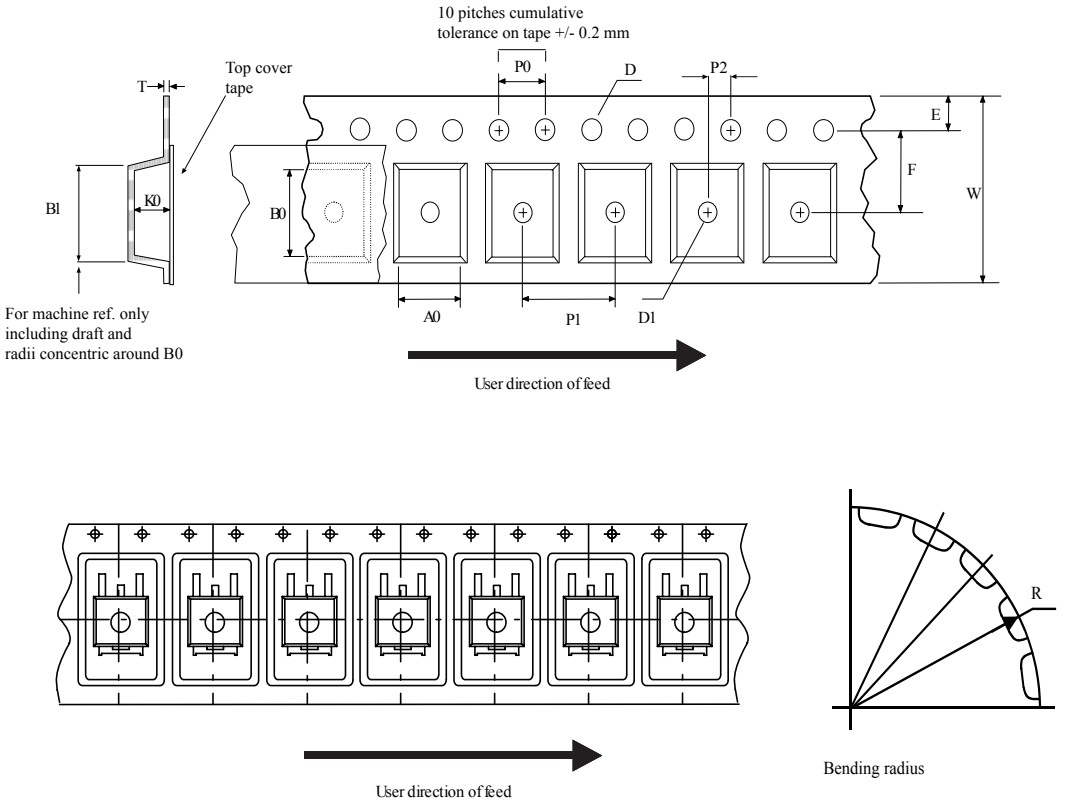
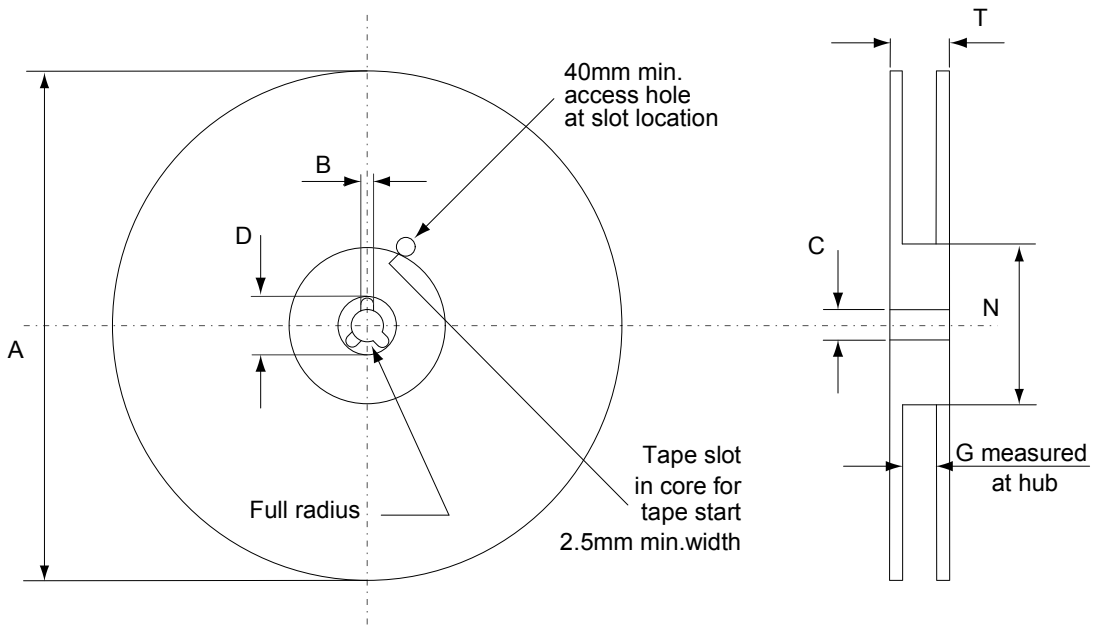


Figure 19. **DPAK (TO-252) reel outline**



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Table 9. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
20-May-2014	1	First release.
02-Oct-2014	2	Document status promoted from preliminary to production data Added *Section 2.1: "Electrical characteristics (curves)".*
26-Apr-2022	3	Updated Section 4.1 DPAK (TO-252) type A package information Added Section 4.2 DPAK (TO-252) type A2 package information Minor text changes.

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