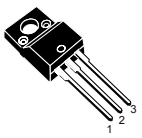
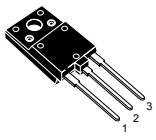
STF12N120K5, STFW12N120K5

Datasheet

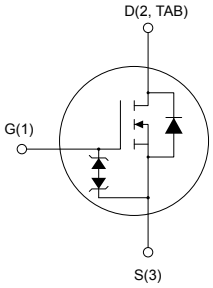
N-channel 1200 V, 620 mΩ typ. 12 A MDmesh K5 Power MOSFETs in TO-220FP and TO-3PF packages



TO-220FP



TO-3PF



AM01476v1_tab

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STF12N120K5	1200 V	690 mΩ	12 A
STFW12N120K5			

- Very low FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Product status links
STF12N120K5
STFW12N120K5

Product summary	
Order code	**STF12N120K5**
Marking	12N120K5
Package	TO-220FP
Packing	Tube
Order code	**STFW12N120K5**
Marking	12N120K5
Package	TO-3PF
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP	TO-3PF	
V_{DS}	Drain-source voltage	1200		V
V_{GS}	Gate-source voltage	±30		V
I_D	Drain current (continuous) at T_C = 25 °C	12		A
	Drain current (continuous) at T_C = 100 °C	7.6		
I_{DM}(1)	Drain current (pulsed)	48		A
P_{TOT}	Total power dissipation at T_C = 25 °C	40	63	W
dv/dt(2)	Peak diode recovery voltage slope	4.5		V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C = 25 °C)	2.5	3.5	kV
T_{stg}	Storage temperature range	-55 to 150		°C
T_J	Maximum operating junction temperature	150		°C

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 12 A, di/dt ≤ 100 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$.*
3. *V_{DS} ≤ 960 V.*

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220FP	TO-3PF	
R_{thJC}	Thermal resistance, junction-to-case	3.1	1.98	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	50	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	4	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	215	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	1200			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 1200 V			1	µA
		V_{GS} = 0 V, V_{DS} = 1200 V, T_C = 125 °C (1)			50	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 6 A		620	690	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 kHz, V_{GS} = 0 V	-	1370	-	pF
C_{oss}	Output capacitance		-	110	-	pF
C_{rss}	Reverse transfer capacitance		-	0.6	-	pF
$C_{o(tr)}$ (1)	Equivalent capacitance, time-related	V_{DS} = 0 to 960 V, V_{GS} = 0 V	-	128	-	pF
$C_{o(er)}$ (2)	Equivalent capacitance, energy-related		-	42	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	3.5	-	Ω
Q_g	Total gate charge	V_{DD} = 960 V, I_D = 6 A, V_{GS} = 0 to 10 V (see Figure 17. Test circuit for gate charge behavior)	-	44.2	-	nC
Q_{gs}	Gate-source charge		-	7.3	-	nC
Q_{gd}	Gate-drain charge		-	30	-	nC

1. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
2. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 600 V, I_D = 6 A, R_G = 4.7 Ω , V_{GS} = 10 V (see Figure 19. Unclamped inductive load test circuit)	-	23	-	ns
t_r	Rise time		-	11	-	ns
$t_{d(off)}$	Turn-off delay time		-	68.5	-	ns
t_f	Fall time		-	18.5	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
I_{SDM}(1)	Source-drain current (pulsed)		-		48	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 12 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	630		ns
Q_{rr}	Reverse recovery charge		-	12.6		µC
I_{RRM}	Reverse recovery current		-	40		A
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	892		ns
Q_{rr}	Reverse recovery charge		-	15.6		µC
I_{RRM}	Reverse recovery current		-	35		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220FP

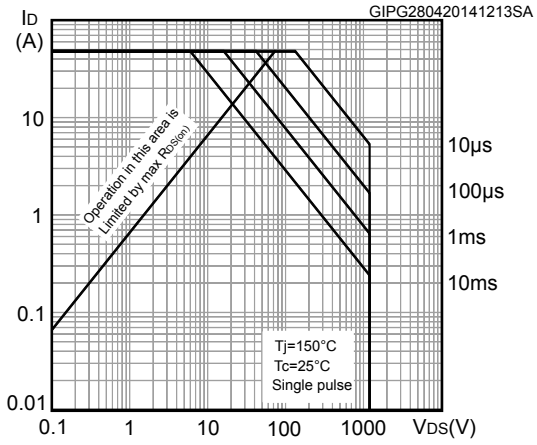


Figure 2. Normalized transient thermal impedance for TO-220FP

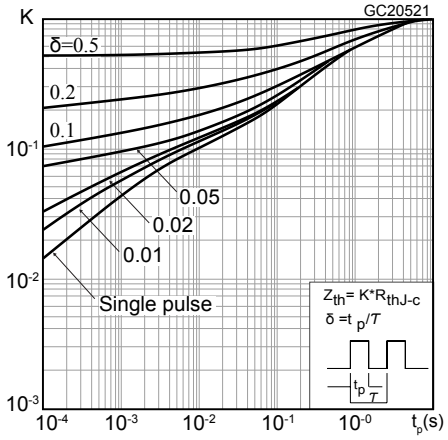


Figure 3. Safe operating area for TO-3PF

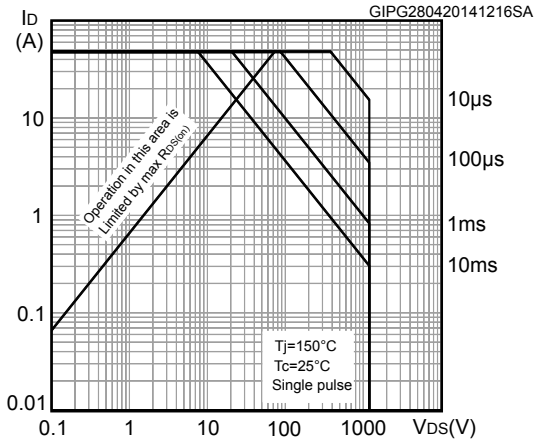


Figure 4. Normalized transient thermal impedance for TO-3PF

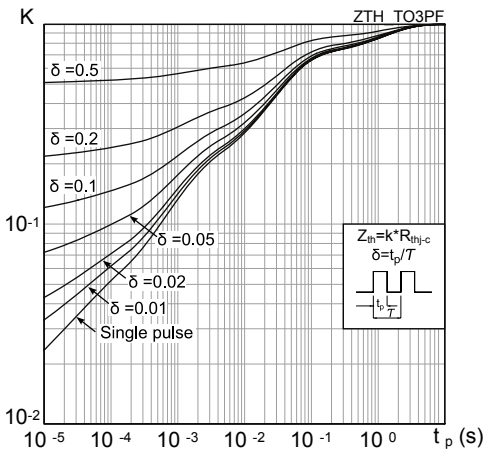


Figure 5. Typical output characteristics

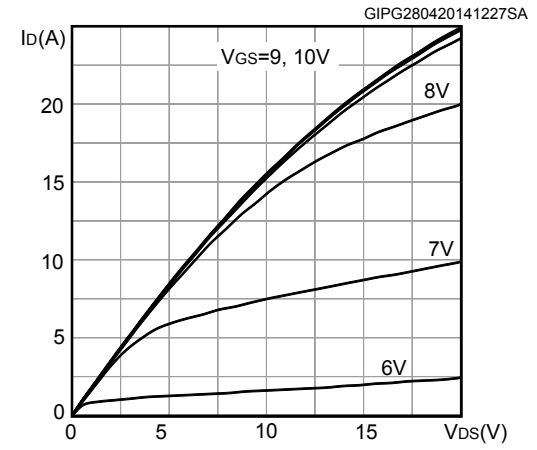


Figure 6. Typical transfer characteristics

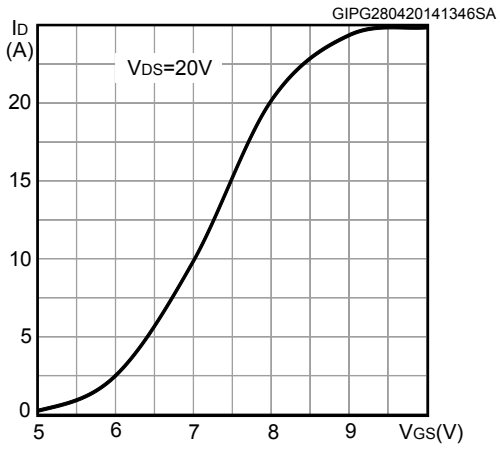


Figure 7. Typical gate charge characteristics

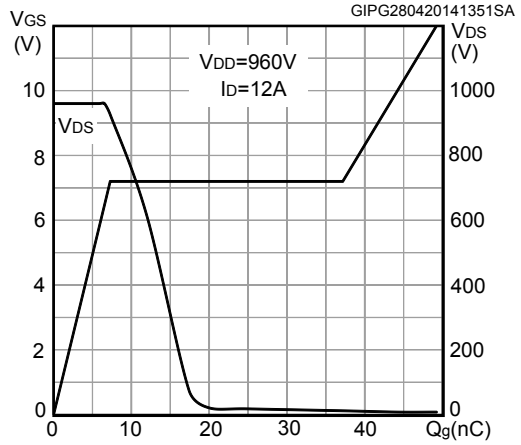


Figure 8. Typical drain-source on-resistance

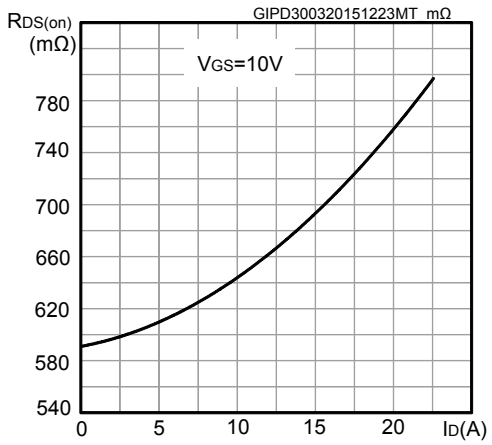


Figure 9. Typical capacitance characteristics

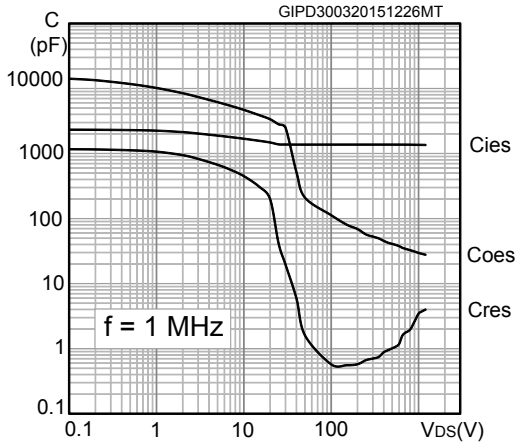


Figure 10. Normalized gate threshold vs temperature

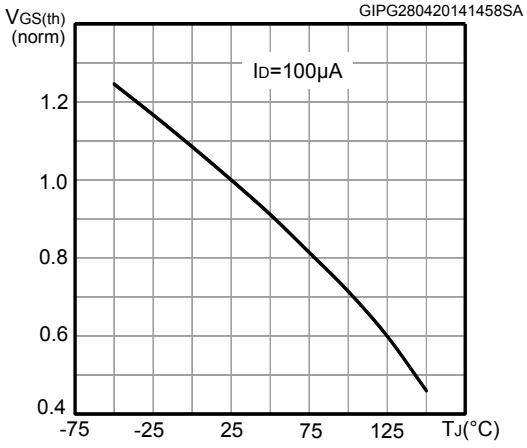


Figure 11. Normalized on-resistance vs temperature

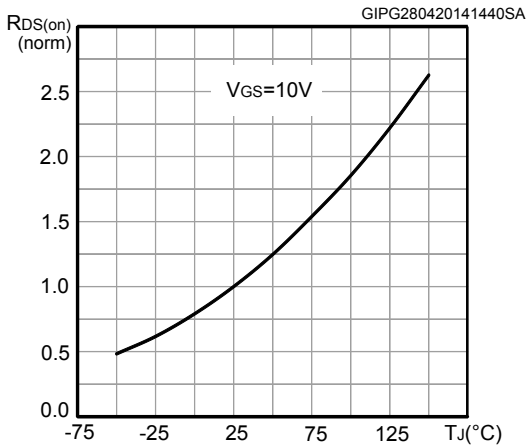


Figure 12. Normalized breakdown voltage vs temperature

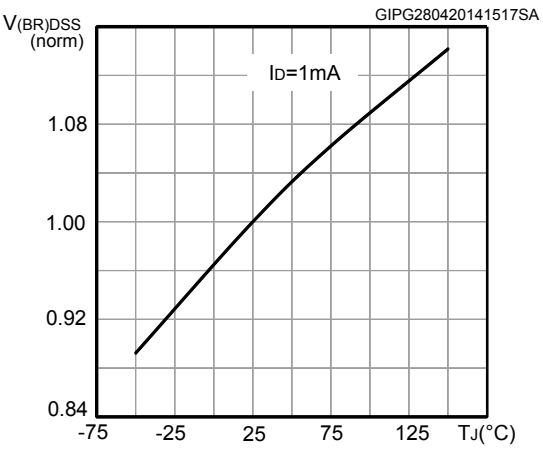


Figure 13. Typical output capacitance stored energy

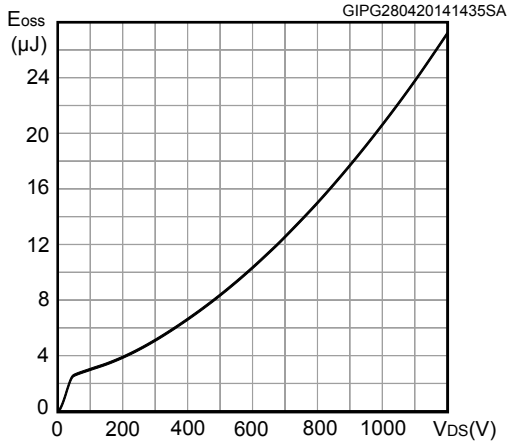


Figure 14. Typical reverse diode forward characteristics

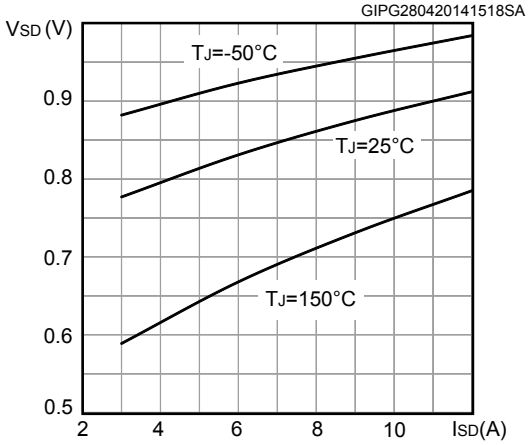
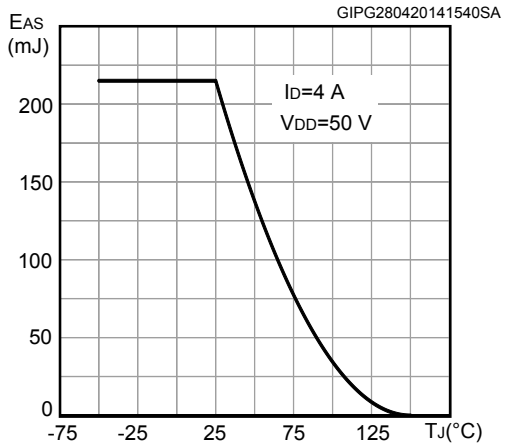
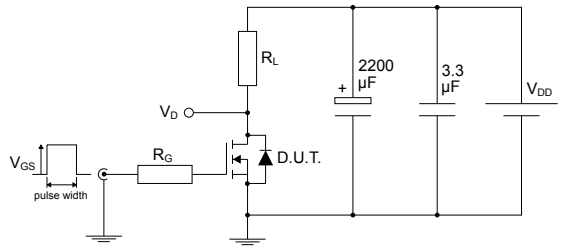


Figure 15. Maximum output capacitance stored energy



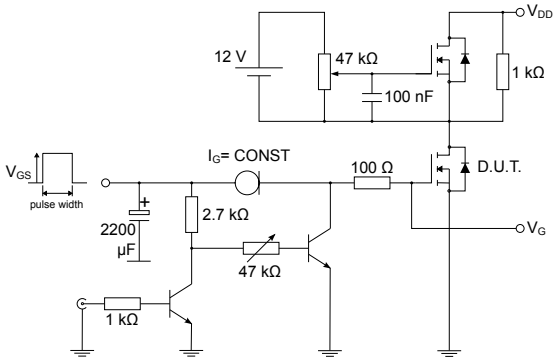
3 Test circuits

Figure 16. Test circuit for resistive load switching times



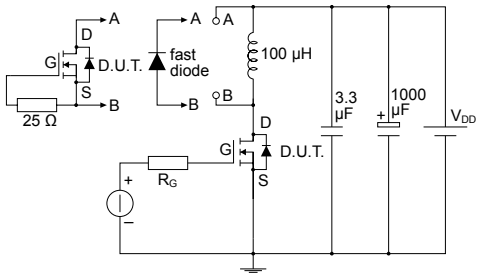
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Figure 17. Test circuit for gate charge behavior



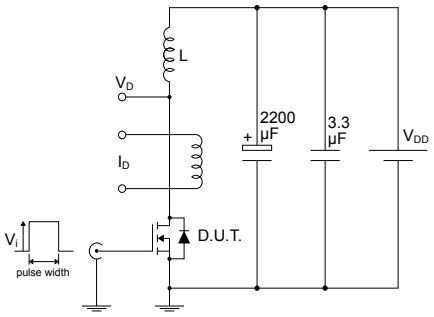
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Figure 18. Test circuit for inductive load switching and diode recovery times



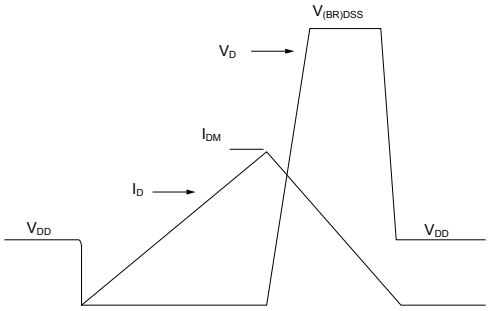
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Figure 19. Unclamped inductive load test circuit



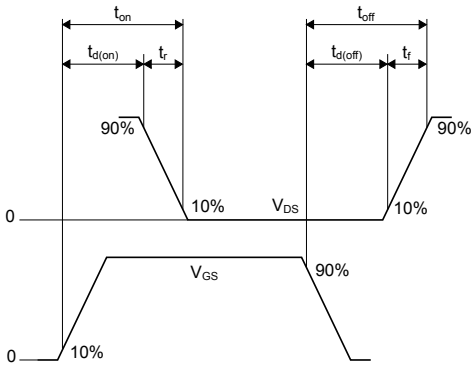
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Figure 20. Unclamped inductive waveform



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Figure 21. Switching time waveform



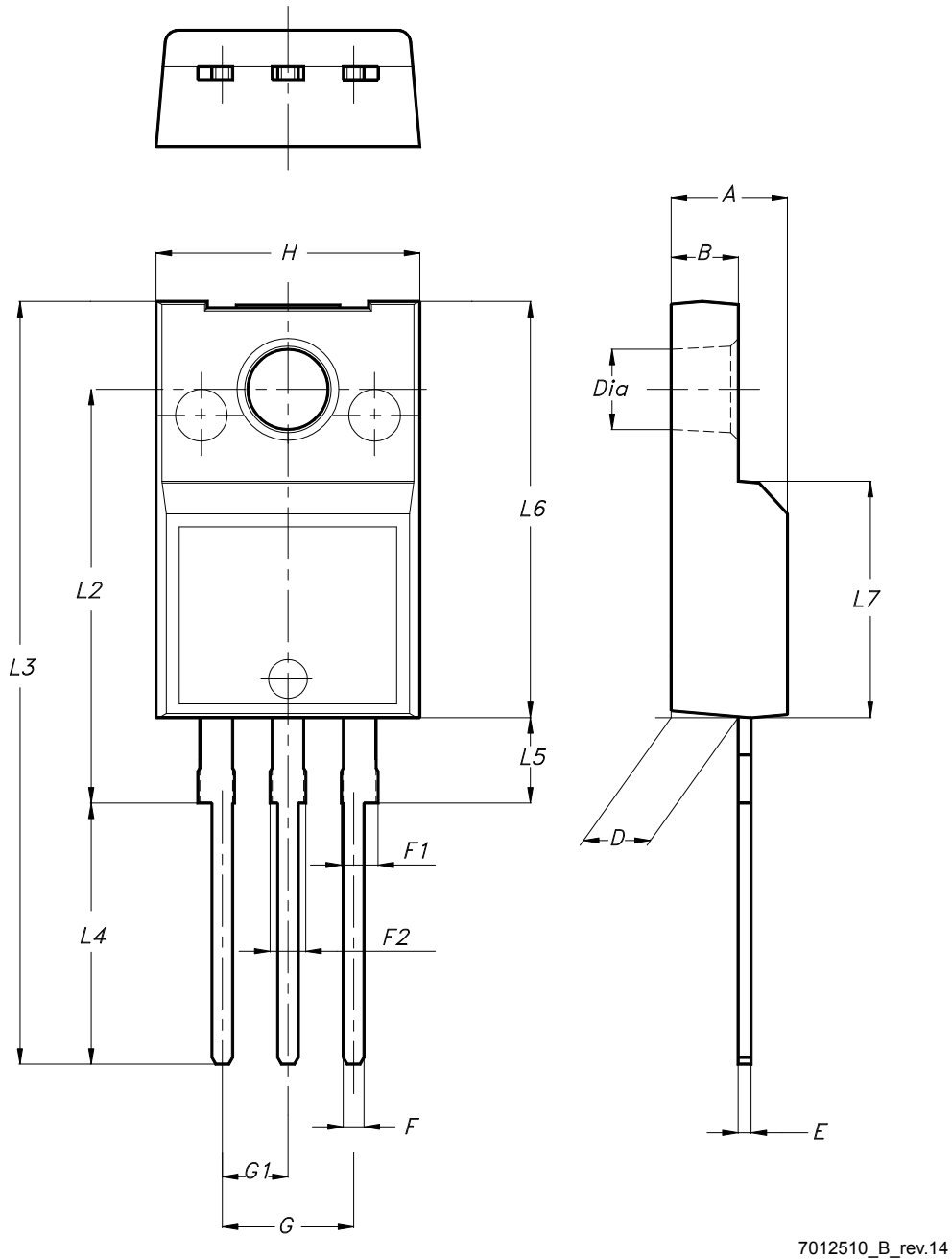
AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP type B package information

Figure 22. TO-220FP type B package outline



7012510_B_rev.14

Table 8. **TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.2 TO-3PF type A package information

Figure 23. **TO-3PF type A package outline**

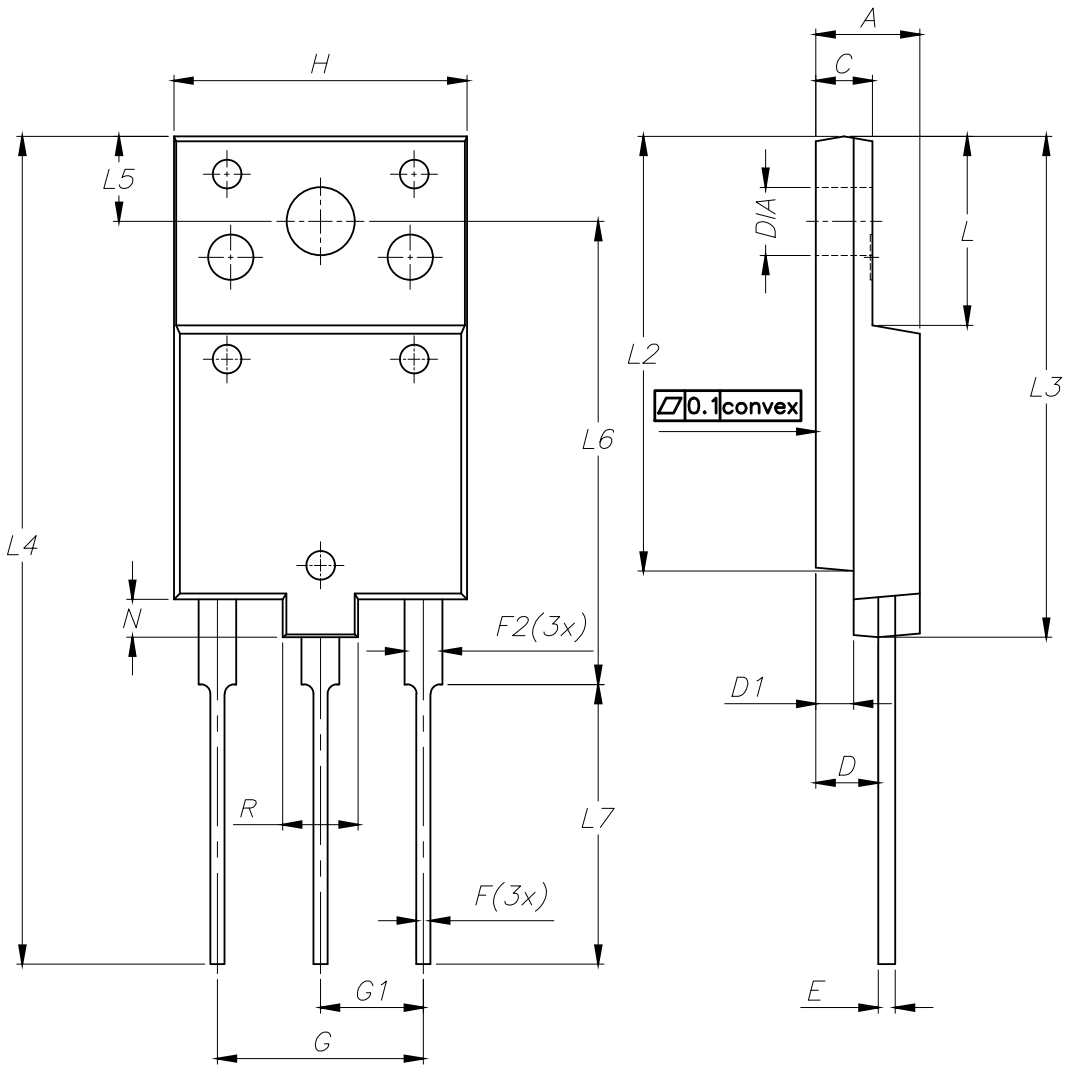


Table 9. **TO-3PF type A mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	5.30		5.70
C	2.80		3.20
D	3.10		3.50
D1	1.80		2.20
E	0.80		1.00
F	0.65		0.85
F2	1.80		2.20
G	10.80		11.00
G1	5.35	5.45	5.55
H	15.30		15.70
L	9.80	10.00	10.20
L2	22.80		23.20
L3	26.30		26.70
L4	43.60		44.00
L5	4.30		4.70
L6	24.30		24.70
L7	14.60		15.00
N	1.80		2.20
R	3.80		4.20
Dia	3.40		3.80

4.3 TO-3PF type B package information

Figure 24. **TO-3PF type B package outline**

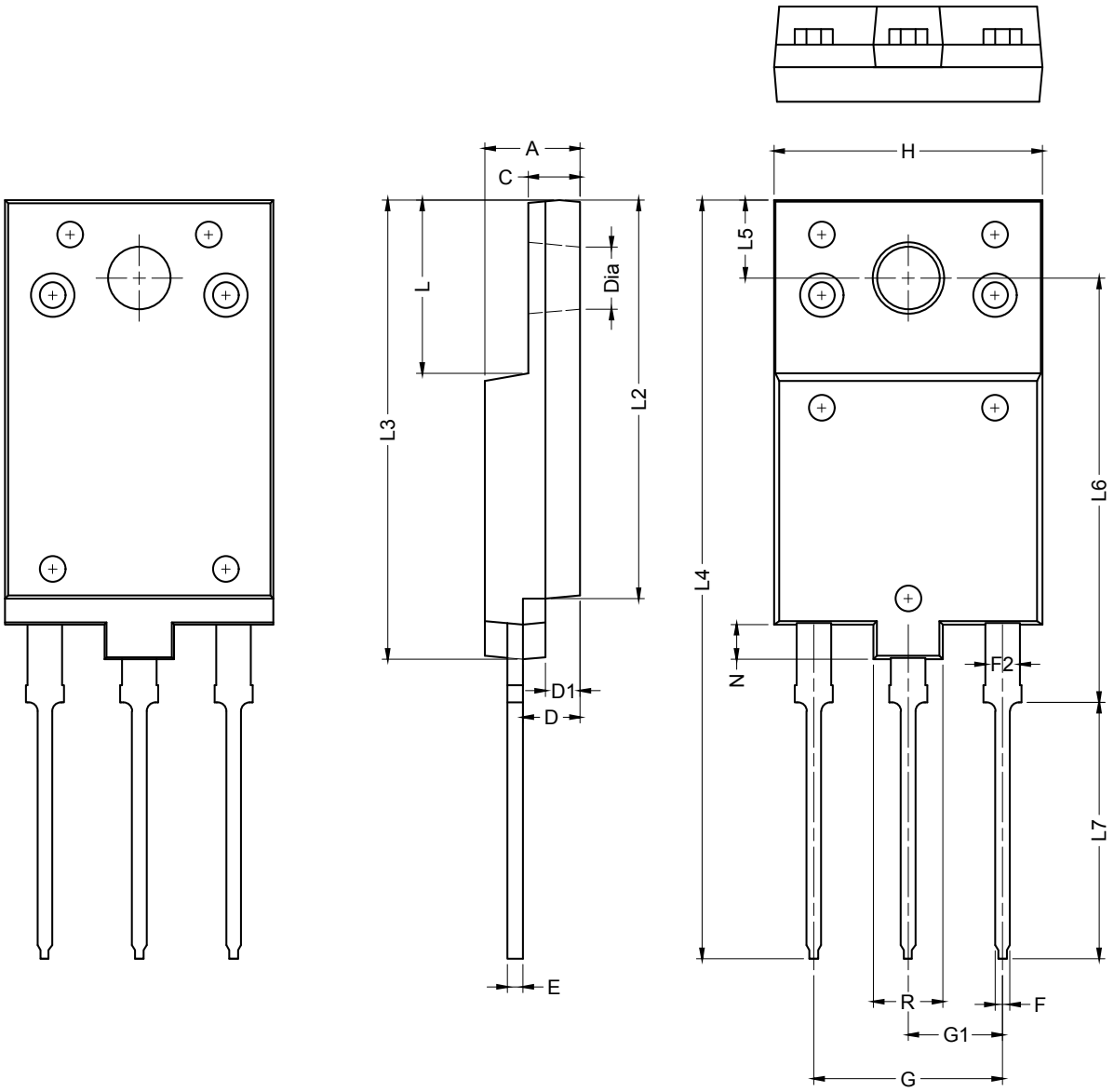


Table 10. **TO-3PF type B mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	5.30	5.50	5.70
C	2.80	3.00	3.20
D	3.10	3.30	3.50
D1	1.80	2.00	2.20
E	0.80	0.95	1.10
F	0.65	0.80	0.95
F2	1.80	2.00	2.20
G	10.30	10.90	11.50
G1		5.45	
H	15.30	15.50	15.70
L	9.80	10.00	10.20
L2	22.80	23.00	23.20
L3	26.30	26.50	26.70
L4	43.20	43.80	44.40
L5	4.30	4.50	4.70
L6	24.30	24.50	24.70
L7	14.60	14.80	15.00
N	1.80	2.00	2.20
R	3.80	4.00	4.20
Dia	3.40	3.60	3.80

Revision history

Table 11. **Document revision history**

Date	Revision	Changes
22-May-2014	1	First release. Part number (STFW12N120K5) previously included in datasheet DocID022133
11-May-2015	2	Updated title, features and description. Updated *Table 4.: On/off states* and *Table 5.: Dynamic*. Updated *Figure 9.: Static drain-source on-resistance* and *Figure 10.: Capacitance variations* Minor text changes.
16-Set-2025	3	Updated Section 4: Package information. Minor text changes.

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