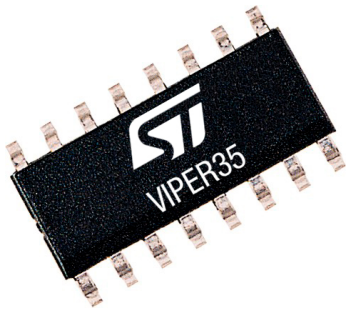
VIPER35

Datasheet

Quasi-resonant high performance off line high voltage converter



SO 16 N

Product status link

VIPER35

Product label

SUSTAINABLE TECHNOLOGY

Features

- 800 V avalanche-rugged power MOSFET allowing ultra wide range input V_{AC} to be achieved
- Embedded HV start-up and senseFET
- Built-in soft-start
- Quasi-resonant current mode PWM controller with drain current limit (I_{Dlim})
- Multifunction ZCD pin:
  - Zero-current detection
  - OCP threshold ($_{IDlim}$) setup
  - Output OVP (auto-restart)
  - Feed-forward compensation
- Support isolated flyback topology with optocoupler
- Frequency limit:
  - 136 kHz (L type), 225 kHz (H type)
- Less than 30 mW @ 230 V_{AC} in no-load condition
- Brown-out set through resistor divider
- Short-circuit protection (auto-restart)
- Hysteretic thermal shutdown

Application

- Auxiliary power supply
- Adapter/charger for PDA, camcorders, shavers, tablet, video games, STB
- Supplies for industrial systems, metering, appliances

Description

VIPER35 is a high voltage converter, which smartly integrates an 800 V rugged power MOSFET with a quasi-resonant current mode PWM control. This IC meets severe energy saving standards as it has very low consumption and operates in burst mode under light load conditions.

The VIPER35 features the brown-out enabling the IC to set the switch-off and switch-on threshold independently one of each other. The quasiresonant operation reduces the level of EMI and the quantity of components in the application.

The quasi-resonant operation reduces the switching losses and improves power conversion efficiency. The device features high level protections such as: output overvoltage, shortcircuit and thermal shutdown with hysteresis.

After the removal of a fault condition, the IC is automatically restarted.

1 Block diagram

Figure 1. **Block diagram**

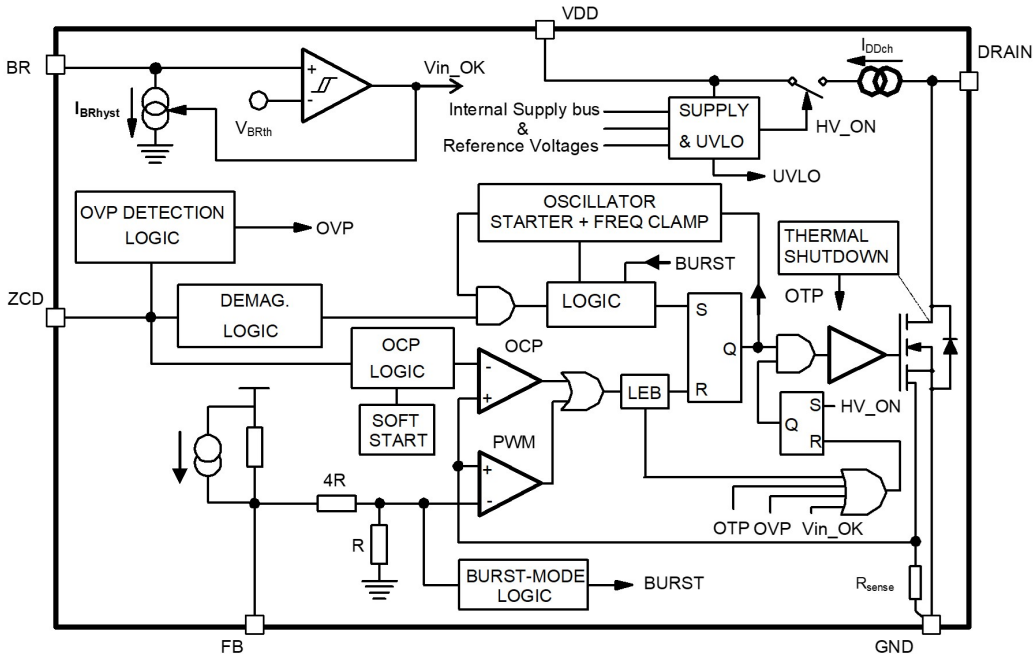
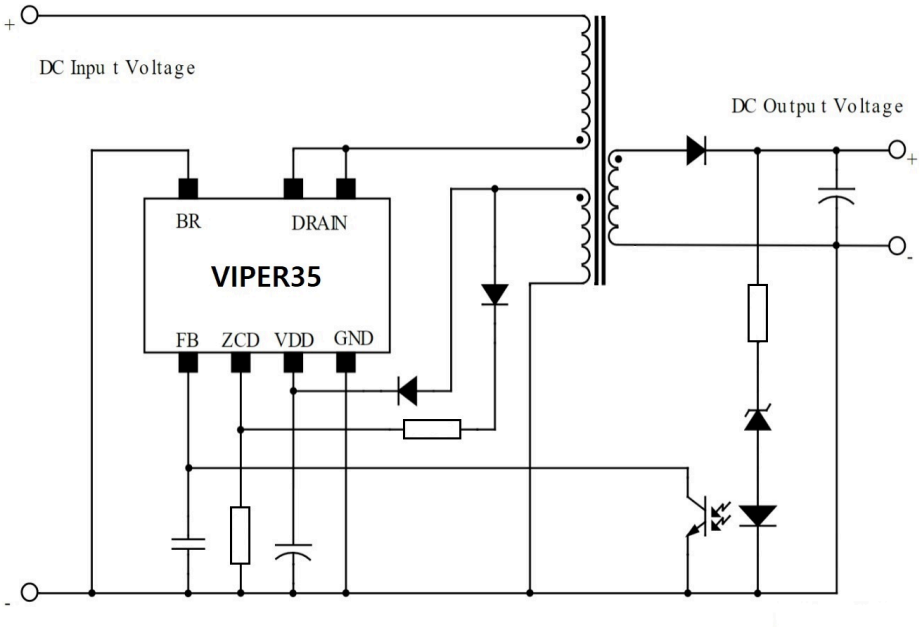


Figure 2. **Basic application schematic**



2 Typical output power

Table 1. Typical output power

Part number	230 V_{AC}		85-265 V_{AC}	
	Adapter (1)	Open frame (2)	Adapter (1)	Open frame (2)
VIPER35	20 W	22 W	15 W	16 W

1. *Typical continuous power in non-ventilated enclosed adapter measured at 50 °C ambient.*
2. *Maximum practical continuous power in an open frame design at 50 °C ambient, with adequate heatsinking.*

3 Pin description

Figure 3. **Pin description**

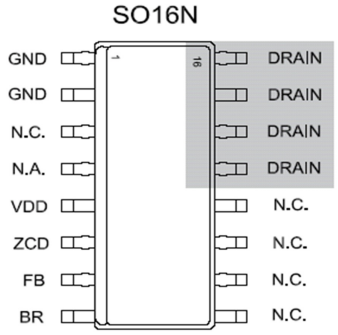


Table 2. **Pin settings**

No.	Name	Function
1,2	GND	Device ground and source ofthe power MOSFET.
3	N.C.	Not internally connected. Itcan be connected to GND.
4	N.A.	Not available for user. This pin is mechanically connected to the controller die pad of the frame. In order to improve the noise immunity it should be connected to GND (pin 1, 2).
5	VDD	Supply voltage ofthe control section. This pin provides the charging current of the external capacitor during the power-up.
6	ZCD	Multifunction pin: 1. Zero-current detection for quasi-resonant operations. 2. Drain current limit (IDlim) setup for overcurrent protection (RLIM). 3. Feed-forward compensation (RFF) setup. 4. Output overvoltage protection (resistor divider ROVP / RLIM) setup.
7	FB	Control input for duty cycle control. Internal current generator provides bias current for loop regulation. A voltage below the threshold V_{FBbm} activates the burst-mode operation. A level close to the threshold V_{FBlin} means that the cycle-by-cycle overcurrent set-point is close.
8	BR	Brown-out protection input with hysteresis. A voltage below the threshold V_{BRth} shuts down (not latch) the device and lowers the power consumption. The device operation restarts as the voltage exceeds the threshold V_{BRth} + V_{BRhyst}. It must be connected to ground when it is not used.
9 to 12	N.C.	Not internally connected. These pins must be left floating in order to get a safe clearance distance.
13 to 16	DRAIN	High voltage drain pin. The built-in high voltage switched start-up bias current is drawn from this pin. Pins connected to the metal frame facilitate heat dissipation.

4 Absolute maximum ratings and thermal data

Table 3. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DRAIN}	Drain-to-source (ground) voltage		800	V
E_{AV}	Repetitive avalanche energy (limited by T_J = 150 °C)		5	mJ
I_{AR}	Repetitive avalanche current (limited by T_J = 150 °C)		1.5	A
I_{DRAIN}	Single pulse drain current		3	A
V_{ZCD}	Input pin voltage (with I_{ZCD} = 1 mA)	-0.3	Self limited	V
V_{FB}	Input pin voltage	-0.3	5.5	V
V_{BR}	Input pin voltage (with I_{BR} = 0.25 mA)	-0.3	Self limited	V
V_{DD}	Supply voltage	-0.3	Self limited	V
I_{DD}	Input current		25	mA
P_{TOT}	Power dissipation at T_A<60 °C		1.5	W
T_J	Operating junction temperature range	-40	150	°C
T_{STG}	Storage temperature	-55	150	°C

Table 4. Thermal data

Symbol	Parameter	Max.	Unit
R_{thJP}	Thermal resistance junction pin (dissipated power = 1 W)	35	°C/W
R_{thJA}	Thermal resistance junction ambient (dissipated power = 1 W)	110	°C/W
R_{thJA}	Thermal resistance junction ambient (1) (dissipated power = 1 W)	80	°C/W

1. *When mounted on a standard single side FR4 board with 100 mm2 (0.155 sq inch) of Cu (35 µm thick).*

5 Electrical characteristics

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_J= -40 to 125 °C, VDD= 14 V (1) (unless otherwise specified)						
V_{BVDSS}	Breakdown voltage	I_{DRAIN} = 1 mA, V_{FB} = GND T_J = 25 °C	800			V
I_{OFF}	Off-state drain current	V_{DRAIN} = 800 V V_{FB} = GND, T_J = 25 °C			60	uA
$R_{DS(on)}$	Drain-source on- state resistance	I_{DRAIN} = 0.4 A, V_{FB} = 3 V V_{BR} = GND, T_J = 25 °C			4.5	Ω
		I_{DRAIN} = 0.4 A, V_{FB} = 3 V V_{BR} = GND, T_J=125 °C			9	Ω
C_{OSS}	Effective (energy related) output capacitance	V_{DRAIN} = 0 to 640 V		17		pF
Voltage						
T_J = -40 to 125 °C (unless otherwise specified)						
V_{DRAIN_START}	Drain-source start voltage		60	80	100	V
I_{DDch1}	Start-up charging current (power-up)	V_{DRAIN} = 120 V V_{BR} = GND V_{FB} = GND V_{DD} = 4 V	-2	-3	-4	mA
I_{DDch2}	Start-up charging current (auto-restart)	V_{DRAIN} = 120 V V_{BR} = GND V_{FB} = GND V_{DD} = 5 V, after fault	-0.4	-0.6	-0.8	mA
V_{DD}	Operating voltage range	After turn-on	8.5		23.5	V
$V_{DDclamp}$	Clamp voltage	I_{DD} = 20 mA	23.5			V
V_{DDon}	V_{DD} start-up threshold	V_{DRAIN} = 120 V V_{BR} = GND V_{FB} = GND	13	14	15	V
V_{DDoff}	V_{DD} undervoltage shutdown threshold		7.5	8	8.5	V
$V_{DD(RESTART)}$	V_{DD} restart voltage threshold		4	4.5	5	V
Current						
I_{DD0}	Operating supply current, notswitching	V_{FB} = GND V_{BR} = GND V_{DD} = 10 V (2)		0.6	0.7	mA
I_{DD1}	Operating supply current switching	V_{DRAIN} = 120 V V_{DD} = 16 V ZCD switching @100kHz Resistive load: 100 Ω V_{FB} = 2.5 V		2	3	m

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{DD_FAULT}	Operating supply current withprotection tripping	V_{DD} = 10 V			400	uA
I_{DDoff}	Operating supply current	V_{DD} <V_{DDoff}			270	uA
Feedback pin						
T_J = -40 to 125 °C (unless otherwise specified)						
V_{FBolp}	Overload shutdown threshold		4.5	4.8	5.2	V
V_{FBlin}	Linear dynamics upper limit		3.1	3.3	3.5	V
V_{FBbm}	Burst mode threshold	Voltage falling	0.56	0.6	0.64	V
$V_{FBbmhys}$	Burst mode hysteresis	Voltage rising		100		mV
I_{FB}	Feedback sourced current	V_{FB} = 0.3 V	-150	-215	-280	µA
		3.3 V< V_{FB}<4 V	-2.5	-3	-3.5	µA
$R_{FB(DYN)}$	Dynamic resistance	V_{FB}> 2.5 V	12		25	kΩ
H_{FB}	V_{FB}/I_D		0.5		2	V/A
ZCD pin						
V_{ZCDCLh}	Upper clamp voltage	I_{ZCD} = 1 mA	5	5.5	6	V
V_{ZCDAth}	Arming voltage threshold	Positive-going edge	0.75	0.8	0.85	V
V_{ZCDTth}	Triggering voltage threshold	Negative-going edge	0.55	0.6	0.65	V
I_{ZCD}	Internal pull-up	V_{FB} <V_{FBlin}	-7.5	-10	-12.5	µA
t_{DELAY}	Turn-on delay after ZCD trigger			300		ns
t_{BLANK}	Turn-on inhibit time after MOSFET turn- off	V_{ZCD}<1 V		6.3		µs
		V_{ZCD}>1 V		2.5		µs
Current limitation						
I_{Dlim}	Drain current limitation	V_{FB} = 4V I_{ZCD} = -10 µA T_J = 25 °C	0.95	1	1.05	A
		V_{FB} = 4 V I_{ZCD} = - 55 µA T_J = 25 °C	0.68	0.8	0.92	A
		V_{FB} = 4 V I_{ZCD} = - 105 µA T_J = 25 °C	0.55	0.65	0.75	A
t_{SS}	Soft-start time	VIPER35L			3.5	ms
		VIPER35H			4.2	ms
t_{SU}	Start-up time	VIPER35L	7.5		15	ms
		VIPER35H	9.5		18	ms
t_{ON_MIN}	Minimum turn-on time		220	400	480	ns
t_d	Propagation delay	(3)		100		ns
t_{LEB}	Leading edge blanking	(3)		300		ns
I_{D_BM}	Peak drain current during burst mode	V_{FB} = 0.6 V	120	170	220	mA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Overvoltage protection						
V_{OVP}	Overvoltage threshold		3.8	4.2	4.6	V
tSTROBE	Strobe time			2.2		µs
Oscillator section						
F_{OSClim}	Internal frequency limit	VIPER35L	122	136	150	kHz
		VIPER35H	200	225	250	kHz
$F_{STARTER}$	Starter frequency	V_{FB} = 1 V V_{ZCD} <V_{ZCDTth} t< t_{SU}		1/4 FOSClim		kHz
		V_{FB} = 1V V_{ZCD} <V_{ZCDTth} t> t_{SU}		1/8 F_{OSClim}		kHz
Brown-out protection						
V_{BRth}	Brown-out threshold	Voltage falling	0.41	0.45	0.49	A
V_{BRHyst}	Voltage hysteresis above V_{BRth}		40	50	60	mV
I_{BRHyst}	Current hysteresis		7		12	µA
$V_{BRclamp}$	Clamp voltage	I_{BR} = 250 µA		3		V
V_{DIS}	Brown-out disable voltage		50		150	mV
Thermal shutdown						
T_{SD}	Thermal shutdown temperature	(3)	150	160		°C
T_{HYST}	Thermal shutdown hysteresis	(3)		30		°C

1. *Adjust V_{DD} above V_{DDon} start-up threshold before setting 14 V*
2. *Adjust V_{DD} above V_{DDon} start-up threshold before setting 10 V.*
3. *Specification assured by design, characterization and statistical correlation.*

6 Typical electrical characteristics

Figure 4. V_{DDon} vs T_J

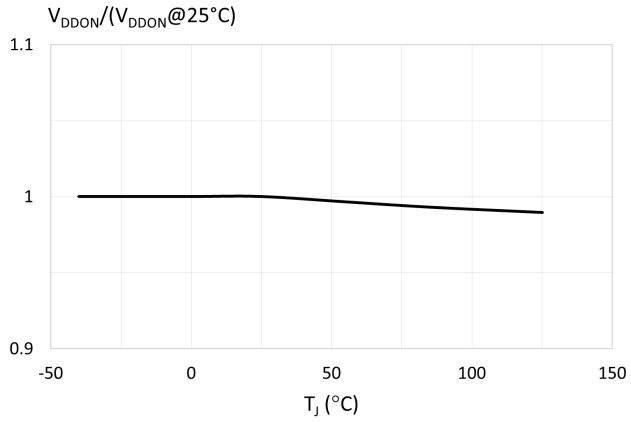


Figure 5. $V_{DD(RESTART)}$ vs T_J

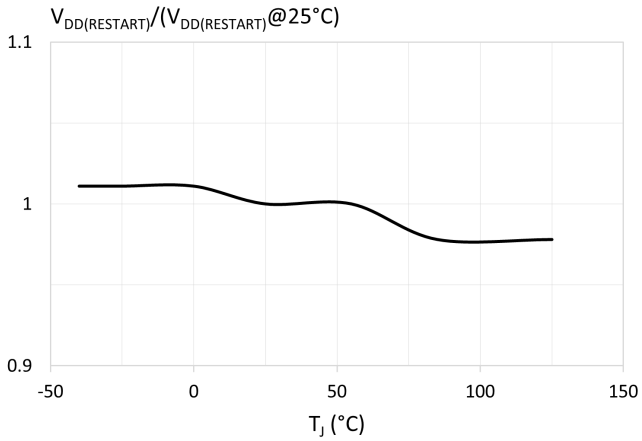


Figure 6. I_{Dlim} vs T_J

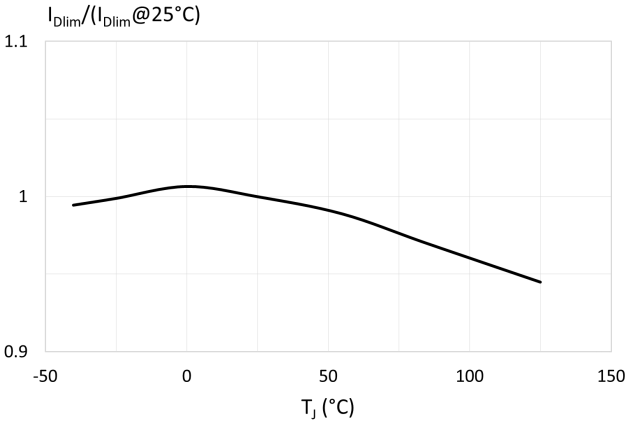


Figure 7. V_{DRAIN_START} vs T_J

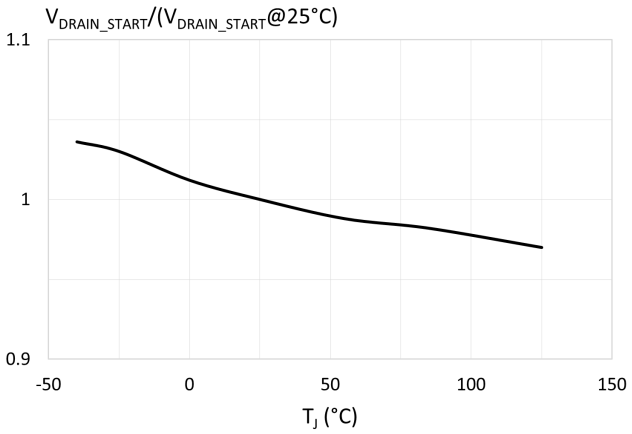


Figure 8. H_{FB} vs T_J

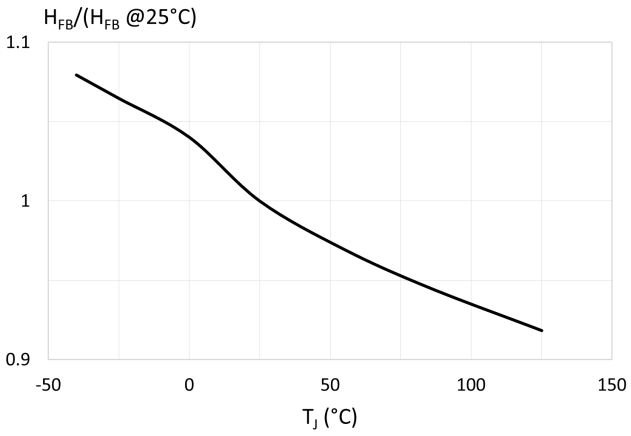


Figure 9. $V_{DD(RESTART)}$ vs T_J

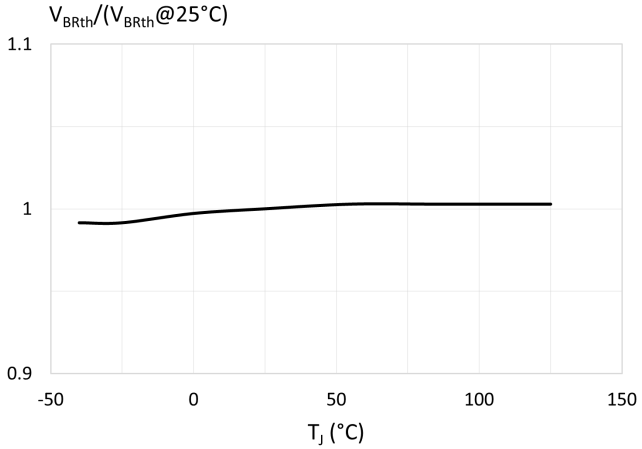


Figure 10. V_{BRhyst} vs T_J

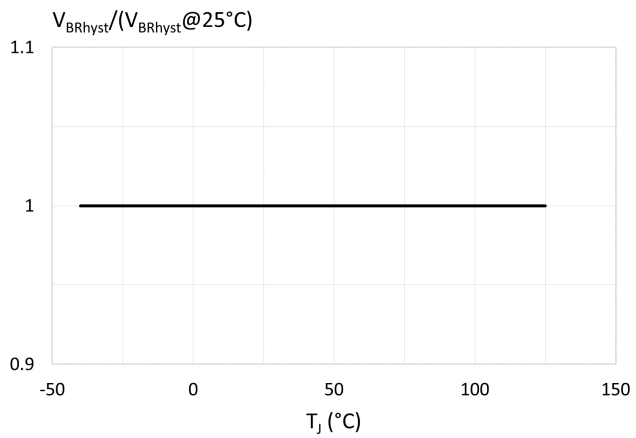


Figure 11. I_{BRhys} vs T_J

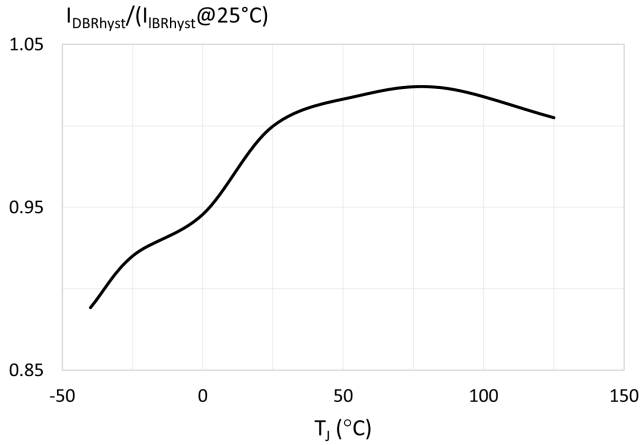


Figure 12. I_{DD0} vs T_J

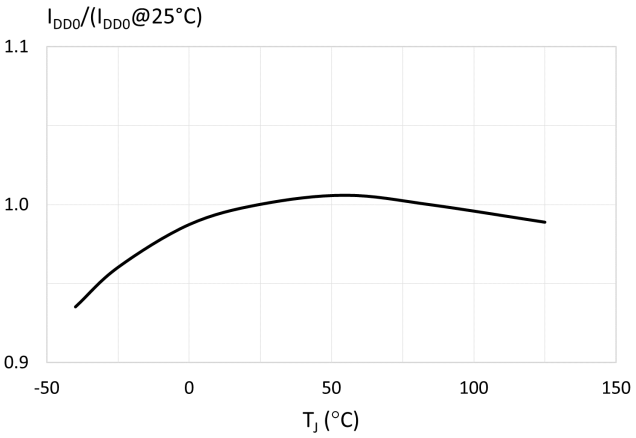


Figure 13. I_{DD1} vs T_J

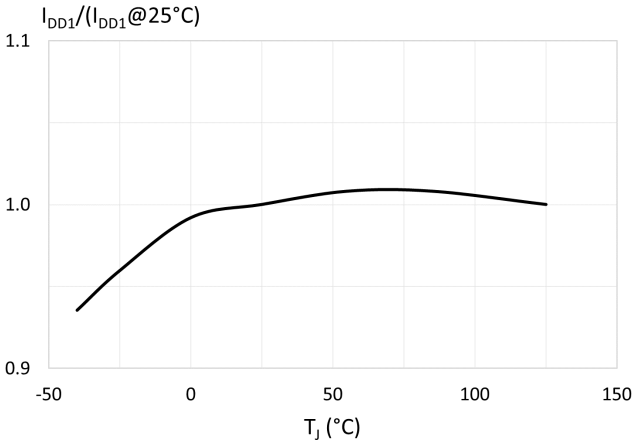


Figure 14. V_{ZCD} vs I_{ZCD}

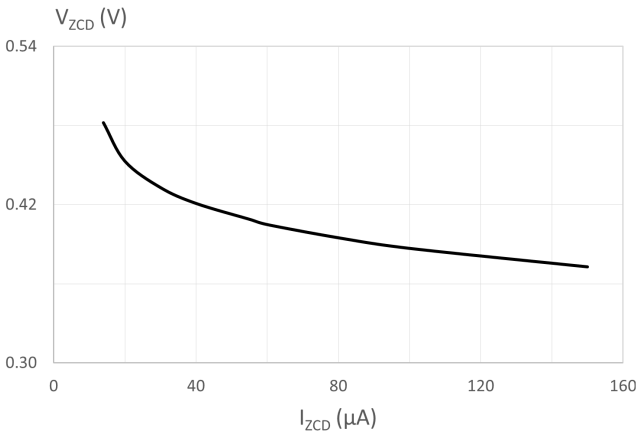


Figure 15. I_{Dlim} vs I_{ZCD}

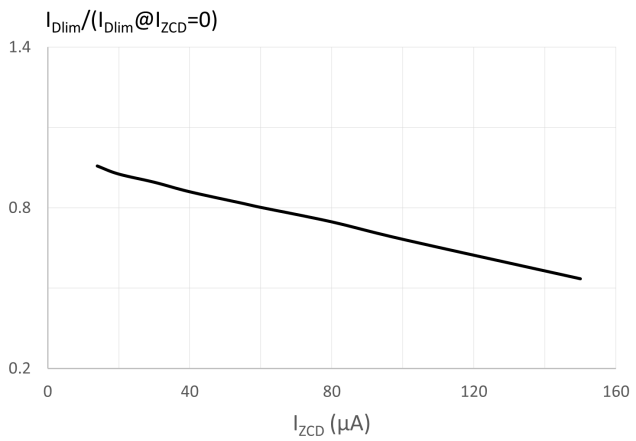


Figure 16. $R_{DS(on)}$ vs T_J

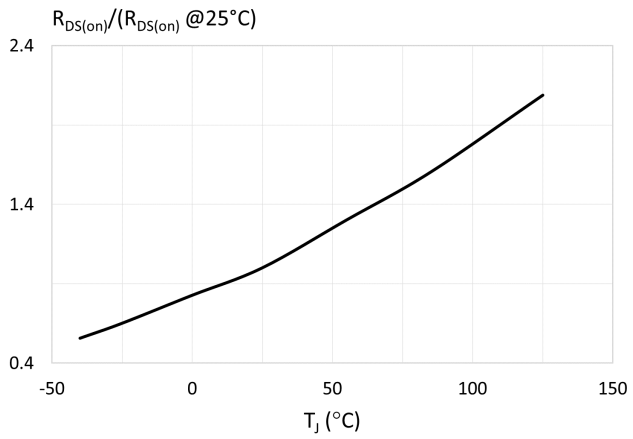


Figure 17. V_{BVDSS} vs T_J

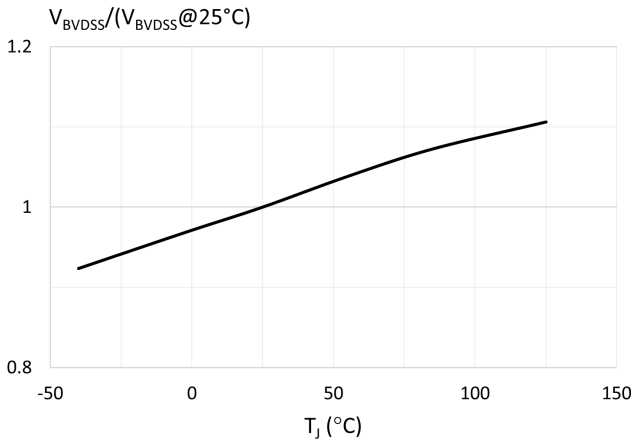


Figure 18. I_{DDch1} vs T_J

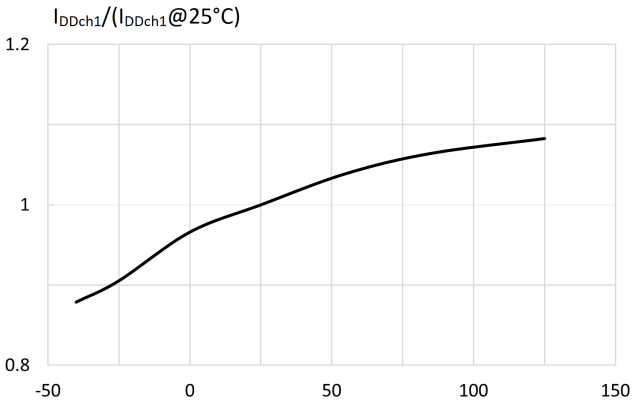


Figure 19. I_{DDch2} vs T_J

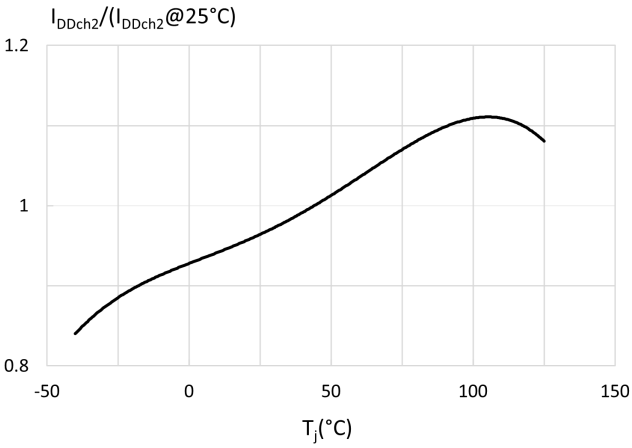


Figure 20. F_{OSClim_L} vs T_J

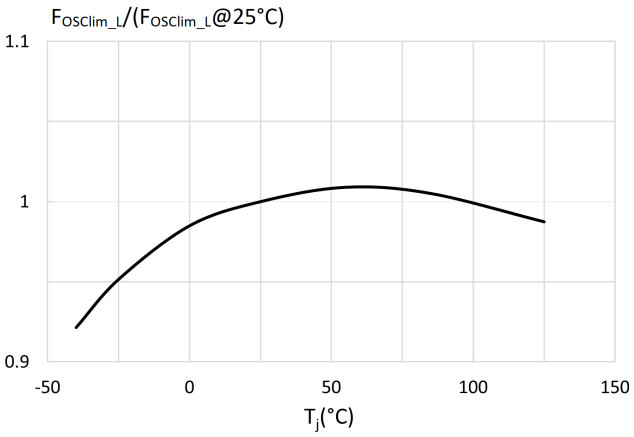


Figure 21. F_{OSClim_H} vs T_J

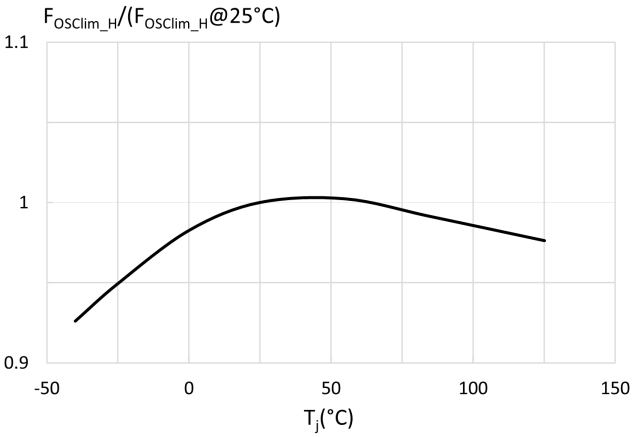
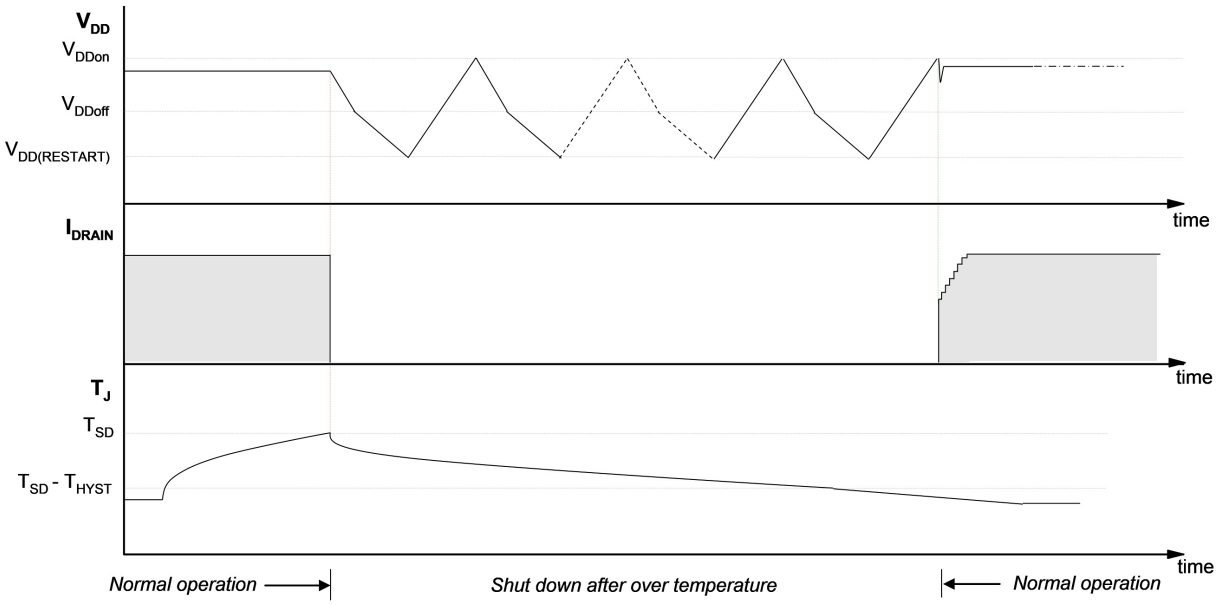


Figure 22. **Thermal shutdown timing diagram**



7 Typical circuits

Figure 23. **Min-feature quasi-resonant flyback (isolated)**

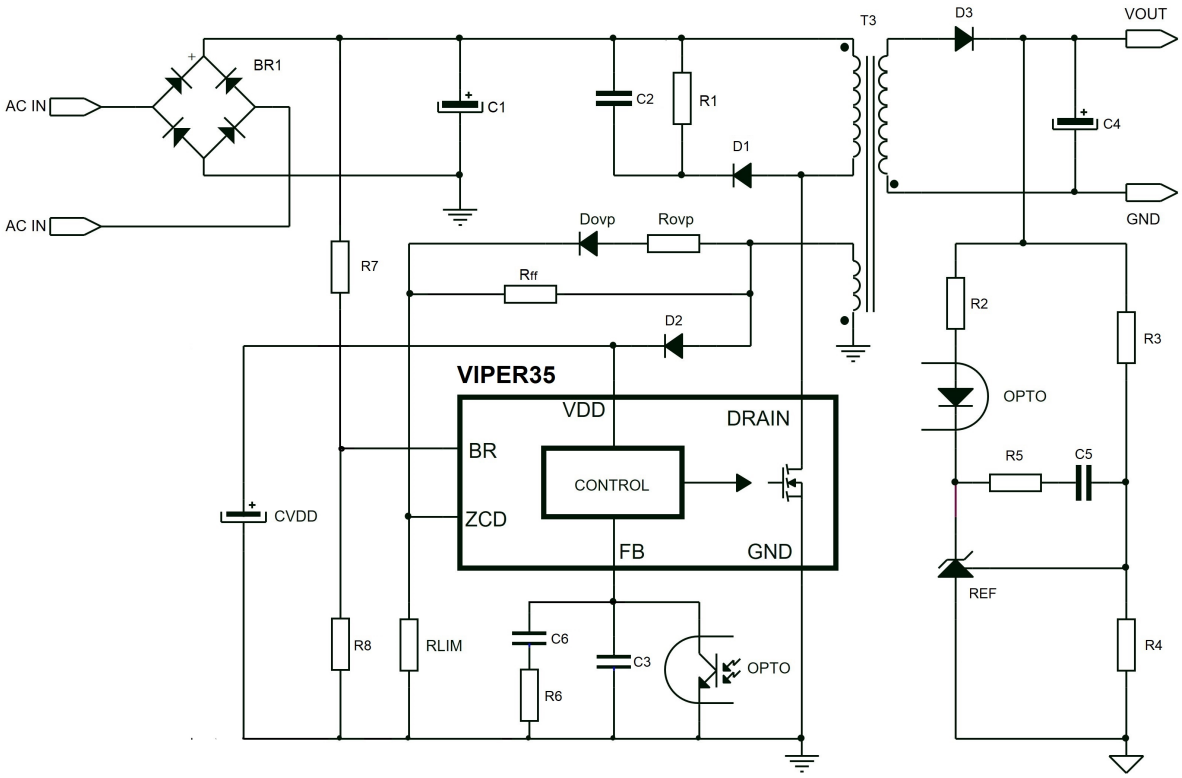
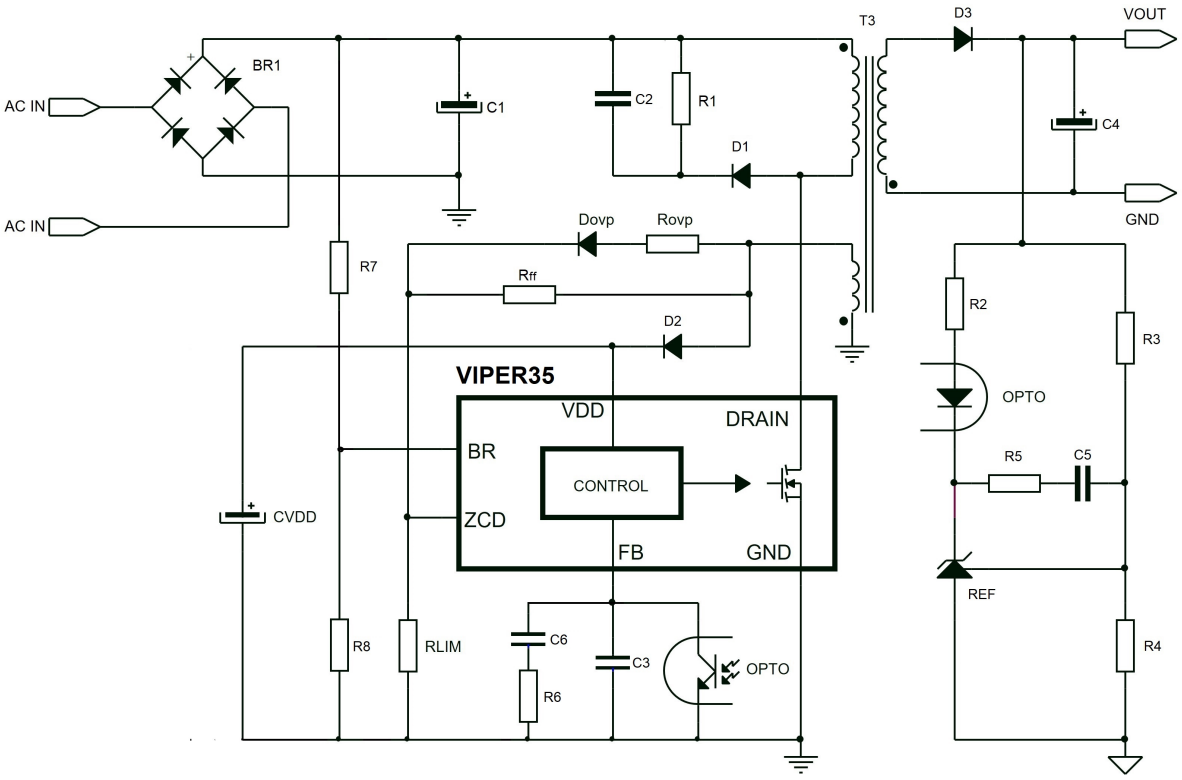


Figure 24. **Full-feature quasi-resonant flyback (isolated)**



8 Efficiency performance for a typical flyback converter

The efficiency of the converter has been measured in different load and line voltage conditions. In accordance with the Energy Star average active mode testing efficiency method, the efficiency measurements have been performed at 25%, 50% and 75% and 100% of the rated output power, both at 115 V_{AC} and 230 V_{AC}.

Table 6. Power supply efficiency, V_{OUT} = 12 V, V_{IN} = 115 V_{AC}

% load	I_{OUT}[A]	V_{OUT}[V]	P_{OUT}[W]	P_{IN}[W]	Efficiency[%]
25%	0.31	12.1	3.78	4.53	83.47
50%	0.63	12.1	7.56	8.98	84.21
75%	0.94	12.1	11.34	13.4	84.65
100%	1.25	12.1	15.12	17.93	84.36
Average efficiency					84.17

Table 7. Power supply efficiency, V_{OUT} = 12 V, V_{IN} = 230 V_{AC}

% load	I_{OUT}[A]	V_{OUT}[V]	P_{OUT}[W]	P_{IN}[W]	Efficiency[%]
25%	0.31	12.1	3.78	4.71	80.28
50%	0.63	12.1	7.56	9.22	82.02
75%	0.94	12.1	11.34	13.53	83.84
100%	1.25	12.1	15.12	17.77	85.12
Average efficiency					82.82

Figure 25. Power supply consumption at light output loads,V_{OUT} = 12 V

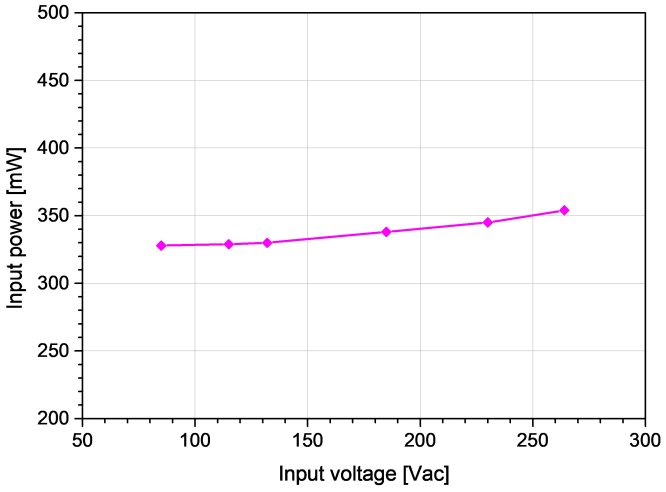
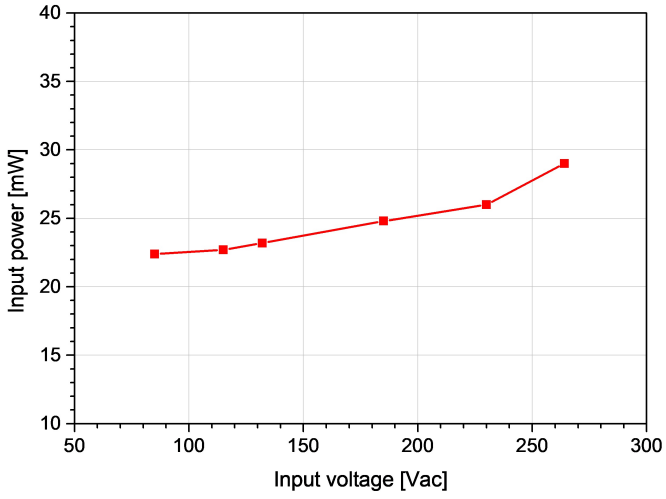


Figure 26. Power supply consumption at no output load, V_{OUT} = 12 V



9 Operation description

The device is a high-performance low voltage PWM controller chip with an 800 V, avalanche-rugged power section.

The controller includes the PWM logic, ZCD logic for quasi-resonant operation, oscillator, start-up circuit with soft-start, current limiting circuit with adjustable set-point, burst mode management, brown-out circuit, UVLO circuit, auto-restart circuit and thermal protection circuit.

The current limit set-point can be reduced by ZCD pin. Burst mode operation guarantees high performance in standby mode and meets energy-saving standards.

Allfault protections are built-in auto-restart mode with very low repetition rate to prevent the IC overheating.

9.1 Power section and gate driver

The power section is given by an avalanche-rugged N-channel MOSFET, which guarantees safe operation within the specified energy rating as well as high dv/dt capability. The power MOSFET has a B_{VDSS} of 800 V min. and a typical $R_{DS\ (on)}$ of 4.5 Ω at 25 °C. The integrated senseFET structure allows a virtual loss-less current sensing.

The gate driver is designed to supply a controlled gate current during both turn-on and turn- off to minimize common-mode EMI. Under UVLO conditions an internal pull-down circuit holds the gate low to ensure that the power section cannot be turned on accidentally.

9.2 High voltage start-up generator

The HV current generator is supplied through the DRAIN pin and it is enabled only if the input bulk capacitor voltage is higher than V_{DRAIN_START} threshold, 80 V DC typically.

When HV current generator is on, I_{DDch1} current (3 mA typical value) is delivered to the capacitor on VDD pin. During auto-restart mode after a fault event, the current is reduced to I_{DDch2} (0.6 mA, typ.) in order to have a slow duty cycle during the restart phase.

9.3 Power-up and soft-start

When the input voltage reaches the device start threshold, V_{DRAIN_START}, the V_{DD} voltage begins growing due to I_{DDch1} current (see Section 5 : Feedback pin) coming from the internal high voltage start-up circuit. If the V_{DD} voltage reaches V_{DDon} threshold, the power MOSFET starts switching and the HV current generator turns off.

The IC is powered by the energy stored in the capacitor on V_{DD} pin, C_{VDD}, until the selfsupply circuit (typically an auxiliary winding of the transformer and a steering diode) develops a voltage so high to sustain the operation.

C_{VDD} capacitor must be correctly sized to avoid fast discharge and keep the required voltage higher than V_{DDoff} threshold. In fact, an insufficient capacitance value could terminate the switching operation before the controller receives any energy from the auxiliary winding.

The following formula can be used to calculate C_{VDD} capacitor:

$$C_{VDD} = \frac{I_{DDch} \times t_{SSaux}}{V_{DDon} - V_{DDoff}} \quad (1)$$

t_{SSaux} is the time needed for the steady-state of the auxiliary voltage. It represents an estimate of the user's application according to the output stage configurations (transformer, output capacitances, etc.).

During the normal operation, the power MOSFET switches on after the transformer demagnetization, detected through the voltage V_{ZCD} sensed on ZCD pin.

At power-up, the initial output voltage is zero and the voltage V_{ZCD} is not so high to correctly arm the internal ZCD circuit. In this case, the power MOSFET turns on with the fixed frequency $F_{STARTER}$, reported in Section 5 : Feedback pin. After the start-up, as soon as the voltage on ZCD logic is enabled to work, the turn-on of the power MOSFET is driven by this circuit and it is not related to the internal oscillator (except for the frequency foldback function) any longer.

The start-up phase is managed by a dedicated internal logic and is activated by every attempt of the start-up converter or after a fault.

An internal clock counter defines the start-up time, t_{SU}, since during quasi-resonant operation, the switching frequency and the duration of the start-up time depend on the load, t_{SU} range is indicated in Section 5 : Feedback pin. At the beginning of the start-up time, the drain current limitation progressively rises to the maximum value. In this way a soft-start occurs and the stress on the secondary diode is considerably reduced. It also prevents transformer saturation.

The soft-start time lasts 3.5 ms (VIPER35L) or 4.2 ms (VIPER35H), (see t_{SS} in Section 5 : Feedback pin).

At the start-up, until the output voltage reaches its regulated value, the feedback loop is open and an improper activation of the overload protection could occur. In order to avoid this, OLP logic is disabled and it is active at the end of the start-up phase, $t > t_{SU}$. Figure 29 and Figure 30 show two possible start-up cases.

As soon as the output voltage reaches the regulated value, the regulation loop takes over and the drain current is regulated below its limit, I_{Dlim}, by the feedback voltage, which is at a value lower than the V_{FBlin} threshold.

Figure 27. I_{DD} current during start-up and burst mode

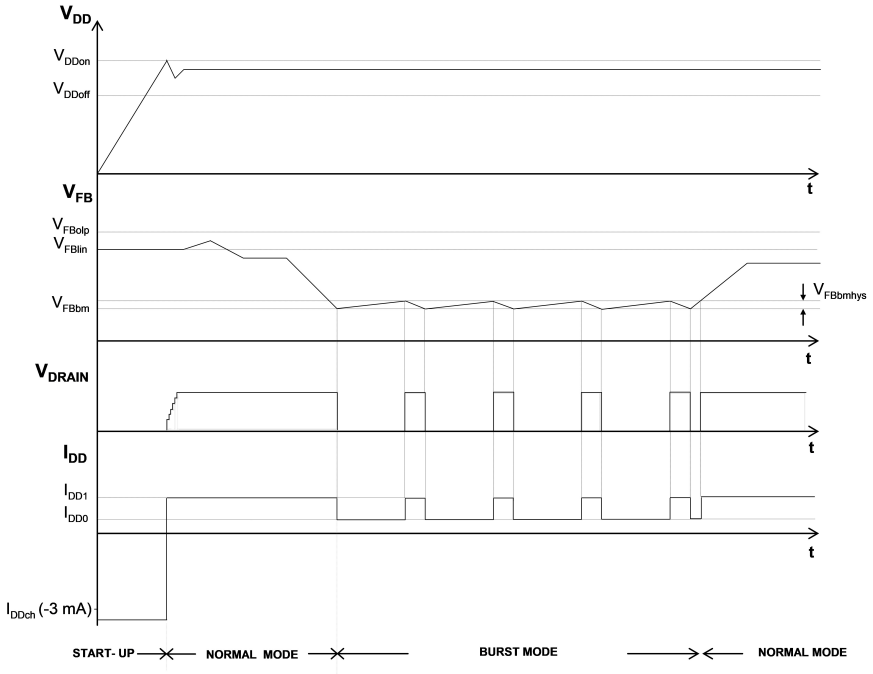


Figure 28. **Timing diagram: normal power-up and power-down sequence**

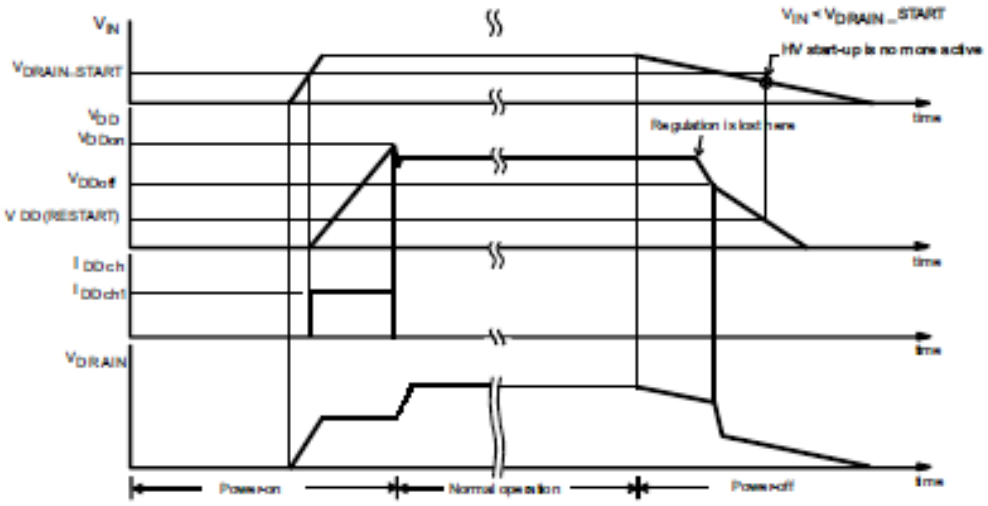


Figure 29. **Timing diagram: start-up phase and soft-start (case 1)**

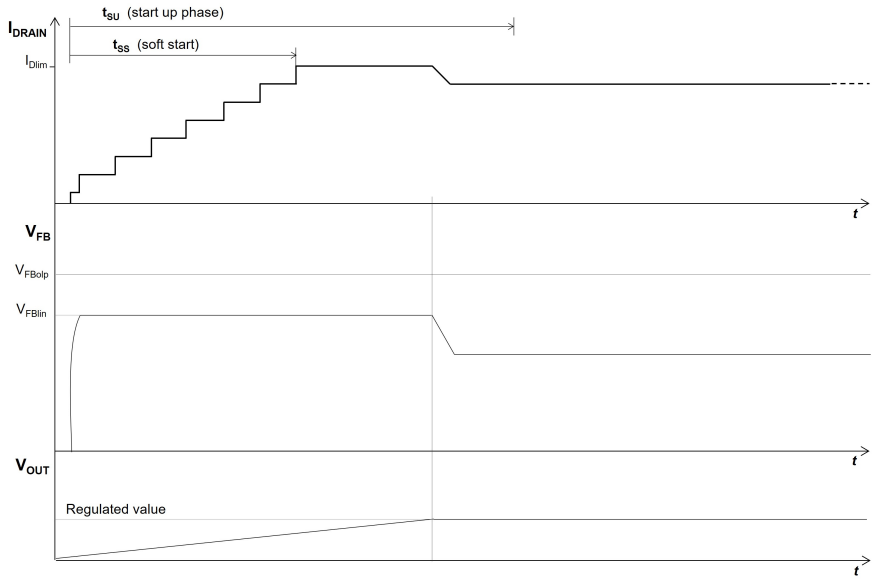
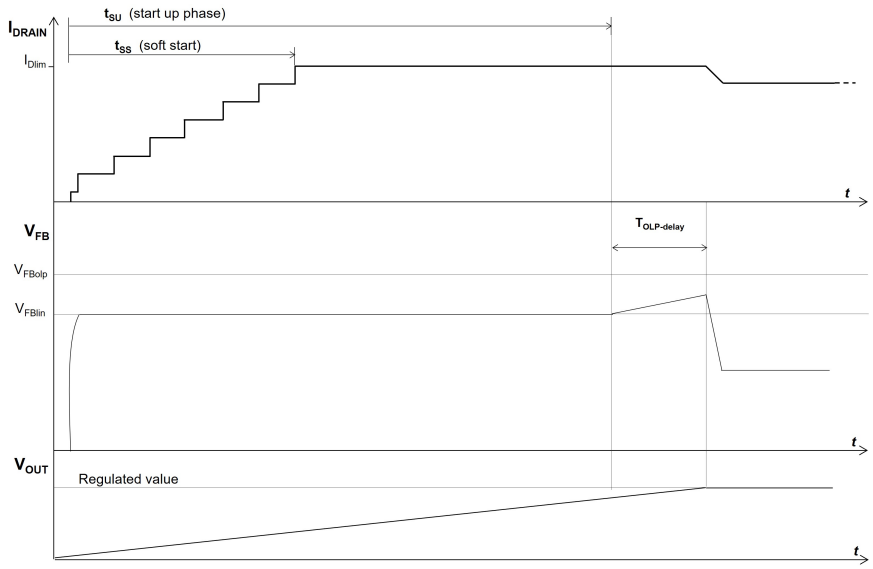


Figure 30. **Timing diagram: start-up phase and soft-start (case 2)**



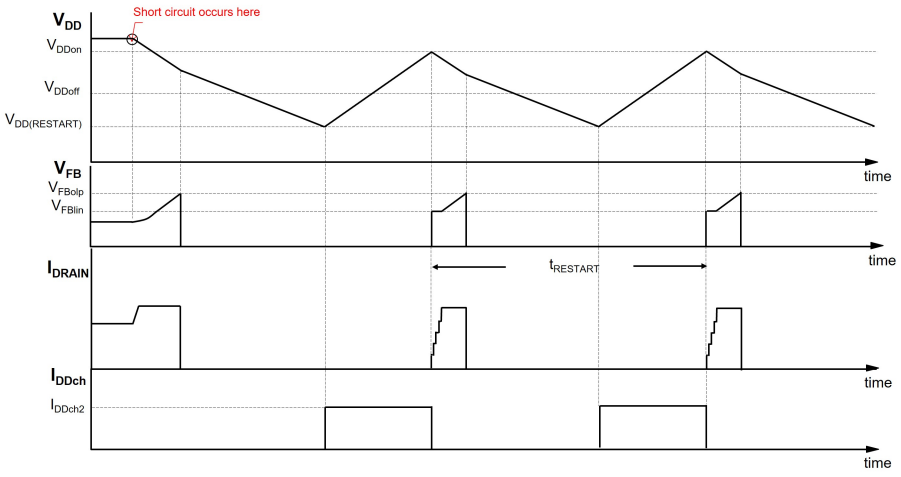
9.4 Power-down description

At converter power-down, the system loses its ability to regulate as soon as the decreasing input voltage is so low to reach the peak current limitation. V_{DD} voltage drops and when it falls below V_{DDoff} threshold (see Section 5 : Feedback pin) the power MOSFET switches off, the energy is interrupted, V_{DD} voltage decreases, the start-up sequence is inhibited and the power-down is completed. This feature prevents any restart attempt and ensures a monotonic output voltage decay during the system power-down.

9.5 Auto-restart description

Every time a protection is tripped, the IC automatically restarts after a duration depending on the discharge and recharge of C_{VDD} capacitor. As shown in Figure 31, after a fault, the IC stops and V_{DD} voltage decreases because of IC consumption. As soon as $_{VDD}$ voltage falls below $V_{DD(RESTART)}$ threshold and if the DC input voltage is higher than V_{DRAIN_START} threshold, the internal HV current source turns on and it starts to charge C_{VDD} capacitor with the current I_{DDch2} (0.6 mA, typ.). As soon as V_{DD} voltage reaches $V_{DD(ON)}$ threshold, the IC restarts.

Figure 31. **Timing diagram: behavior after short-circuit**



9.6 Quasi-resonant operation (QR)

The control core of the VIPER35 is a current mode PWM controller with a zero-current detect circuit designed for quasi-resonant (QR) operation, a technique whose benefits are: minimum turn-on losses, low EMI emission and safe behavior in case of short-circuit. At heavy load the converter operates in quasi-resonant mode; operation synchronizes MOSFET turn-on to the transformer demagnetization by detecting the resulting negative going edge of the voltage across any winding of the transformer. The system works close to the boundary between discontinuous (DCM) and continuous conduction (CCM) of the transformer and as a result, the switching frequency is different according to different line/load conditions. See the hyperbolic-like portion reported in Figure 32.

At medium/ light load, depending on the converter input voltage as well, the device enters valley-skipping mode. An internal oscillator, synchronized to MOSFET turn-on, defines the maximum operating frequency of the converter, F_{OSClim}.

The VIPER35 is available as type 'L' or type 'H', depending on F_{OSClim} value, see Section 5 : Feedback pin.

During the normal operation the converter works with a frequency below F_{OSClim}, so the 'L' type is suitable for applications where the priority is on the EMI filter minimization. The 'H' type is suitable when an extended QR operation range or the transformer size reduction are priorities.

As the load is reduced, and the switching frequency tends to exceed the oscillator's one, MOSFET turn-on doesn't occur on the first valley but on the second one, the third one and so on. In this way a "frequency clamp" effect is achieved, piecewise linear portion is showed in Figure 32.

When the load is extremely light or disconnected, the converter enters burst mode operation. By decreasing the load, the frequency is reduced even few hundred hertz, so to comply with energy saving regulations or recommendations. As the peak current is low, no audible noise occurs.

The above mentioned operation is based on ZCD pin. This pin is the input of the integrated ZCD circuit which allows the power section turn-on at the end of the transformer demagnetization. The input signal for the ZCD is obtained as a partition of the auxiliary voltage used to supply the device, see Figure 33.

When the triggering circuit senses a negative-going edge below V_{ZCDTth} threshold (see Section 5 : Feedback pin), after an internal delay that helps to achieve minimum drain-source voltage switch-on ("valley switching"), the power MOSFET turns on. However, to enable power MOSFET turn-on, the triggering circuit has to be previously armed by a positive-going edge exceeding V_{ZCDAth} threshold (see Section 5 : Feedback pin) on the same ZCD pin.

After the MOSFET turn-off, the blanking time, $t_{BLANK,}$ is generated to avoid an erroneous arming and triggering due to the noise, generated by the leakage inductance resonance of the transformer which rings and couples with ZCD pin.

Figure 32. Switching frequency vs power

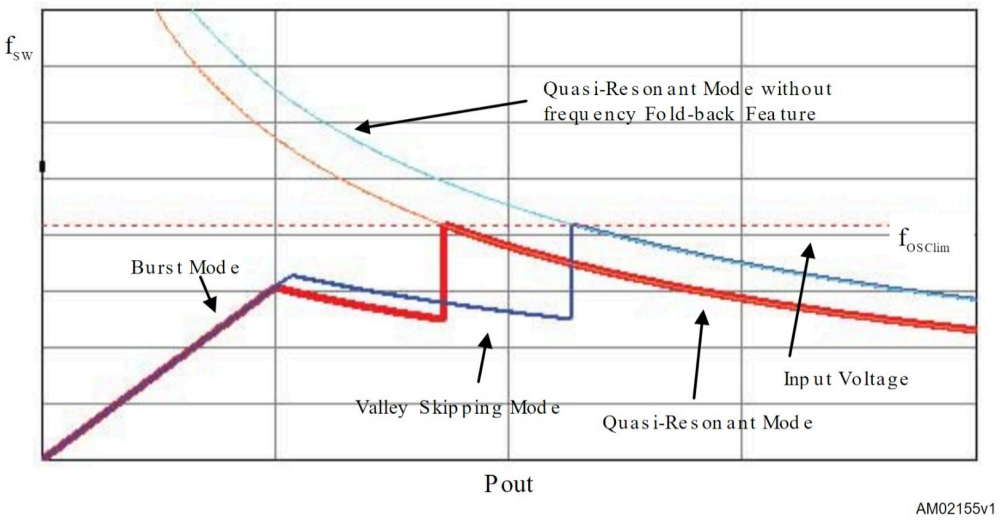
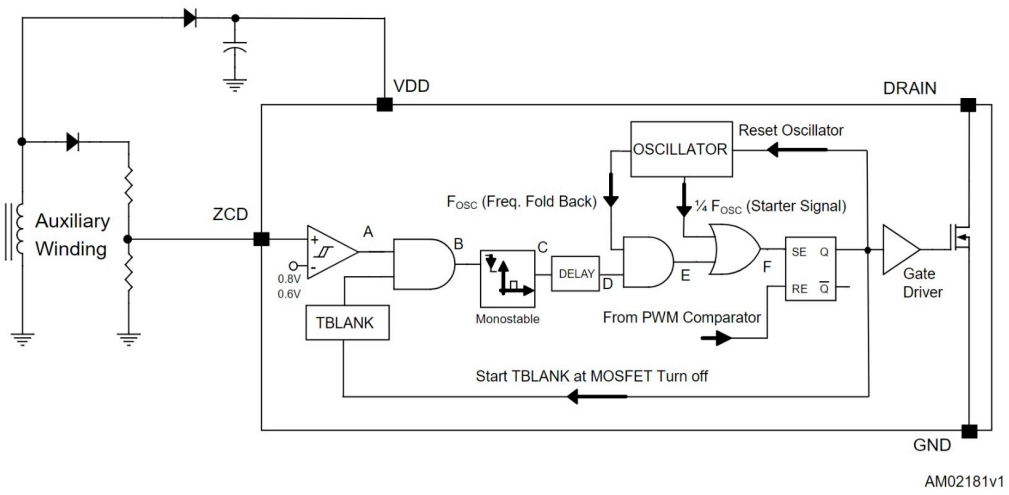


Figure 33. **Zero-current detection circuit**



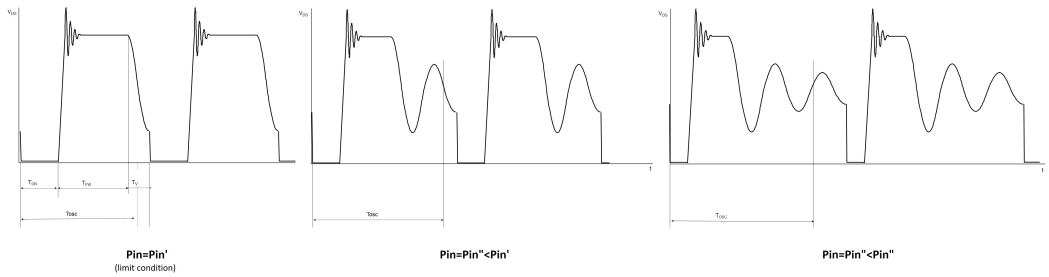
9.7 Frequency foldback function and valley-skipping mode

The switching frequency, in quasi-resonant mode, is not fixed and it depends on both the load and the converter input voltage. The switching frequency increases when the load decreases, or when the mains voltage increases, and vice versa. To avoid that, the VIPER35 taps the maximum switching frequency of the application thanks to its control logic.

The frequency limit is given by an internal oscillator switching at 136 kHz for the VIPER35L or at 225 kHz for the VIPER35H, (see parameter $F_{OSClimin}$Section 5 : Feedback pin). This oscillator is synchronized with the power MOSFET turn-on. When the power MOSFET is off, if the first negative-going edge voltage of the ZCD pin, resulting from transformer demagnetization, appears after at least one oscillator cycle has been completed, the MOSFET turns on and the oscillator is synchronized again.

Otherwise,if the first negative-going edge voltage appears before completing one oscillator cycle, the signal is ignored. Due to the ringing of the drain voltage, the ZCD pin experiences another positive-going edge voltage that arms the circuit and a negative-going edge voltage. Again, if this appears before the oscillator cycle is completed, it is ignored, otherwise the MOSFET turns on and the oscillator is synchronized. In this manner, one or more drain ringing cycles are skipped (Figure 34 shows the so called “valley-skipping mode”) and the switching frequency doesn’t exceed F_{OSClim} limit.

Figure 34. **Drain ringing cycle skipping as the load progressively reduces**



When the system operates in valley-skipping mode, uneven switching cycles may be observed under some line/load conditions, due to the fact that the off-time of the power MOSFET changes its discrete steps one ringing cycle, while the off-time needed for cycle by-cycle energy balance could fall in between. Therefore one or even longer switching cycles are compensated by one or more shorter cycles and vice versa. This mechanism is natural and any effect on the converter performance and on its output voltage appears.

This operation does not consider the blanking time t_{BLANK} after power MOSFET turn-off. Actually t_{BLANK} is not taken into account as long as the following condition is met:

$$D \leq 1 - \frac{T_{BLANK}}{T_{OSClim}} = 1 - T_{BLANK} \cdot F_{OSClim} \quad (2)$$

where D is the MOSFET duty cycle. If this condition is not met, the time during which MOSFET turn-on is inhibited is extended beyond t_{OSClim} by a fraction of t_{BLANK}. As a consequence, the maximum switching frequency is a little bit lower than the internal limit set by the oscillator and valley-skipping mode takes place slightly earlier than expected.

9.8 Blanking time

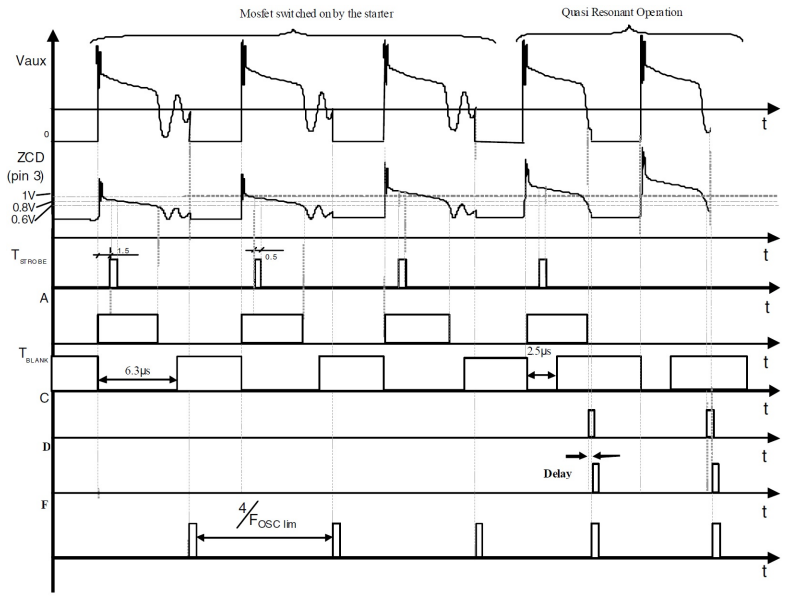
The blanking time, t_{BLANK}, can have two different values: the lower one is 2.5 seconds (typical value) and the higher one is 6.3 seconds (typical value). The value is linked to the voltage V_{ZCD}, sampled during the time t_{STROBE}. The time t_{BLANK} has the lower value if V_{ZCD}>1 V or it has the higher value if V_{ZCD}<1 V, refer to Section 5 : Feedback pin and Figure 35.

The higher value of the blanking time is active during the start-up phase or in case of output short-circuit, when the output voltage of the converter is quite lower than the regulated value. In this condition, during the demagnetization of the transformer, VZCD can be very close to the arming and triggering thresholds (V_{ZCDAth} and V_{ZCDTth}) and ZCD circuit can be erroneously trigged, leading the system to work with higher frequency and in continuous mode. This false trigger is inhibited by the selection of t_{BLANK} higher value when V_{ZCD} is lower than 1 V.

During the normal operation, in steady-state condition, the voltage V_{ZCD} during the demagnetization is higher than 1 V and the selected t_{BLANK} value is the lower one.

Figure 35 shows the typical waveforms during the power-up and the linked t_{BLANK} selection.

Figure 35. Timing diagram: doubleblanking time



9.9 Starter

If the amplitude of the voltage on ZCD pin at the end of one oscillator cycle is smaller than V_{ZCDAth} arming threshold, (in this case MOSFET turn-on could not be triggered), the system stops.

This is what normally happens during the converter power-up or under overload/short-circuit conditions.

During the converter start-up phase, the voltage on ZCD pin is not so high to arm the triggering circuit. Thus, the converter operates at a fixed frequency, $F_{STARTER}$, (see Section 5 : Feedback pin). As the voltage developed across the auxiliary winding arms the ZCD circuit,

MOSFET turn-on is locked to transformer demagnetization, hence quasi-resonant operation is set.

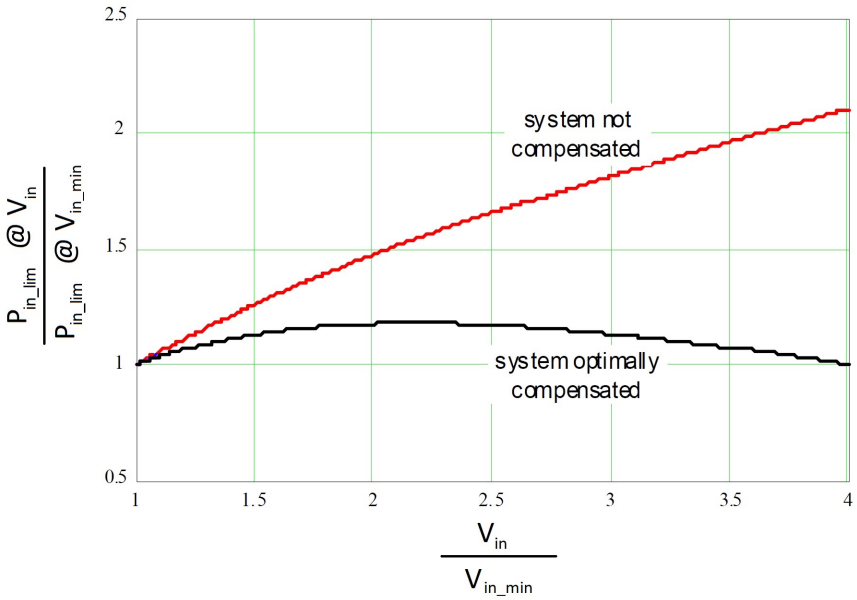
9.10 Current limit set-point and feed-forward option

The VIPER35 is a current mode converter and the drain current is limited cycle-by-cycle according to FB pin voltage value, which is related to the feedback loop response and the load. When the drain current, sensed by the integrated senseFET, reaches the current limitation, after the internal propagation delay, the MOSFET switches off. The current limitation cannot exceed a certain value, I_{Dlim}, which can vary according to the current sunk by ZCD pin during MOSFET on-time.

Usually a resistor, R_{LIM}, connected from ZCD pin to ground fixes this sunk current and then the peak drain current set-point: the lower the resistor, the lower I_{Dlim}.

For a quasi-resonant flyback converter, the power capability strongly depends on the input voltage. In wide range applications, at maximum line, the power capability can be more than twice the value at minimum line, as shown by the upper curve in the diagram, see Figure 36. To reduce this dependence, the I_{Dlim} has to be reduced according to the increment of the input voltage, this is the line feed-forward. It's given by a resistor, RFF, connected between the ZCD pin and the auxiliary winding, see Figure 37. Since the voltage across the auxiliary winding during MOSFET on-time is proportional to the input voltage through the auxiliary-to-primary turn ratio N_{AUX}/N_P, a current proportional to the input voltage is sunk by the ZCD pin, thus the overcurrent set-point lowers.

Figure 36. Typical power capability vs input voltage in quasi-resonant converter



In order to select the R_{FF} resistance value (see Figure 37), when the proper overcurrent set- points are known at minimum and at the maximum converter input voltage, in Figure 15 the needed current to sink during MOSFET on-time is visible. With the following approximated formula, the value of R_{FF} resistor can be calculated:

$$R_{FF} = \frac{V_{in_max} - V_{in_min}}{n_{aux} \cdot (I_{ZCD1} - I_{ZCD2})} \quad (3)$$

where:

- V_{in_Max} and V_{in_min} are the maximum and minimum converter rectified input voltage.
- N_{AUX} is the primary-to-auxiliary winding turn ratio.
- I_{ZCD1}, and I_{ZCD2} are the currents needed to sink from the ZCD pin, in order to obtain the selected overcurrent set-points, at maximum and minimum flyback input voltage, see Figure 15.

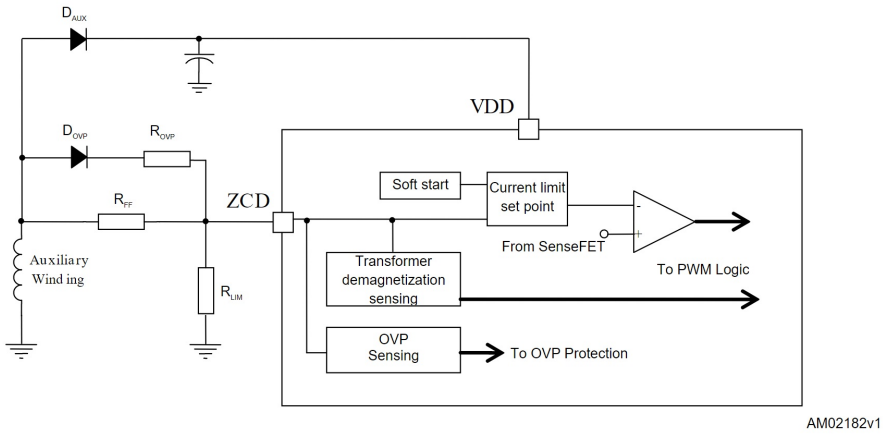
Given R_{FF} value, R_{LIM} value can be calculated by the following formula:

$$R_{LIM} = Max\left(\frac{V_{ZCD1}}{I_{ZCD1} - \frac{\frac{V_{in_min}}{n_{aux}} + V_{ZCD1}}{R_{FF}}}, \frac{V_{ZCD2}}{I_{ZCD2} - \frac{\frac{V_{in_max}}{n_{aux}} + V_{ZCD2}}{R_{FF}}}\right) \quad (4)$$

where:

V_{ZCD1} and V_{ZCD2} are ZCD pin voltages when the sunk current is I_{ZCD1} and I_{ZCD2} respectively, see Figure 14.

Figure 37. ZCD pin typical external configuration



9.11 Overvoltage protection (OVP)

The device has integrated the logic to monitor the output voltage using as input signal, the voltage V_{ZCD} during the off-time of the power MOSFET. This is the time when the voltage from the auxiliary winding tracks the output voltage, through the turn ratio N_{AUX}/N_{SEC}.

ZCD pin has to be connected to the auxiliary winding through the diode D_{OVP} and the resistors R_{OVP} and R_{LIM} as shown in Figure 37. When, during the off-time, the voltage V_{ZCD} exceeds, four consecutive times, the reference voltage V_{OVP} (reported in Table 6), the overvoltage protection stops the power MOSFET and the converter enters auto-restart mode.

In order to bypass the noise after the turn-off of the power MOSFET, V_{ZCD} voltage is sampled inside a short window after the time t_{STROBE}, see Section 5 ,Feedback pin, and Figure 38. The sampled signal, if higher than V_{OVP}, triggers the internal OVP digital signal and increments the internal counter. The same counter is reset every time the signal OVP is not triggered in one oscillator cycle.

Referring to Figure 37, the resistor divider ratio kOVPis given by below equations:

$$k_{OVP} = \frac{V_{OVP}}{\frac{N_{aux}}{N_{sec}} \cdot \left(V_{OUTOVP} + V_{DSEC}\right) - V_{DAUX}} \quad (5)$$

$$k_{OVP} = \frac{R_{LIM}}{R_{LIM} + R_{OVP}} \quad (6)$$

where:

- V_{OVP} is theOVP threshold (see Section 5 ,Feedback pin,)
- V_{OUTOVP} is the converter output voltage value to activate the OVP (set by design)
- N_{AUX} is the auxiliary winding turn
- N_{SEC} is the secondary winding turn
- V_{DSEC} is the secondary diode forward voltage
- V_{DAUX} is the auxiliary diode forward voltage

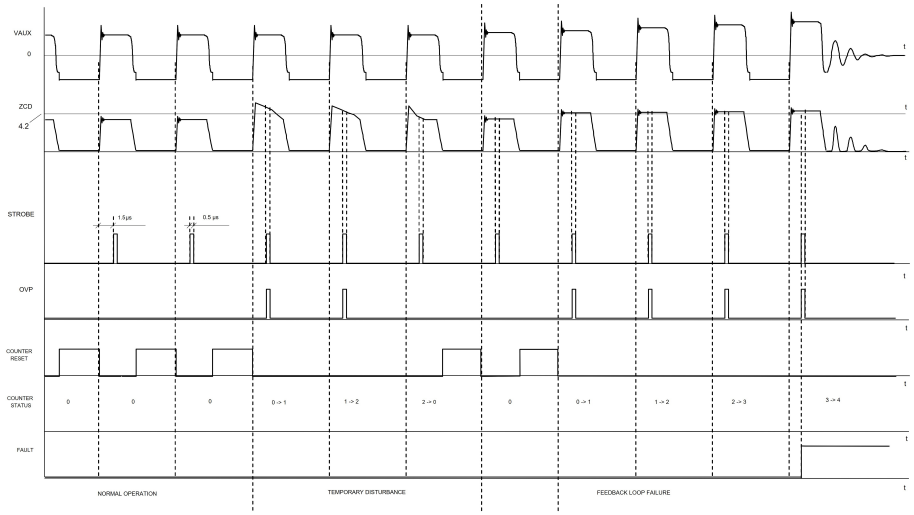
- R_{OVP} and R_{LIM} make the output voltage divider

Byfixing R_{LIM}, according to the desired I_{Dlim}, R_{OVP} can be calculated as follows:

$$R_{OVP} = R_{LIM} \cdot \frac{1 - k_{OVP}}{k_{OVP}} \quad (7)$$

The resistor values let the current sourced and sunk by the ZCD pin be within the rated capability of the internal clamp.

Figure 38. Timing diagram:OVP



9.12 ZCD pin summary

With reference to Figure 37, the circuitry connected to the ZCD pin enables the following functions:

1. Current limit set-point (I_{DLIM})
2. Line feed-forward compensation (FF)
3. Output overvoltage protection (OVP)
4. Zero-current detection for QR operation

Chosen R_{LIM}, R_{FF} and R_{OVP} as described in the previous sections, these functions are automatically defined.

Section 5 ,Feedback pin, refers to Figure 37 and lists the external resistance combinations needed to activate one or more functions associated to ZCD pin.

Table 8. ZCD pin configurations

I_{Dlim}	OVP	FF	R_{Lim}	R_{OVP}	R_{FF}	D_{OVP}
■	□	□		Eq. (7) with V_{OUTOVP} >2 V_{OUT}	-	Yes
□	■	□	22 kΩ	Eq. (7)	-	Yes
□	□	■	22 kΩ	Eq. (7) with V_{OUTOVP}>2V_{OUT}	Eq. (3)	Yes
■	■	□	with R_{FF}= ∞	Eq. (7)	-	Yes
□	■	■	22 kΩ	Eq. (7)	Eq. (3)	Yes
■	□	■	Eq. (4)	Eq. (7) with V_{OUTOVP} >2V_{OUT}	Eq. (3)	Yes
■	■	■	Eq. (4)	Eq. (7)	Eq. (3)	Yes

9.13 Feedback and overload protection (OLP)

The feedback pin (FB) controls the PWM operation, enters the burst mode and manages the delayed overload protection.

V_{FBbm} and V_{FBlin} thresholds (Section 5 ,Feedback pin,) are respectively low and high limit of PWM operations, where the drain current is sensed by the integrated resistor, R_{SENSE}, and applied to the comparator PWM. The PWM logic turns off the power MOSFET as soon as the sensed voltage is equal to the voltage applied to FB pin and through the integrated resistor network (see Figure 1 and Figure 23).

IC block diagram (Figure 1) shows in parallel with the PWM comparator how OCP comparator limits the drain current to IDlim value, as per Section 5 ,Feedback pin, .

In case of higher load, the voltage VFB increases, when it reaches V_{FBlin} threshold, the drain current is limited to I_{Dlim} by OCP comparator and the internal current starts the charge of CFB capacitor. As soon as the voltage VFB reaches the threshold V_{FBolp}, see Figure 41, the protection turns off the IC. The auto-restart mode is active using the low value of the current I_{DDch}, see Section 5 ,Feedback pin, .

The time, from the high load detection, $V_{FB} = V_{FBlin}$, to the overload turn-off, $V_{FB} = V_{FBolp}$, depends on the value of CFB capacitor and on the internal charge current, IFB. OLP delay time can be calculated as follows:

$$T_{OLP_delay} = C_{FB} \cdot \frac{V_{FBolp} - V_{FBlin}}{I_{FB}} \quad (8)$$

The current, I_{FB}, is 3 A as minimum value. Components, connected to FB pin, belong to the compensation loop, so they have to be selected taking into account the proper delay and loop stability. Figure 39 and Figure 40 show two different feedback networks.

In Figure 39 CFB capacitor, connected to FB pin, is used as part of the circuit to compensate the feedback loop but it is also an element to delay OLP shutdown owing to the time needed to charge the capacitor (see Equation 8). After the start-up time, t_{SU}, during which the feedback voltage is fixed at V_{FBlin}, the output capacitor could not be at its nominal value and the controller detects this situation as an overload condition. In this case, OLP delay avoids the wrong device shutdown during the start-up.

Owing to the above considerations, OLP delay time must last to bypass the initial output voltage transient and check the overload condition only when the output voltage is in steady-state. The output transient time depends on the value of the output capacitor and on the load.

When CFB capacitor value is too low and cannot ensure the OLP delay, an alternative compensation network can be used as showed in Figure 40. Two poles (f_{PFB}, f_{PFB1}) and one zero (f_{ZFB}) are introduced by CFB and C_{FB1} capacitors and R_{FB1} resistor.

The capacitor CFB introduces a pole (f_{PFB}) at higher frequency than f_{ZB} and f_{PFB1}. This pole compensates zero frequency due to ESR (equivalent series resistor) of the output capacitance of the flyback converter.

By taking into account the scheme in Figure 40, these poles and zero frequency are reported as follows:

$$f_{ZFB} = \frac{1}{2 \cdot \pi \cdot C_{FB} \cdot R_{FB}} \quad (9)$$

$$f_{PFB} = \frac{R_{FB(DYN)} - R_{FB1}}{2 \cdot \pi \cdot C_{FB} \cdot \left(R_{FB(DYN)} \cdot R_{FB1}\right)} \quad (10)$$

$$f_{PFB} = \frac{1}{2 \cdot \pi \cdot C_{FB1} \cdot \left(R_{FB1} + R_{FB(DYN)}\right)} \quad (11)$$

$R_{FB(DYN)}$ is the dynamic resistance seen by FB pin and reported in Section 5 ,Feedback pin, . C_{FB1} capacitor fixes the OLP delay and usually it is much higher than C_{FB}. Eq. (8) calculates the OLP delay time but C_{FB1} has to be considered. Using the alternative compensation network, the designer can satisfy the loop stability and OLP delay time.

Figure 39. **FB pin configuration (minimal BOM)**

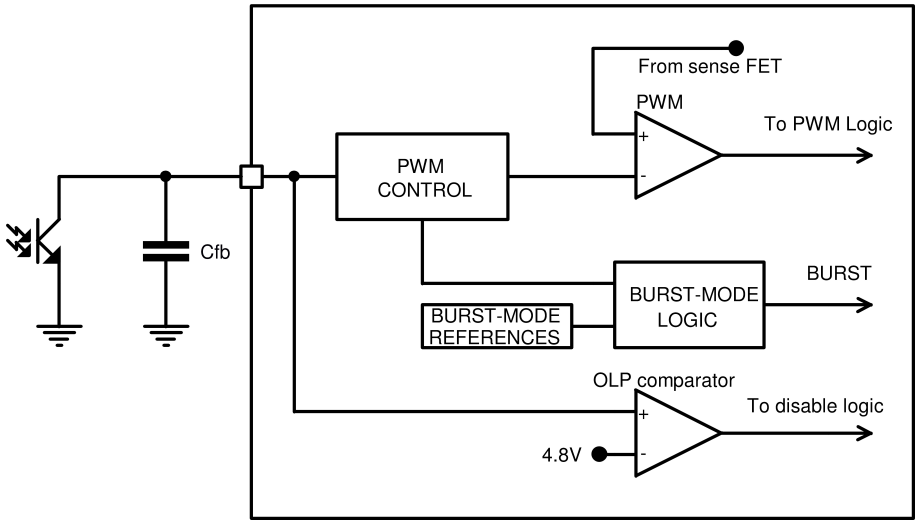


Figure 40. **FB pin configuration**

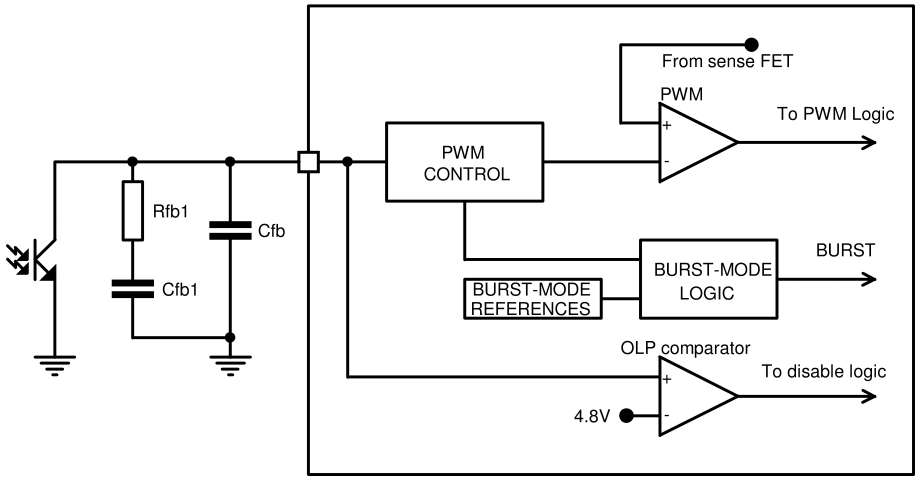
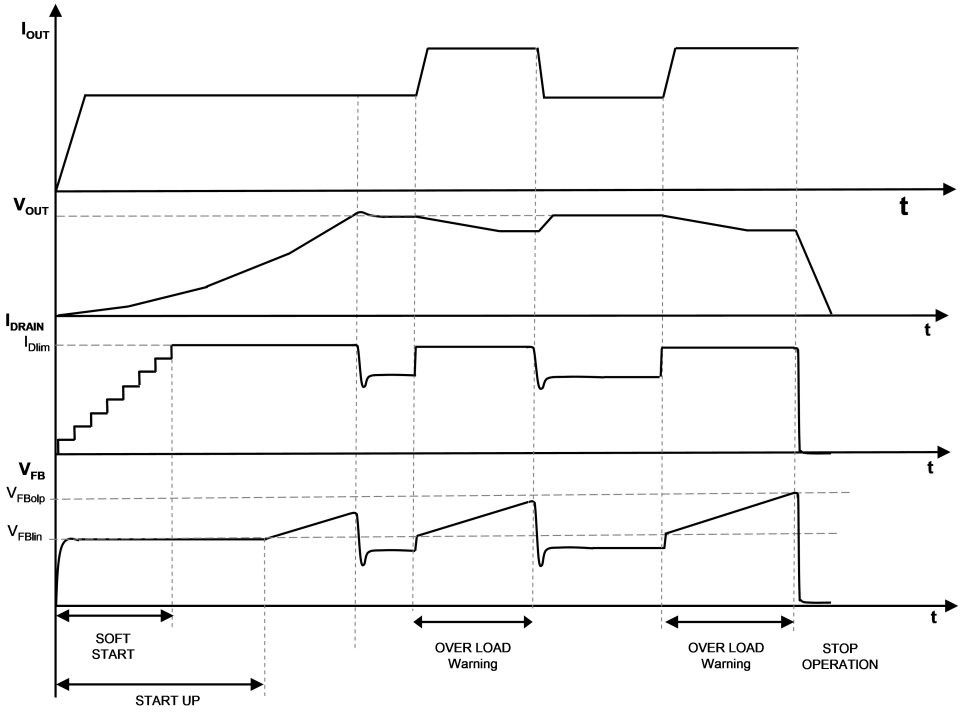


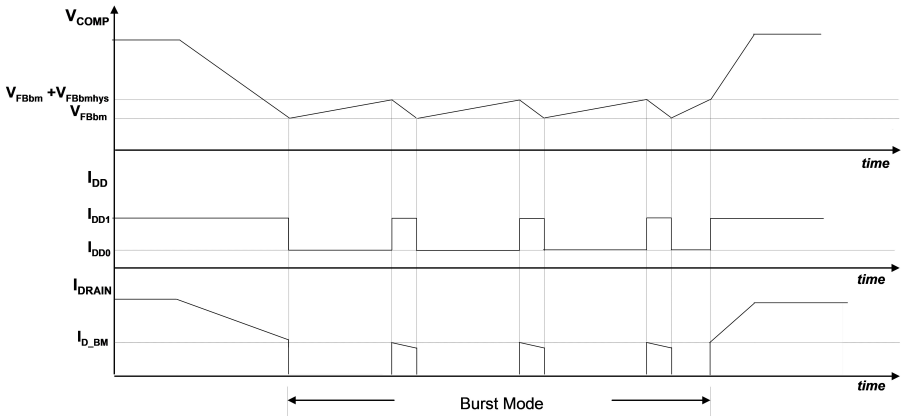
Figure 41. **Timing diagram: overload protection**



9.14 Burst mode operation at no-load or very light load

When the load decreases, the feedback loop lowers the feedback pin voltage. If it falls down the burst mode threshold, V_{FBBm}, the power MOSFET doesn't switch on. After the MOSFET stops, the feedback pin voltage increases and by exceeding the level, $V_{FBbm} + V_{FBbmhys}$, the power MOSFET starts switching again. The burst mode thresholds are reported in Section 5 ,Feedback pin, and Figure 42 shows this behavior. System alternates period of time where power MOSFET switches to period of time where power MOSFET doesn't switch; this device working mode is the burst mode. The power delivered to output during switching periods exceeds the load power demands; the excess of power is balanced by the period where no power is processed. The advantage of burst mode operation is an average switching frequency much lower than the normal operation working frequency, up to some hundred of hertz, minimizing all frequency-related losses. During the burst mode the drain current peak is clamped to the level, I_{D_BM}, (see Section 5 ,Feedback pin,).

Figure 42. **Burstmode timing: light load management**



9.15 Brown-out

Brown-out protection is a not-latched shutdown function active when a condition of mains undervoltage is detected. The brown-out comparator is internally referenced to V_{BRth} threshold (see Section 6) and disables the PWM if the voltage applied to BR pin is below this internal reference. Under this condition the power MOSFET turns off.

Until the brown-out condition is present, the V_{DD} voltage continuously oscillates between the V_{DDon} and the UVLO thresholds, as shown in the timing diagram of Figure 43. A voltage hysteresis improves the noise immunity.

The switching operation restarts as the voltage on the pin is above the reference plus the voltage hysteresis. The brown-out comparator is provided with a current hysteresis, I_{BRhyst}.

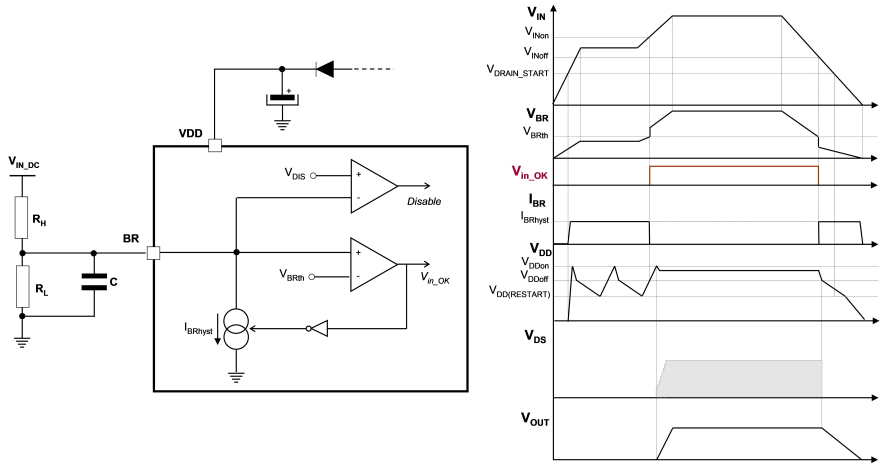
The designer has to set the rectified input voltage above which the power MOSFET starts switching after brown-out event, V_{INon}, and below which the power MOSFET switches off, V_{INoff}. Thanks to the I_{BRhyst}, see Section 5 ,Feedback pin, , these two thresholds can be set separately.

When V_{INon} and V_{INoff} levels are fixed, with reference to Figure 43, the following relationships can be established to calculate R_H and R_L resistors:

$$R_L = -\frac{V_{BRhyst}}{I_{BRhyst}} + \frac{V_{INon} - V_{INoff} - V_{BRhyst}}{V_{INon} - V_{BRth}} \cdot \frac{V_{BRth}}{I_{BRhyst}} \quad (12)$$

$$R_H = \frac{V_{INon} - V_{INoff} - V_{BRhyst}}{I_{BRhyst}} \cdot \frac{R_L}{R_L + \frac{V_{BRhyst}}{I_{BRhyst}}} \quad (13)$$

Figure 43. Brown-out: external setting and timing diagram



V_{INon} must be less than the peak voltage at minimum mains and V_{INoff} voltage has to be less than the minimum voltage on the input bulk capacitor at minimum mains and maximum load.

BR pin is a high impedance input connected to high value resistors, thus it is ready to pick up noise, which might alter the V_{INoff} threshold when the converter operates or causes the undesired switch-off of the device during ESD tests.

The pin ca be bypassed to ground with a small film capacitor (1-10 nF) to prevent any malfunctioning.

If the brown-out function is not used, BR pin has to be connected to GND, ensuring that the voltage is lower than the minimum V_{DIS} threshold (50 mV, see Section 5 ,Feedback pin,). In order to enable the brown-out function, BR pin voltage has to be higher than the maximum V_{DIS} threshold (150 mV, see Section 5 ,Feedback pin,).

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 SO16N package information

Figure 44. **SO16N package outline**

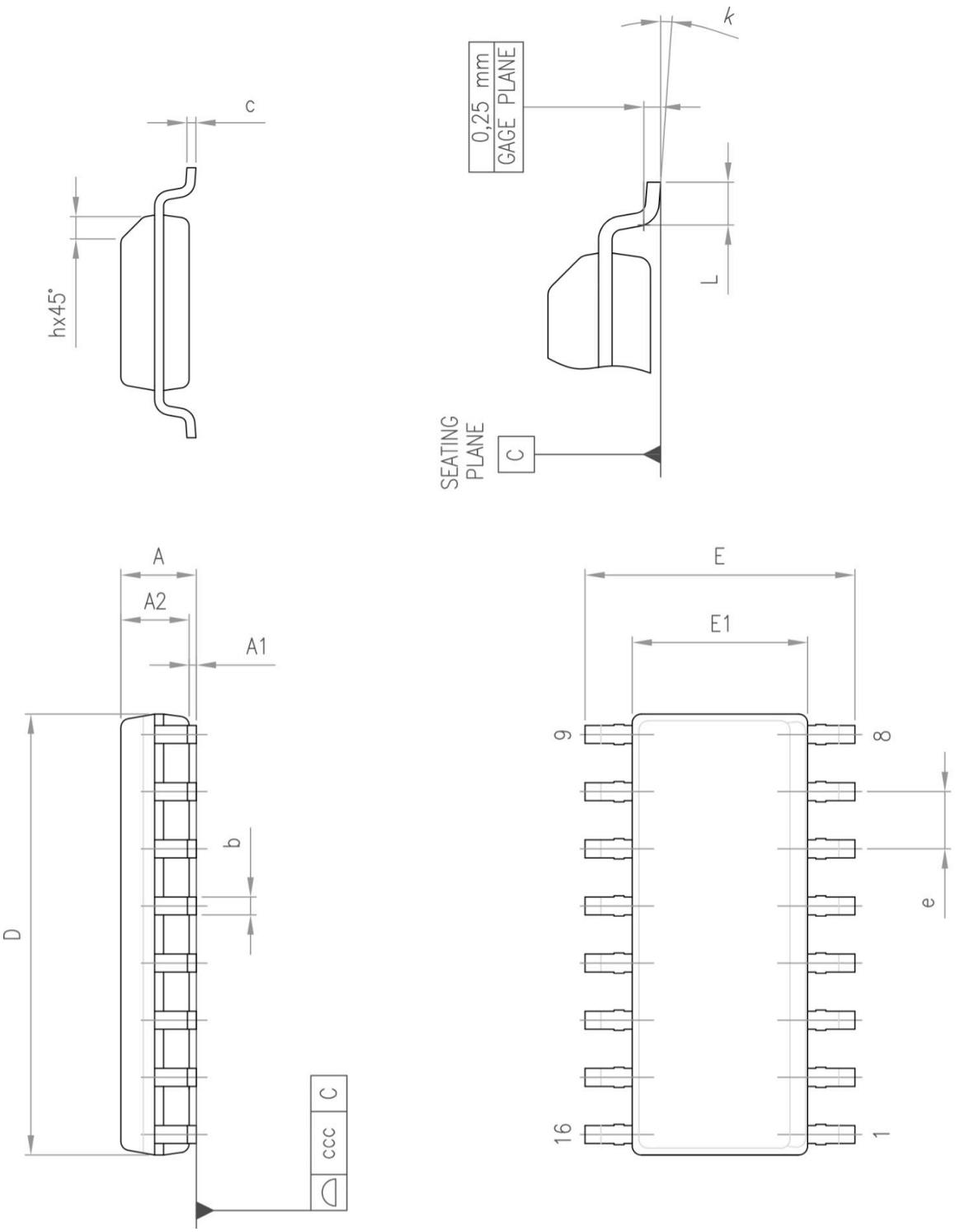


Table 9. **SO16N mechanical data**

Symbol	Milimeters		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
k	0		8°
ccc			0.10

11 Ordering information

Table 10. **Order codes**

Order code	F_{Osclim}	$R_{DS(on)}$	Peak drain current	Package
VIPER35LD	136 kHz	4.5 Ω	1 A	SO16N (tube)
VIPE35LDTR				SO16N (tape and reel)
VIPER35HD	225 kHz			SO16N (tube)
VIPER35HDTR				SO16N (tape and reel)

Revision history

Table 11. **Document revision history**

Date	Version	Changes
23-Feb-2015	1	Initial release.
19-Mar-2015	2	Updated title in cover page. Minor text changes.
08-Jul-2015	3	Document status promoted frompreliminary data to production data. Updated Section 4: Electrical ratings. Minor text changes.
10-Feb-2016	4	Added SDIP10 package Updated Figure 1 title in cover page from “Internal schematic diagram” to “Basic application schematic”. Updated Section 3:Pin settings, Table 2: Pin description, Table 4: Thermal data and Section 10 Ordering information. Added Section 9.2 :SDIP10 package information Minor text changes.
12-Dec-2022	5	Changed picture of package Cover image, changed Section 3 configuration, and some values in Table 4

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