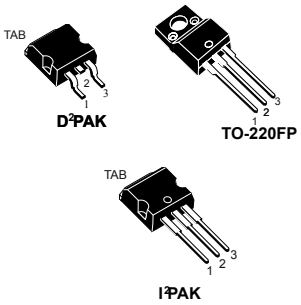
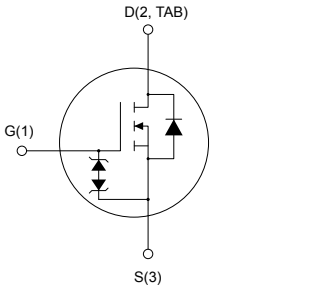
STB33N65M2, STF33N65M2, STI33N65M2

Datasheet

N-channel 650 V, 117 mΩ typ., 24 A MDmesh M2 Power MOSFET in a D²PAK, TO-220FP and I²PAK packages





Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB33N65M2	650 V	140 mΩ	24 A
STF33N65M2			
STI33N65M2			

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the MDmesh M2 technology. Thanks to their strip layout and improved vertical structure, these devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high-efficiency converters.

Product status links
STB33N65M2
STF33N65M2
STI33N65M2

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D^2PAK I^2PAK	TO-220FP	
V_{DS}	Drain-source voltage	650		V
V_{GS}	Gate-source voltage	±25		V
I_D	Drain current (continuous) at T_C = 25 °C	24		A
I_D	Drain current (continuous) at T_C = 100 °C	15		A
I_{DM}(1)	Drain current (pulsed)	96		A
P_{TOT}	Total power dissipation at T_C = 25 °C	190	34	W
dv/dt(2)	Peak diode recovery voltage slope	15		V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	-	2.5	kV
T_{stg}	Storage temperature range	-55 to 150		°C
T_J	Maximum operating junction temperature	150		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 24 A, di/dt ≤ 400 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*
3. *V_{DS} = 520 V.*

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		D^2PAK	I^2PAK	TO-220FP	
R_{thJC}	Thermal resistance, junction-to-case	0.66		3.68	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	30(1)	62.5		°C/W

1. *When mounted on a standard 1 inch^2 area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	2.5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	780	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	650	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C(1)	-	-	100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V	-	-	±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 12 A	-	117	140	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1790	-	pF
C_{oss}	Output capacitance		-	75	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{oss\ eq.}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	380	-	pF
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 24 A, V_{GS} = 0 to 10 V (see the Figure 16. Test circuit for gate charge behavior)	-	41.5	-	nC
Q_{gs}	Gate-source charge		-	6.8	-	nC
Q_{gd}	Gate-drain charge		-	18	-	nC
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	5	-	Ω

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 12 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	13.5	-	ns
t_r	Rise time		-	11.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	72.5	-	ns
t_f	Fall time		-	9	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	24	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	96	A
V_{SD}(2)	Forward on voltage	I_{SD} = 24 A, V_{GS} = 0 V	-	-	1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 24 A, di/dt = 100 A/µs, V_{DD} = 60 V (see the Figure 17. Test circuit for inductive load switching and diode recovery times)	-	426	-	ns
Q_{rr}	Reverse recovery charge		-	7	-	µC
I_{RRM}	Reverse recovery current		-	33.5	-	A
t_{rr}	Reverse recovery time	I_{SD} = 24 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see the Figure 17. Test circuit for inductive load switching and diode recovery times)	-	544	-	ns
Q_{rr}	Reverse recovery charge		-	10	-	µC
I_{RRM}	Reverse recovery current		-	36.5	-	A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for D²PAK and I²PAK

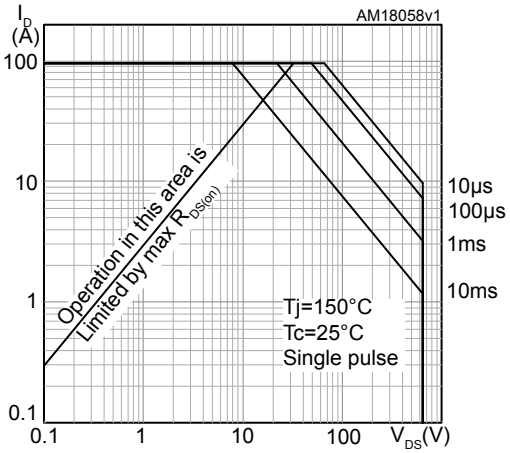


Figure 2. Normalized transient thermal impedance for D²PAK and I²PAK

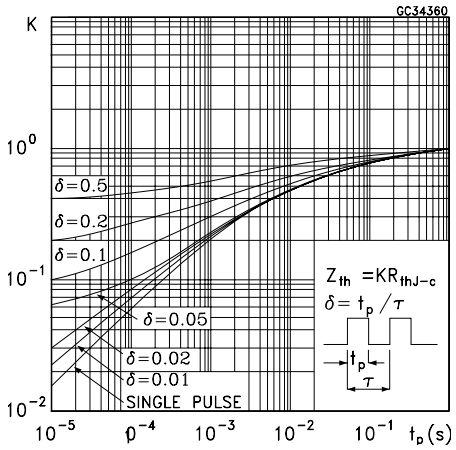


Figure 3. Safe operating area for TO-220FP

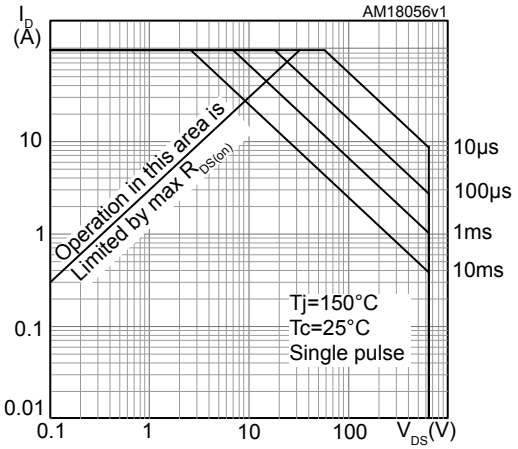


Figure 4. Normalized transient thermal impedance for TO-220FP

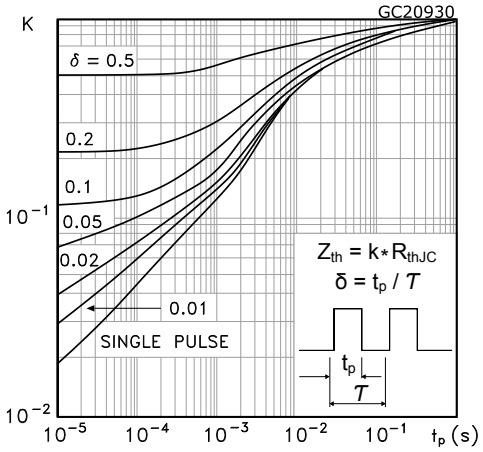


Figure 5. Typical output characteristics

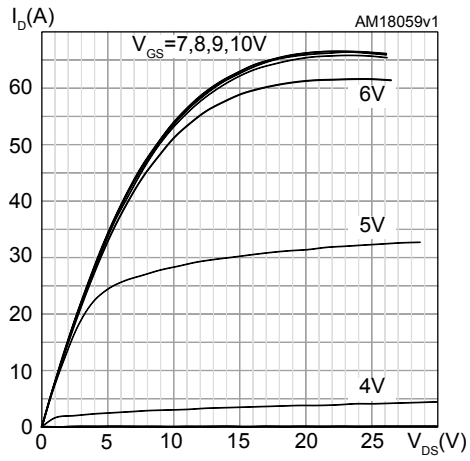


Figure 6. Typical transfer characteristics

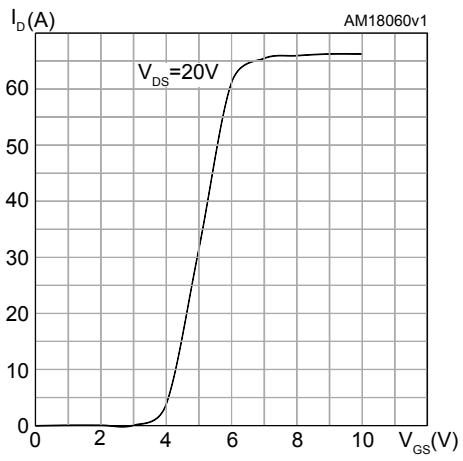


Figure 7. Typical gate charge characteristics

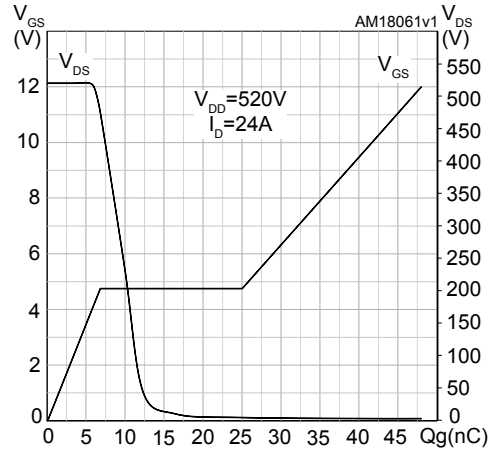


Figure 8. Typical capacitance characteristics

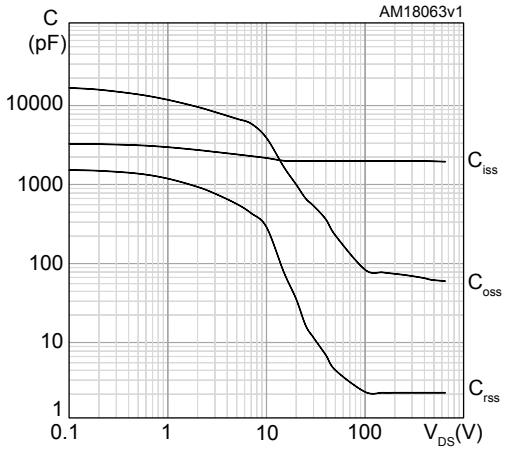


Figure 9. Typical drain-source on-resistance

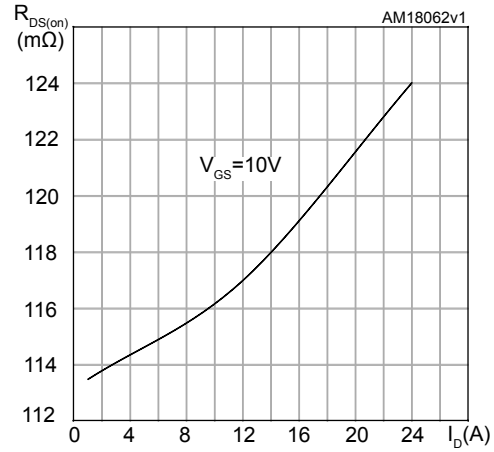


Figure 10. Normalized breakdown voltage vs temperature

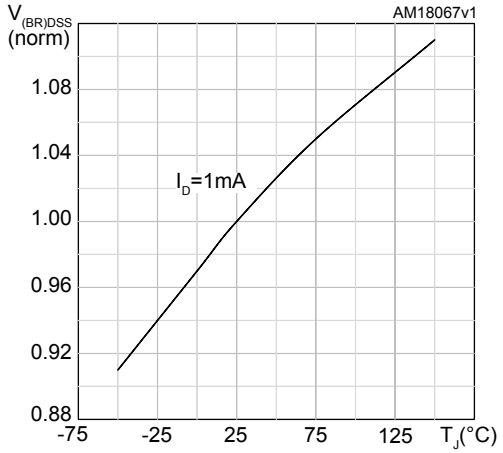


Figure 11. Normalized gate threshold vs temperature

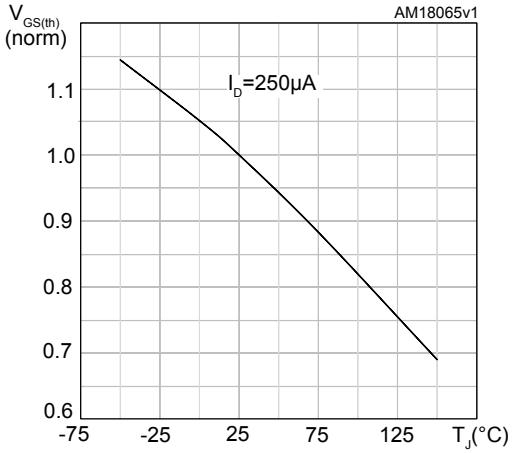


Figure 12. Normalized on-resistance vs temperature

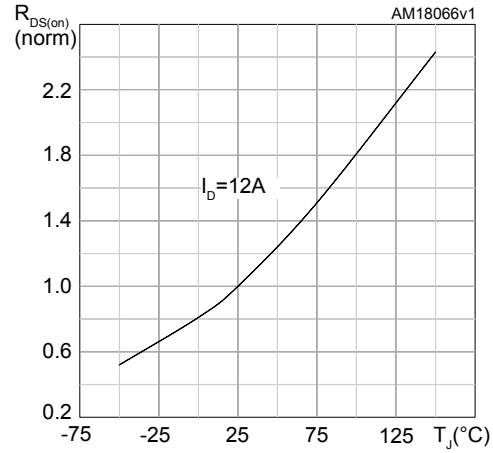


Figure 13. Typical reverse diode forward characteristics

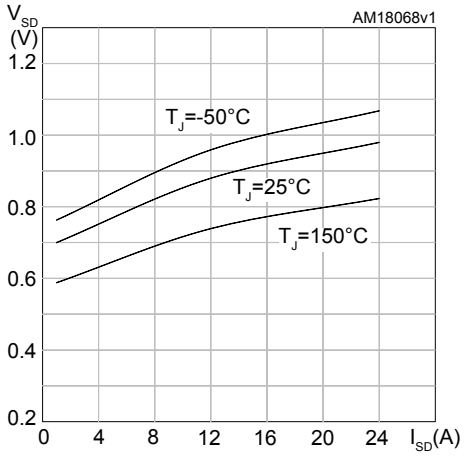
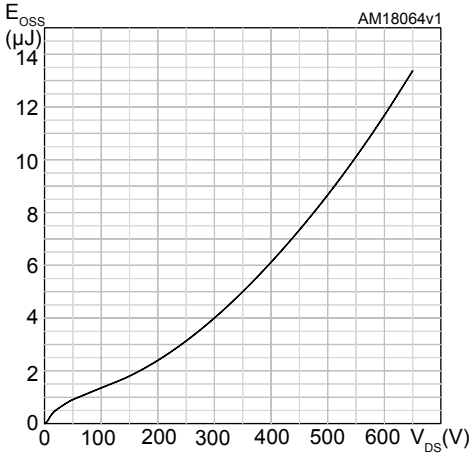
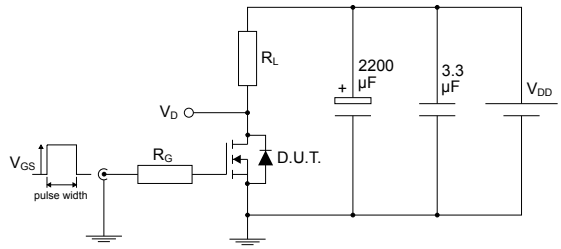


Figure 14. Output capacitance stored energy



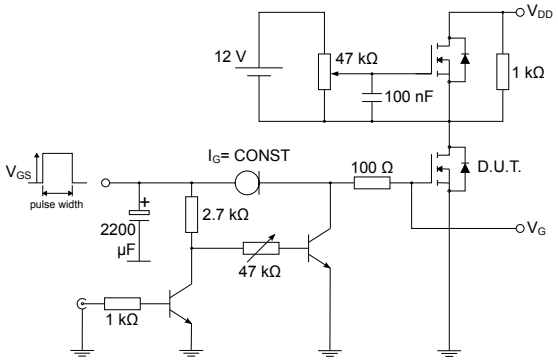
3 Test circuits

Figure 15. Test circuit for resistive load switching times



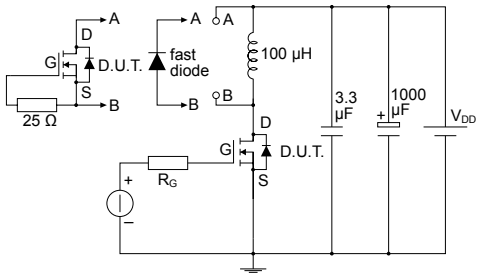
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Figure 16. Test circuit for gate charge behavior



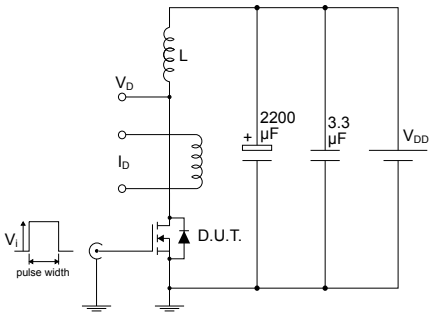
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Figure 17. Test circuit for inductive load switching and diode recovery times



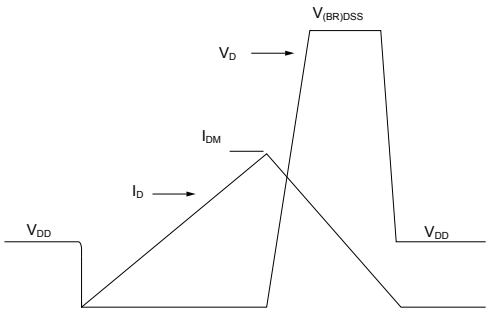
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Figure 18. Unclamped inductive load test circuit



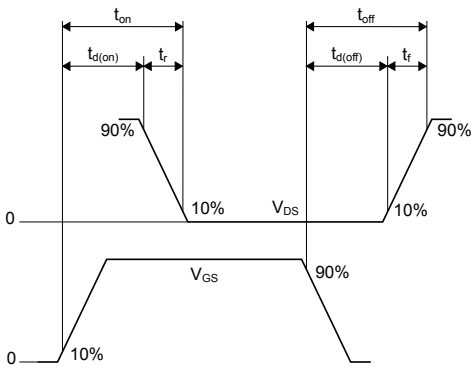
AM01471v1

Figure 19. Unclamped inductive waveform



AM01472v1

Figure 20. Switching time waveform



AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 21. **D²PAK (TO-263) type A package outline**

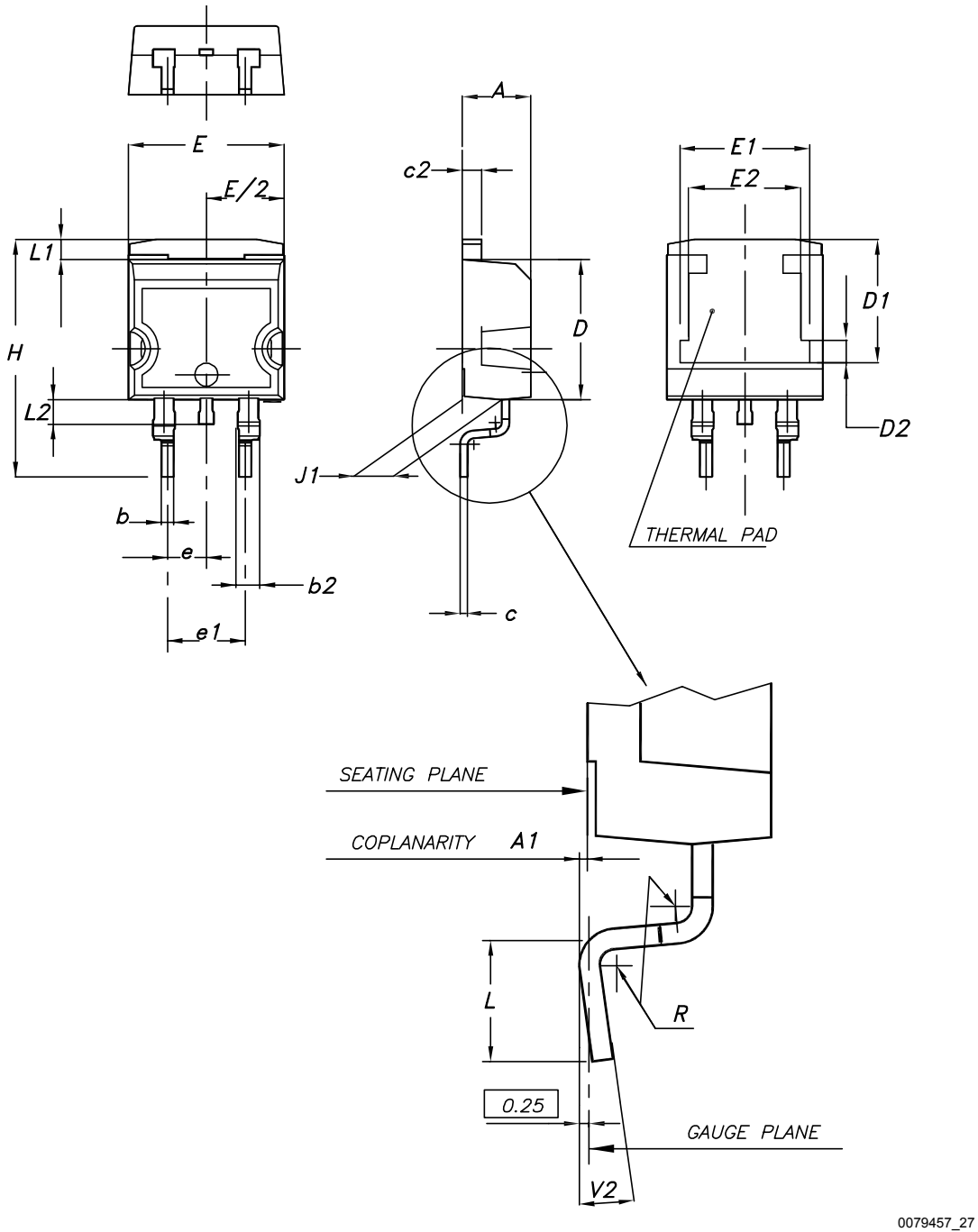
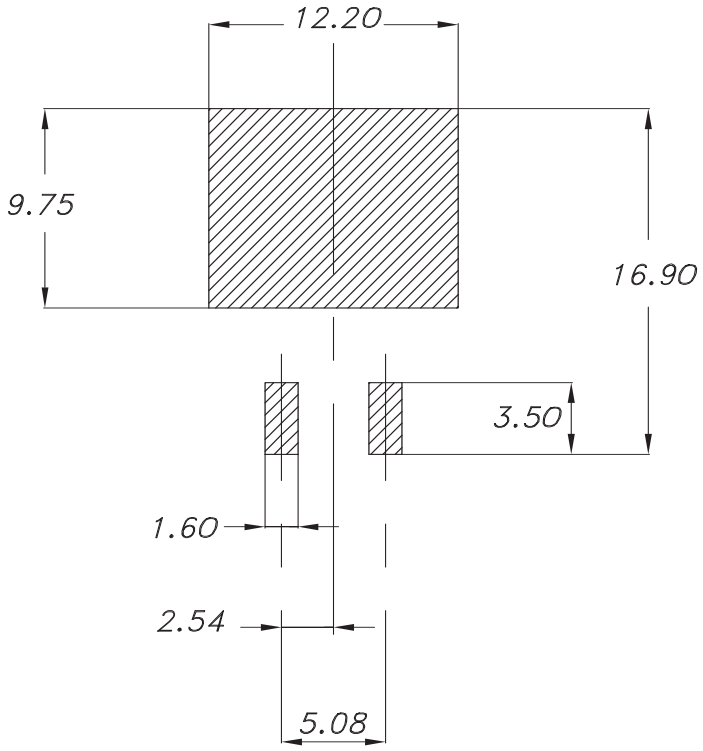


Table 8. D²PAK (TO-263) type A package mechanical data

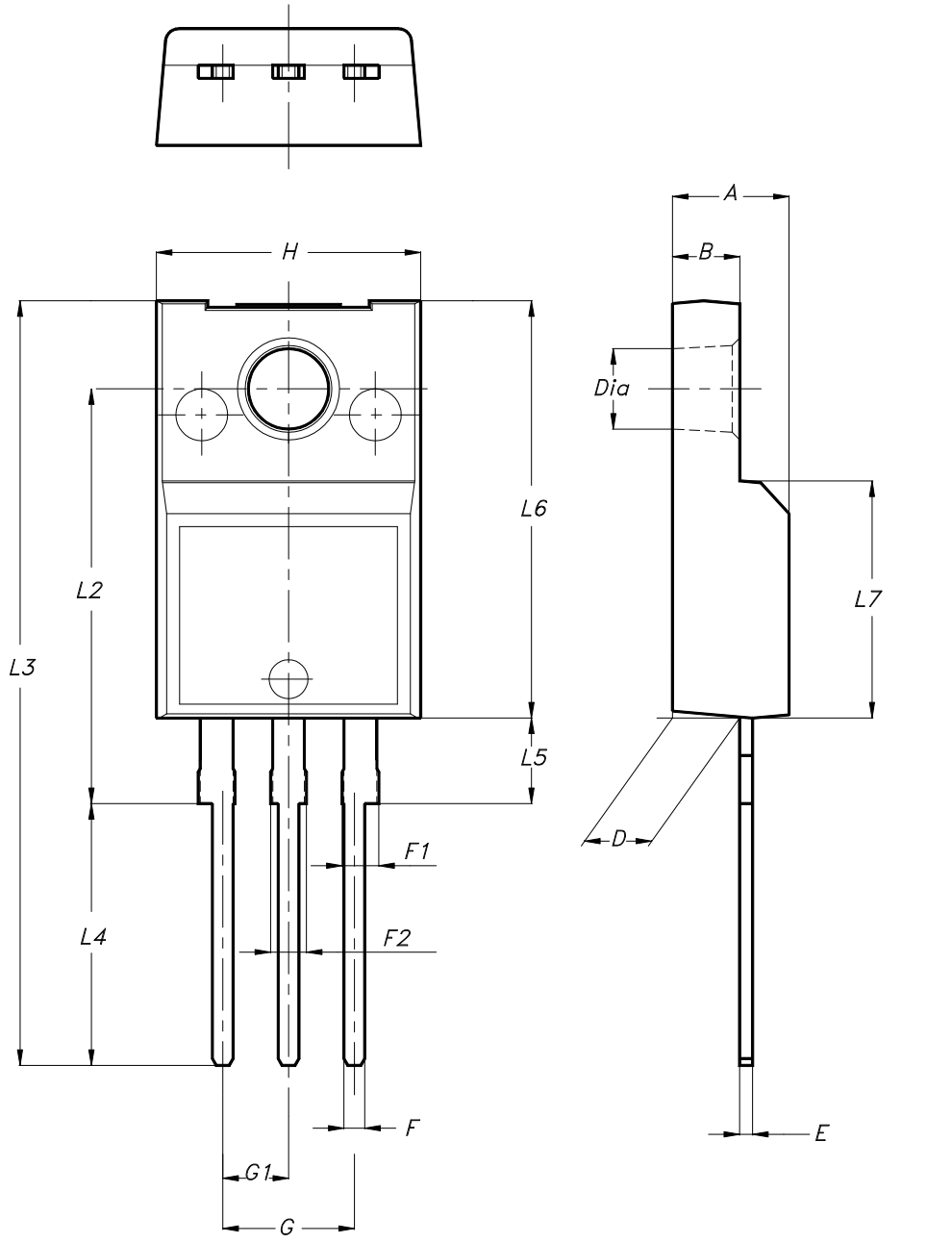
Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 22. D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 TO-220FP type B package information

Figure 23. **TO-220FP type B package outline**



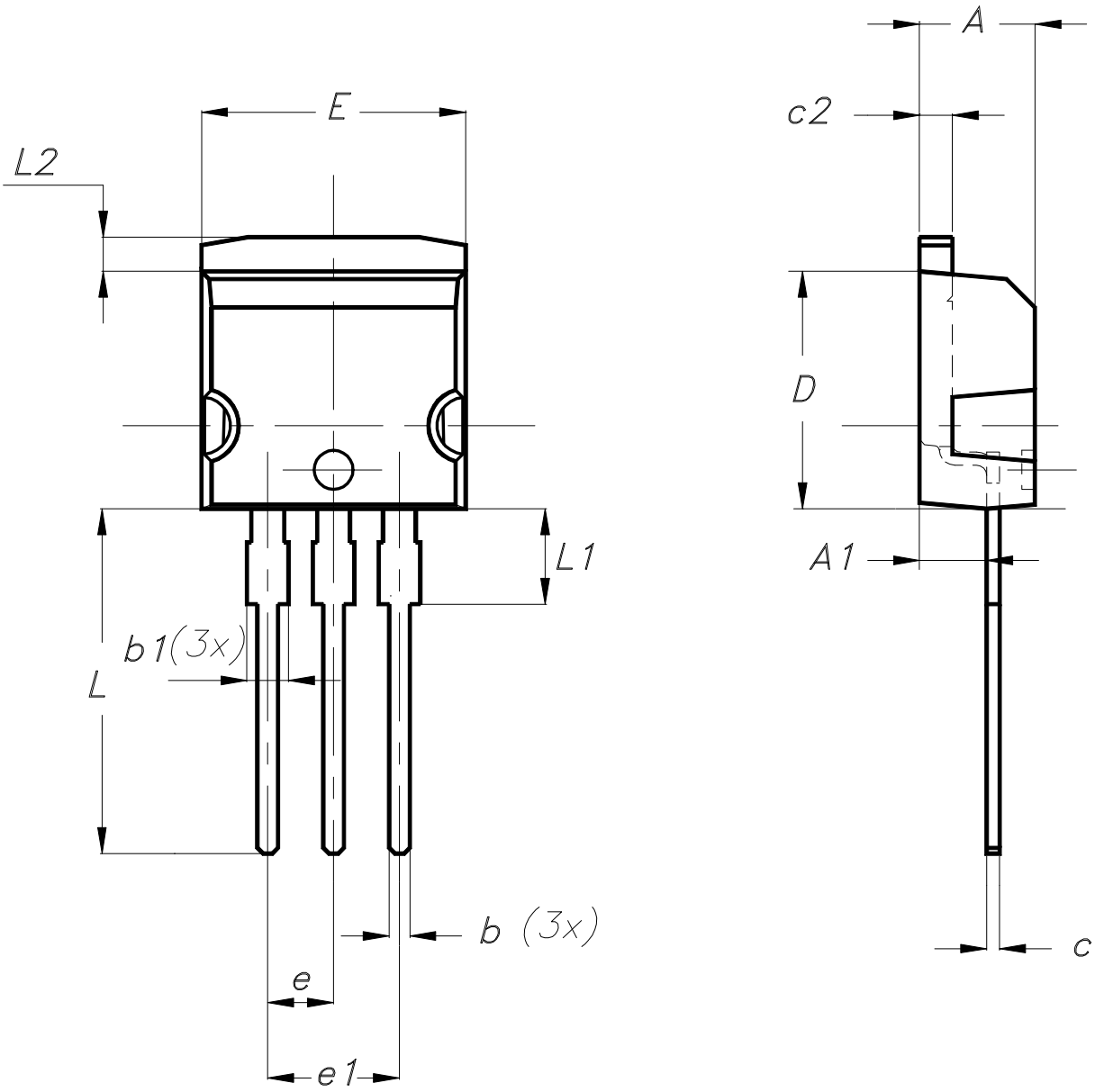
7012510_B_rev.14

Table 9. **TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.3 I²PAK package information

Figure 24. I²PAK package outline



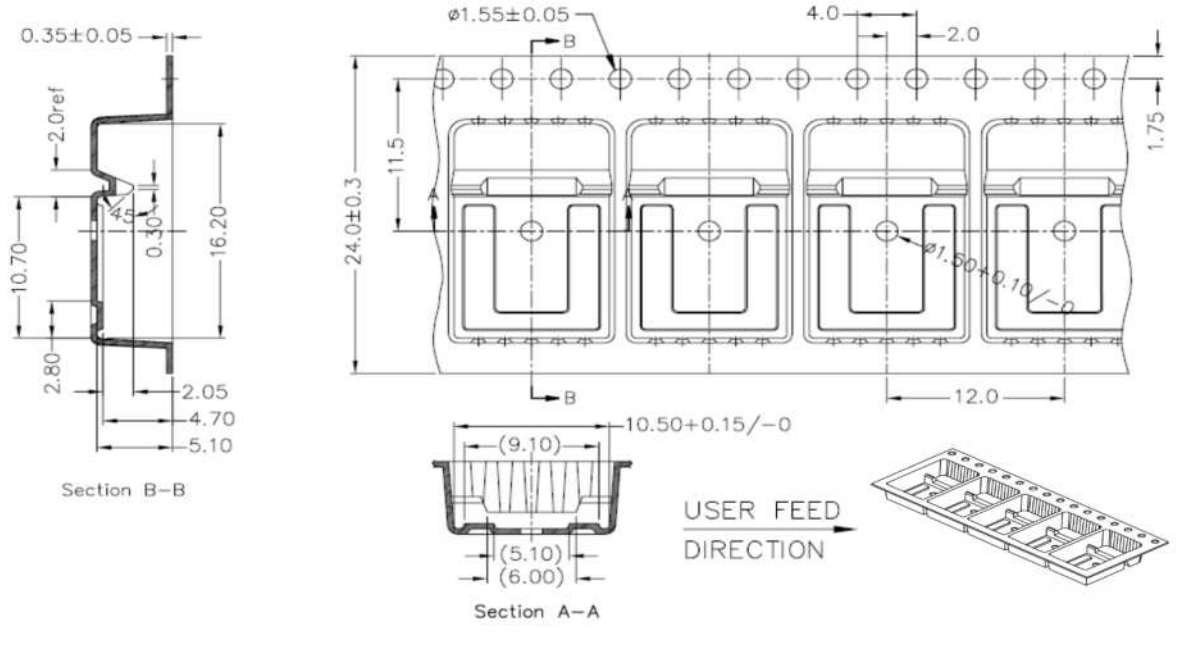
0004982_Rev_10

Table 10. I²PAK package mechanical data

Dim.	mm	
	Min.	Max.
A	4.40	4.60
A1	2.40	2.72
b	0.61	0.88
b1	1.14	1.70
c	0.49	0.70
c2	1.23	1.32
D	8.95	9.35
e	2.40	2.70
e1	4.95	5.15
E	10.00	10.40
L	13.00	14.00
L1	3.50	3.93
L2	1.27	1.40

4.4 D²PAK packing information

Figure 25. **D²PAK tape drawing (dimensions are in mm)**



DM01095771_2

5 Ordering information

Table 11. **Order codes**

Order codes	Marking	Package	Packing
STB33N65M2	33N65M2	D²PAK	Tape and reel
STF33N65M2		TO-220FP	Tube
STI33N65M2		I²PAK	

Revision history

Table 12. **Document revision history**

Date	Revision	Changes
10-Dec-2014	1	First release.
22-Aug-2025	2	Removed order code STP33N65M2. Updated Section 4: Package information. Minor text changes.

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