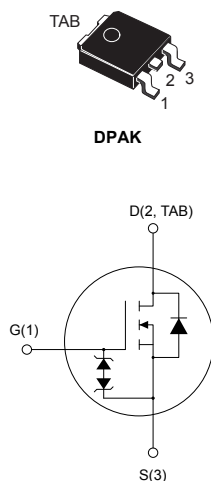


## N-channel 650 V, 370 mΩ typ., 10 A MDmesh M2 Power MOSFET in a DPAK package



AM01476v1\_tab



### Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|------------|----------|-------------------|-------|
| STD13N65M2 | 650 V    | 430 mΩ            | 10 A  |

- Extremely low gate charge
- Excellent output capacitance ( $C_{oss}$ ) profile
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

#### Product status link

[STD13N65M2](#)

#### Product summary

|            |               |
|------------|---------------|
| Order code | STD13N65M2    |
| Marking    | 13N65M2       |
| Package    | DPAK          |
| Packing    | Tape and reel |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol         | Parameter                                                         | Value      | Unit               |
|----------------|-------------------------------------------------------------------|------------|--------------------|
| $V_{GS}$       | Gate-source voltage                                               | $\pm 25$   | V                  |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$  | 10         | A                  |
|                | Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$ | 6.3        |                    |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                                            | 40         | A                  |
| $P_{TOT}$      | Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$     | 110        | W                  |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope                                 | 15         | V/ns               |
| $dv/dt^{(3)}$  | MOSFET $dv/dt$ ruggedness                                         | 50         | V/ns               |
| $T_{stg}$      | Storage temperature range                                         | -55 to 150 | $^{\circ}\text{C}$ |
| $T_J$          | Operating junction temperature range                              |            | $^{\circ}\text{C}$ |

- Pulse width is limited by safe operating area.
- $I_{SD} \leq 10\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS}(\text{peak}) < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .
- $V_{DS} \leq 520\text{ V}$ .

**Table 2. Thermal data**

| Symbol           | Parameter                               | Value | Unit                        |
|------------------|-----------------------------------------|-------|-----------------------------|
| $R_{thJC}$       | Thermal resistance, junction-to-case    | 1.14  | $^{\circ}\text{C}/\text{W}$ |
| $R_{thJA}^{(1)}$ | Thermal resistance, junction-to-ambient | 50    | $^{\circ}\text{C}/\text{W}$ |

- When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 3. Avalanche characteristics**

| Symbol   | Parameter                                                                                                              | Value | Unit |
|----------|------------------------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or non-repetitive (pulse width limited by $T_J$ max.)                                    | 1.8   | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 350   | mJ   |

## 2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

**Table 4. On/off-state**

| Symbol        | Parameter                         | Test conditions                                                                             | Min. | Typ. | Max.     | Unit          |
|---------------|-----------------------------------|---------------------------------------------------------------------------------------------|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                                 | 650  |      |          | V             |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$                                             |      |      | 1        | $\mu\text{A}$ |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$ , $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$ |      |      | 100      |               |
| $I_{GSS}$     | Gate body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$                                          |      |      | $\pm 10$ | $\mu\text{A}$ |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                                          | 2    | 3    | 4        | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 5\text{ A}$                                                 |      | 370  | 430      | m $\Omega$    |

1. Specified by design, not tested in production.

**Table 5. Dynamic**

| Symbol                     | Parameter                     | Test conditions                                                                                                                              | Min. | Typ.  | Max. | Unit     |
|----------------------------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|------|-------|------|----------|
| $C_{iss}$                  | Input capacitance             | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$                                                                         | -    | 590   | -    | pF       |
| $C_{oss}$                  | Output capacitance            |                                                                                                                                              | -    | 27.5  | -    | pF       |
| $C_{rss}$                  | Reverse transfer capacitance  |                                                                                                                                              | -    | 1.1   | -    | pF       |
| $C_{oss\text{ eq.}}^{(1)}$ | Equivalent output capacitance | $V_{DS} = 0\text{ to }520\text{ V}$ , $V_{GS} = 0\text{ V}$                                                                                  | -    | 168.5 | -    | pF       |
| $R_G$                      | Intrinsic gate resistance     | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$                                                                                                      | -    | 6.5   | -    | $\Omega$ |
| $Q_g$                      | Total gate charge             | $V_{DD} = 520\text{ V}$ , $I_D = 10\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$<br>(see Figure 14. Test circuit for gate charge behavior) | -    | 17    | -    | nC       |
| $Q_{gs}$                   | Gate-source charge            |                                                                                                                                              | -    | 3.3   | -    | nC       |
| $Q_{gd}$                   | Gate-drain charge             |                                                                                                                                              | -    | 7     | -    | nC       |

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions                                                                                         | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 325\text{ V}$ , $I_D = 5\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$    | -    | 11   | -    | ns   |
| $t_r$        | Rise time           |                                                                                                         | -    | 7.8  | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time | (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | -    | 38   | -    | ns   |
| $t_f$        | Fall time           |                                                                                                         | -    | 12   | -    | ns   |

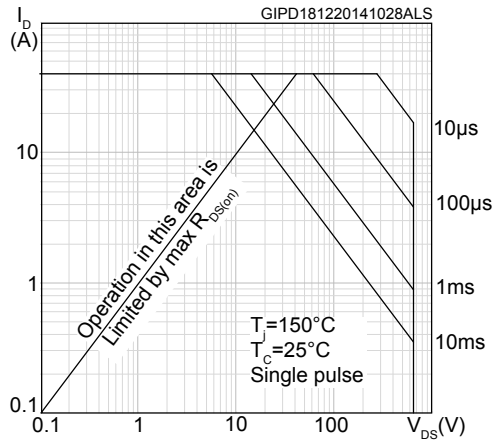
**Table 7. Source-drain diode**

| Symbol          | Parameter                     | Test conditions                                                                                                                                                                                                    | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                                                                                    | -    |      | 10   | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                                    | -    |      | 40   | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 10\text{ A}$ , $V_{GS} = 0\text{ V}$                                                                                                                                                                     | -    |      | 1.6  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 10\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$<br>(see Figure 15. Test circuit for inductive load switching and diode recovery times)                                        | -    | 312  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                    | -    | 2.7  |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                    | -    | 17.5 |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 10\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$<br>(see Figure 15. Test circuit for inductive load switching and diode recovery times) | -    | 464  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                    | -    | 4.1  |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                    | -    | 17.5 |      | A             |

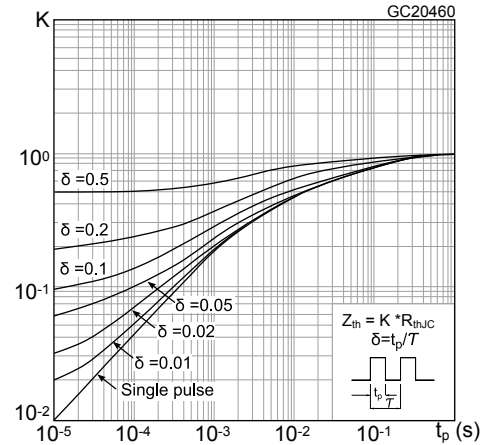
1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

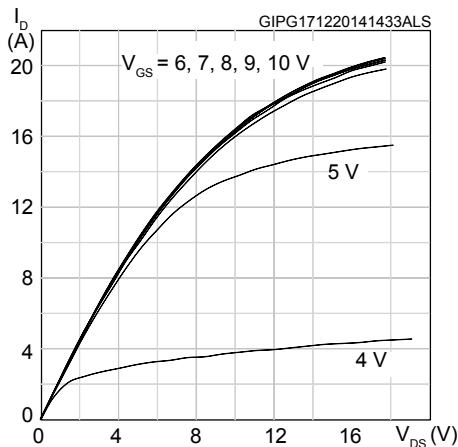
**Figure 1. Safe operating area**



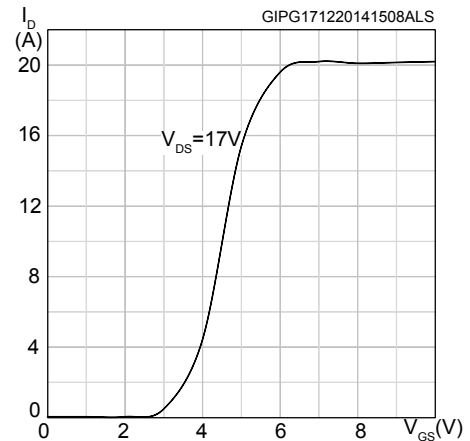
**Figure 2. Normalized transient thermal impedance**



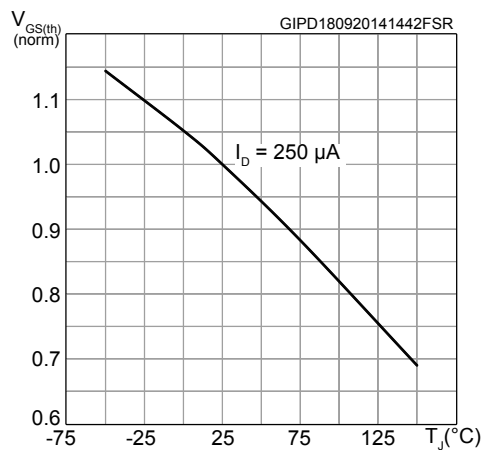
**Figure 3. Typical output characteristics**



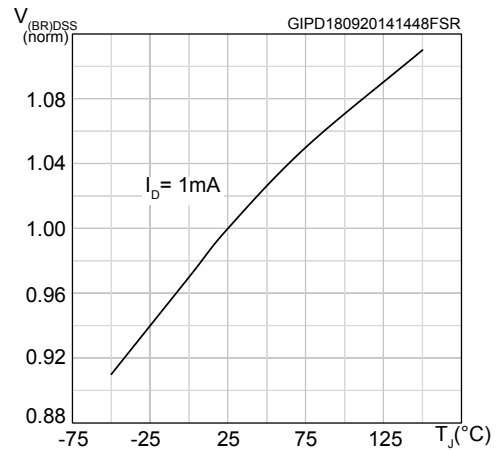
**Figure 4. Typical transfer characteristics**



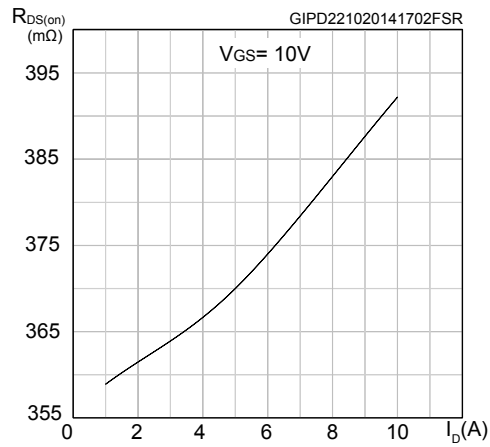
**Figure 5. Normalized gate threshold vs temperature**



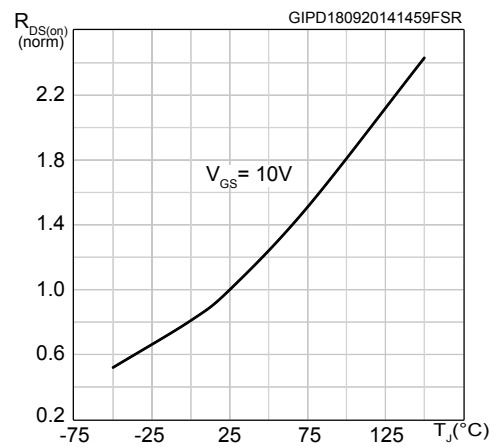
**Figure 6. Normalized breakdown voltage vs temperature**



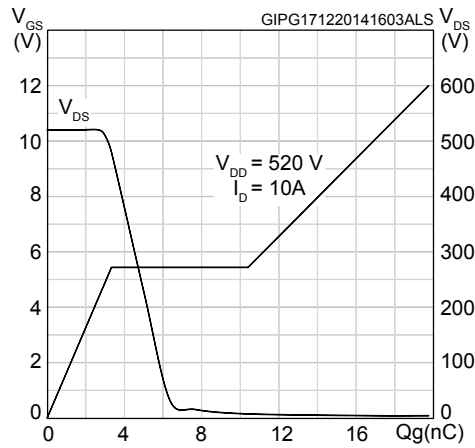
**Figure 7. Typical drain-source on-resistance**



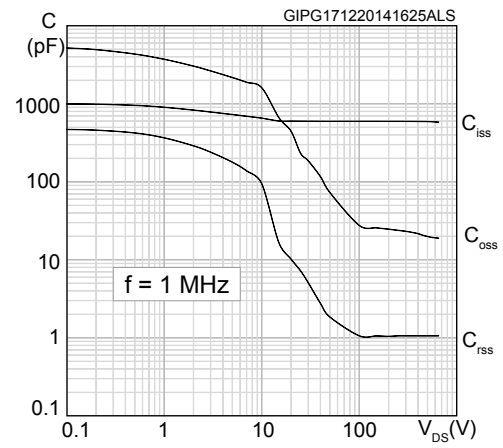
**Figure 8. Normalized on-resistance vs temperature**



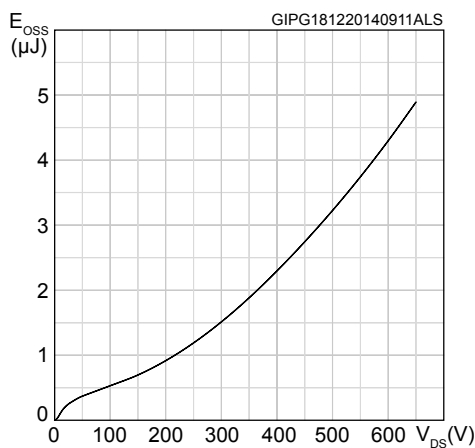
**Figure 9. Typical gate charge characteristics**



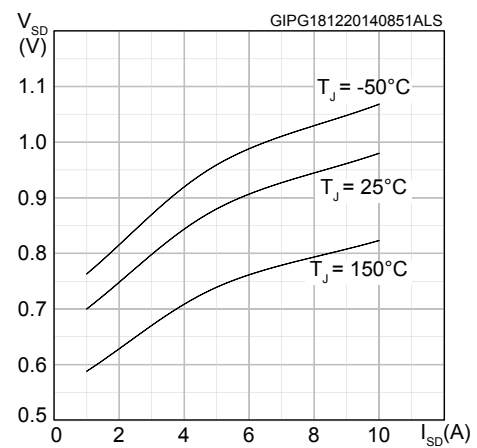
**Figure 10. Typical capacitance characteristics**



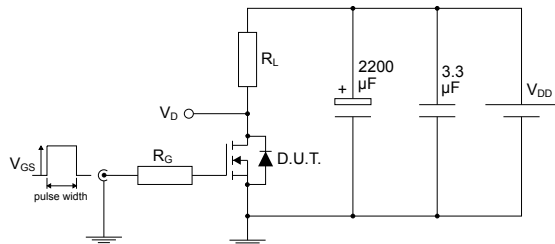
**Figure 11. Typical output capacitance stored energy**



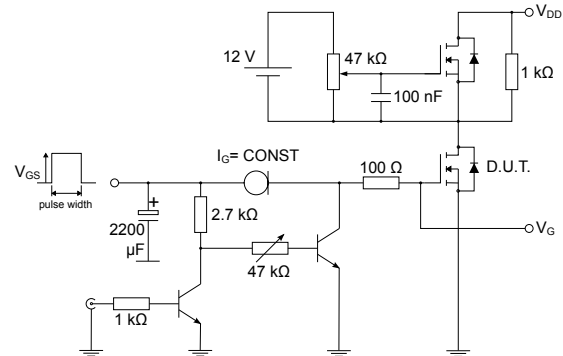
**Figure 12. Typical reverse diode forward characteristics**



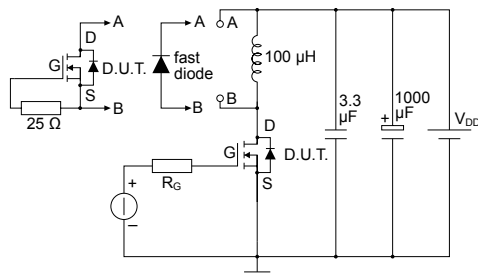
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


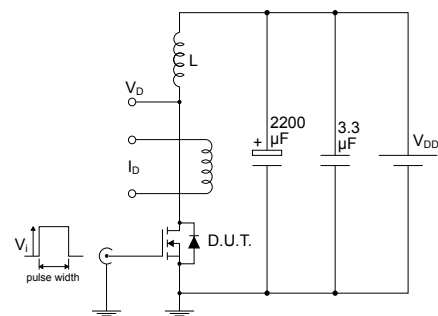
AM01468v1

**Figure 14. Test circuit for gate charge behavior**


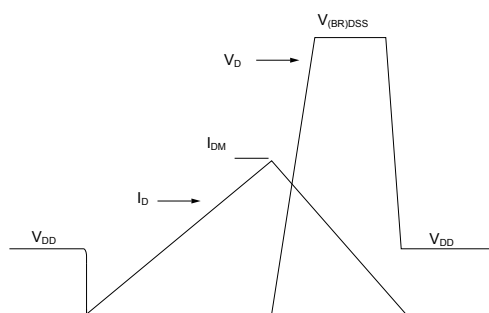
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**Figure 15. Test circuit for inductive load switching and diode recovery times**


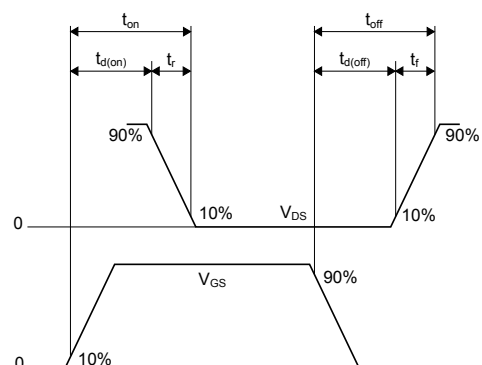
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**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


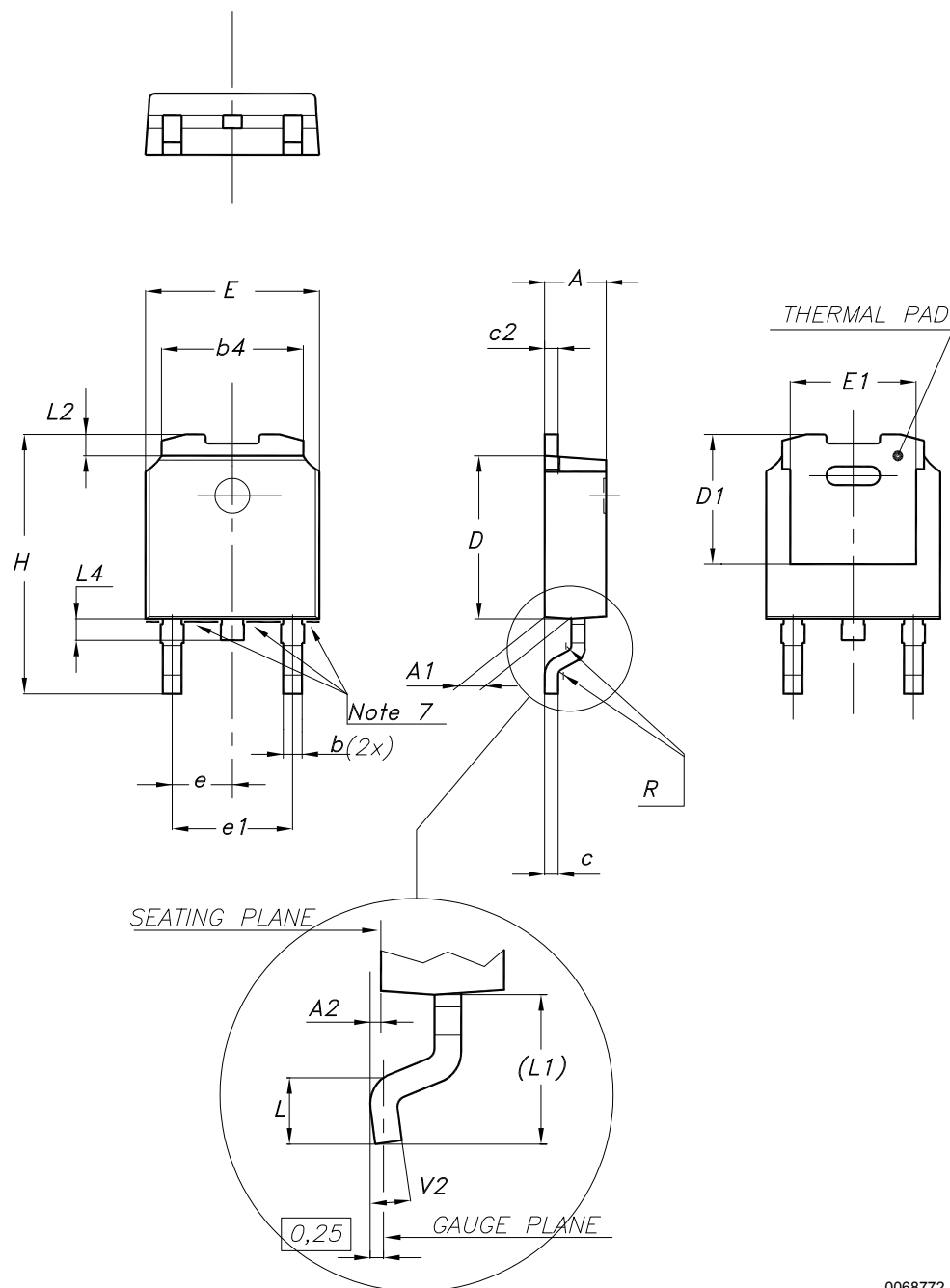
AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 DPAK (TO-252) type A2 package information

**Figure 19. DPAK (TO-252) type A2 package outline**



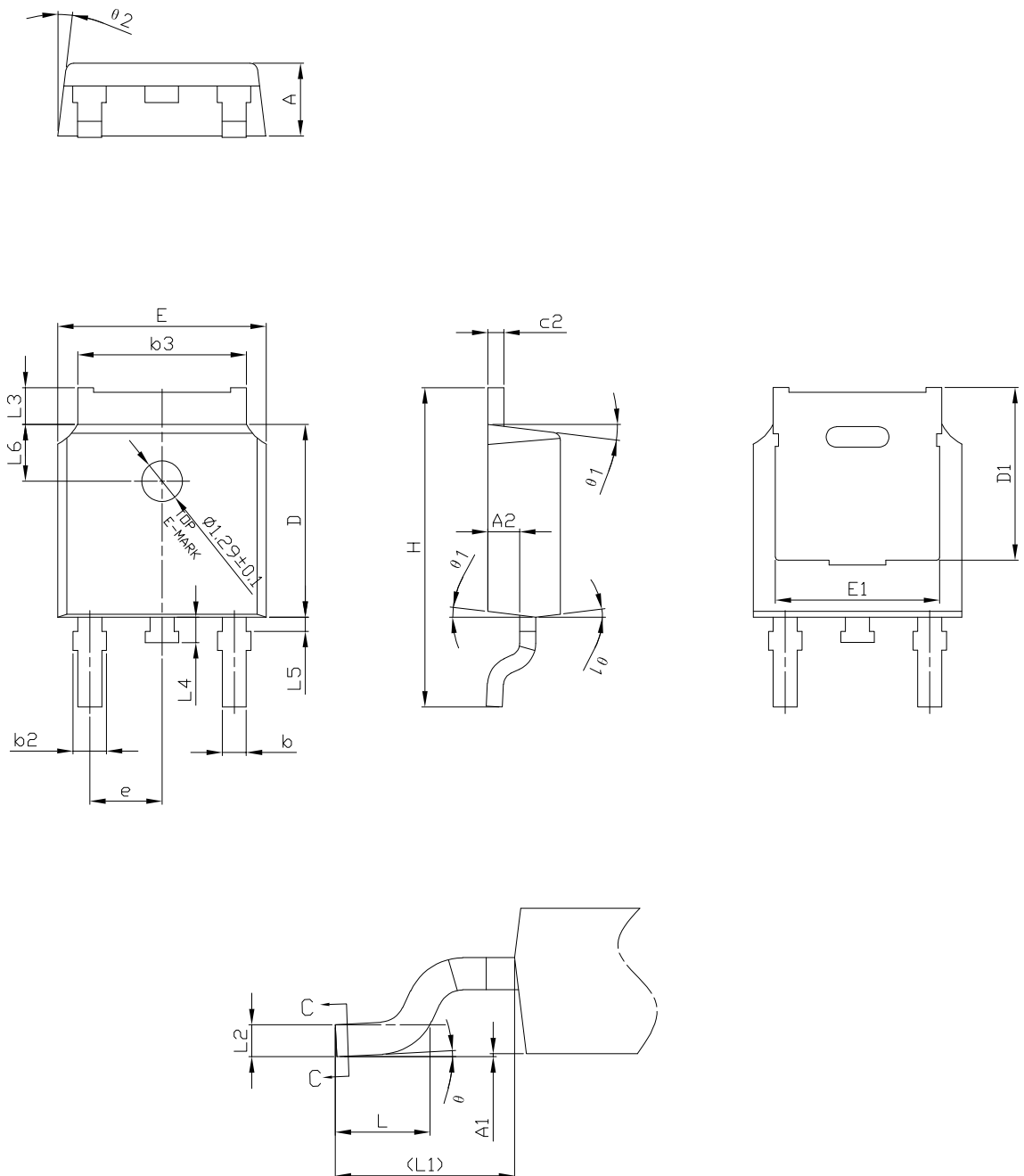
0068772\_type-A2\_rev34

**Table 8. DPAK (TO-252) type A2 mechanical data**

| Dim. | mm    |       |       |
|------|-------|-------|-------|
|      | Min.  | Typ.  | Max.  |
| A    | 2.20  |       | 2.40  |
| A1   | 0.90  |       | 1.10  |
| A2   | 0.03  |       | 0.23  |
| b    | 0.64  |       | 0.90  |
| b4   | 5.20  |       | 5.40  |
| c    | 0.45  |       | 0.60  |
| c2   | 0.48  |       | 0.60  |
| D    | 6.00  |       | 6.20  |
| D1   | 4.95  | 5.10  | 5.25  |
| E    | 6.40  |       | 6.60  |
| E1   | 5.10  | 5.20  | 5.30  |
| e    | 2.159 | 2.286 | 2.413 |
| e1   | 4.445 | 4.572 | 4.699 |
| H    | 9.35  |       | 10.10 |
| L    | 1.00  |       | 1.50  |
| L1   | 2.60  | 2.80  | 3.00  |
| L2   | 0.65  | 0.80  | 0.95  |
| L4   | 0.60  |       | 1.00  |
| R    |       | 0.20  |       |
| V2   | 0°    |       | 8°    |

## 4.2 DPAK (TO-252) type C3 package information

Figure 20. DPAK (TO-252) type C3 package outline



0068772\_type-C3\_rev34

**Table 9. DPAK (TO-252) type C3 mechanical data**

| Dim. | mm       |       |       |
|------|----------|-------|-------|
|      | Min.     | Typ.  | Max.  |
| A    | 2.20     | 2.30  | 2.38  |
| A1   | 0.00     |       | 0.10  |
| A2   | 0.90     | 1.01  | 1.10  |
| b    | 0.72     |       | 0.85  |
| b2   | 0.72     |       | 1.10  |
| b3   | 5.13     | 5.33  | 5.46  |
| c    | 0.47     |       | 0.60  |
| c2   | 0.47     |       | 0.60  |
| D    | 6.00     | 6.10  | 6.20  |
| D1   | 5.20     | 5.45  | 5.70  |
| E    | 6.50     | 6.60  | 6.70  |
| E1   | 5.00     | 5.20  | 5.40  |
| e    | 2.186    | 2.286 | 2.386 |
| H    | 9.80     | 10.10 | 10.40 |
| L    | 1.40     | 1.50  | 1.70  |
| L1   | 2.90 REF |       |       |
| L2   | 0.51 BSC |       |       |
| L3   | 0.90     |       | 1.25  |
| L4   | 0.60     | 0.80  | 1.00  |
| L5   | 0.15     |       | 0.75  |
| L6   | 1.80 REF |       |       |
| θ    | 0°       |       | 8°    |
| θ1   | 5°       | 7°    | 9°    |
| θ2   | 5°       | 7°    | 9°    |

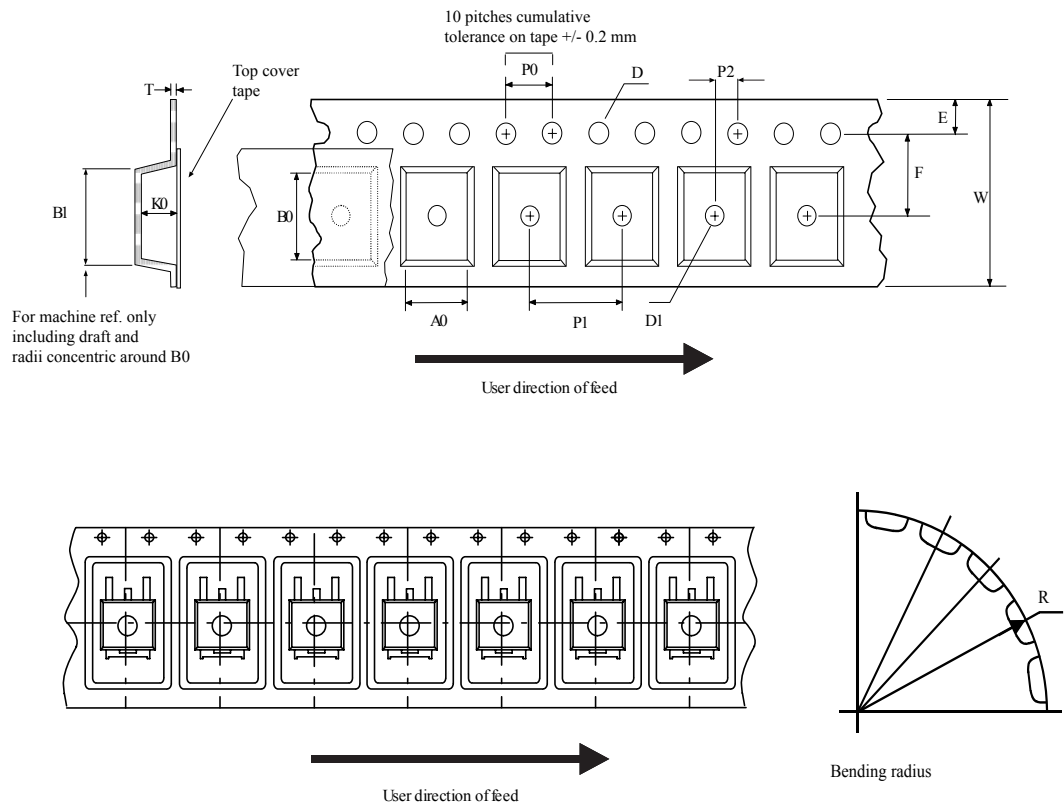
Technical drawing of a mechanical part. The drawing shows a top view and a side view. The top view is a rectangle with a width of 6.3 and a height of 11.2. The side view is a rectangle with a width of 1.5 and a height of 2.9. The part has a central vertical slot with a width of 4.572. The distance from the left edge to the center of the slot is 1.8 MIN. The distance from the center of the slot to the right edge is 6.5. The drawing includes section lines (hatching) and a section line label 'A'.

2) The device must be positioned within  $\oplus 0.05 \text{ A B}$

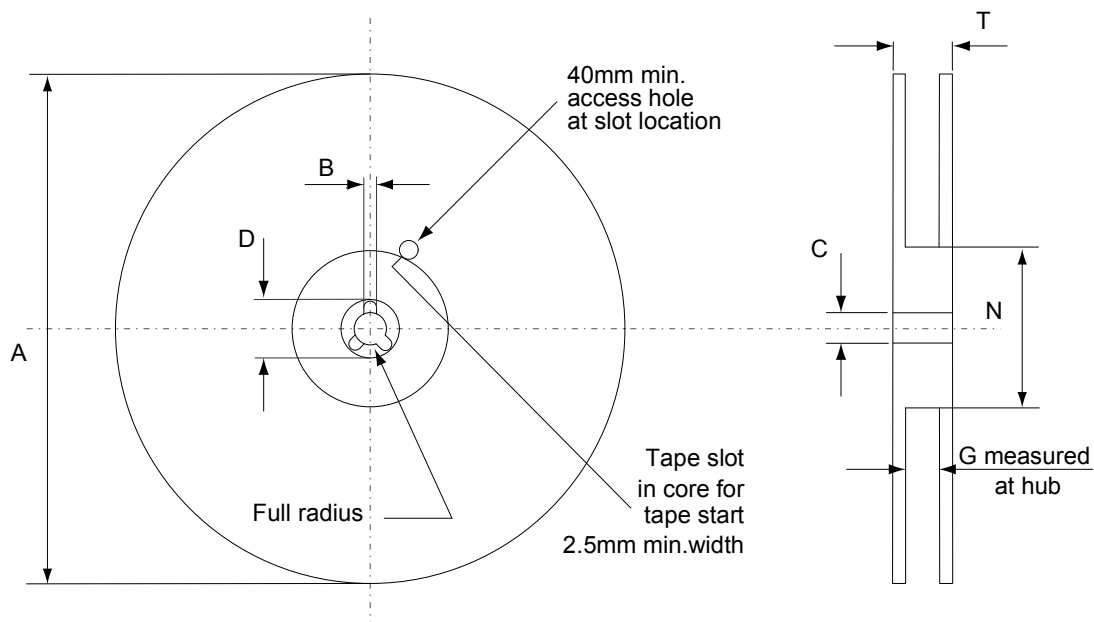
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### 4.3 DPAK (TO-252) packing information

**Figure 22. DPAK (TO-252) tape outline**



AM08852v1

**Figure 23. DPAK (TO-252) reel outline**


AM06038v1

**Table 10. DPAK (TO-252) tape and reel mechanical data**

| Tape |      |      | Reel      |      |      |
|------|------|------|-----------|------|------|
| Dim. | mm   |      | Dim.      | mm   |      |
|      | Min. | Max. |           | Min. | Max. |
| A0   | 6.8  | 7    | A         |      | 330  |
| B0   | 10.4 | 10.6 | B         | 1.5  |      |
| B1   |      | 12.1 | C         | 12.8 | 13.2 |
| D    | 1.5  | 1.6  | D         | 20.2 |      |
| D1   | 1.5  |      | G         | 16.4 | 18.4 |
| E    | 1.65 | 1.85 | N         | 50   |      |
| F    | 7.4  | 7.6  | T         |      | 22.4 |
| K0   | 2.55 | 2.75 |           |      |      |
| P0   | 3.9  | 4.1  | Base qty. |      | 2500 |
| P1   | 7.9  | 8.1  | Bulk qty. |      | 2500 |
| P2   | 1.9  | 2.1  |           |      |      |
| R    | 40   |      |           |      |      |
| T    | 0.25 | 0.35 |           |      |      |
| W    | 15.7 | 16.3 |           |      |      |

## Revision history

**Table 11. Document revision history**

| Date        | Revision | Changes                                                                                                                            |
|-------------|----------|------------------------------------------------------------------------------------------------------------------------------------|
| 18-Dec-2014 | 1        | First release.                                                                                                                     |
| 06-Oct-2023 | 2        | Updated Figure 12. Typical reverse diode forward characteristics.<br>Updated Section 4 Package information.<br>Minor text changes. |

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