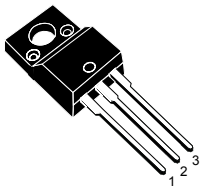
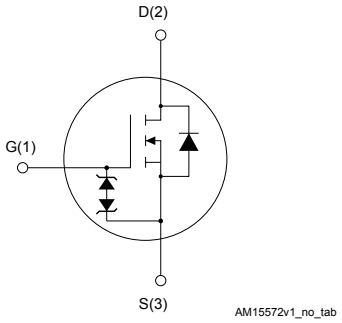
STFU28N65M2

Datasheet

N-channel 650 V, 150 mΩ typ., 20 A MDmesh M2 Power MOSFET in a TO-220FP ultra narrow leads package



TO-220FP
ultra narrow leads



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STFU28N65M2	650 V	180 mΩ	20 A

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using MDmesh M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Product status link
STFU28N65M2

Product summary	
Order code	STFU28N65M2
Marking	28N65M2
Package	TO-220FP ultra narrow leads
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	20	A
	Drain current (continuous) at T_C = 100 °C	13	
I_{DM}(1)	Drain current (pulsed)	80	A
P_{TOT}	Total power dissipation at T_C = 25 °C	30	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	2.5	kV
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 20 A, di/dt ≤ 400 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 520 V.*
3. *V_{DD} ≤ 520 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	4.17	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	2.4	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	760	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 10 A		150	180	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 100 V, f = 1 MHz, V_{GS} = 0 V	-	1440	-	pF
C_{oss}	Output capacitance		-	60	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	307	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	4.9	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 20 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	35	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain charge		-	15	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 10 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	13.4	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off-delay time		-	59	-	ns
t_f	Fall time		-	8.8	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		20	A
I_{SDM} (1)	Source-drain current (pulsed)		-		80	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 20 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 20 A, di/dt = 100 A/µs,	-	384		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V	-	5.7		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	30		A
t_{rr}	Reverse recovery time	I_{SD} = 20 A, di/dt = 100 A/µs,	-	544		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_J = 150 °C	-	8.2		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	30.5		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

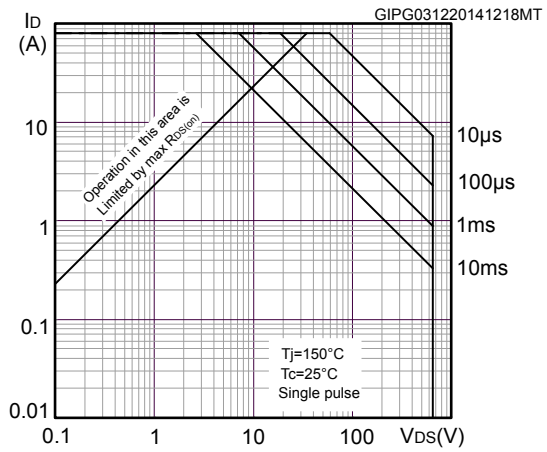


Figure 2. Normalized transient thermal impedance

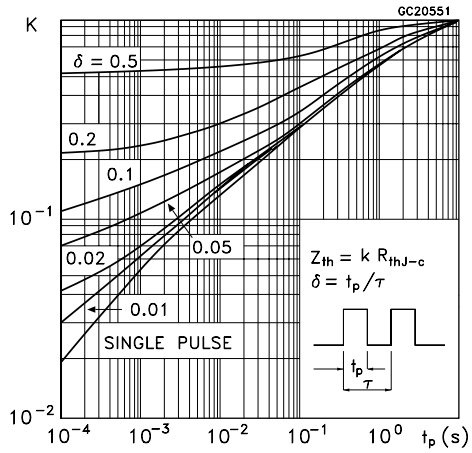


Figure 3. Typical output characteristics

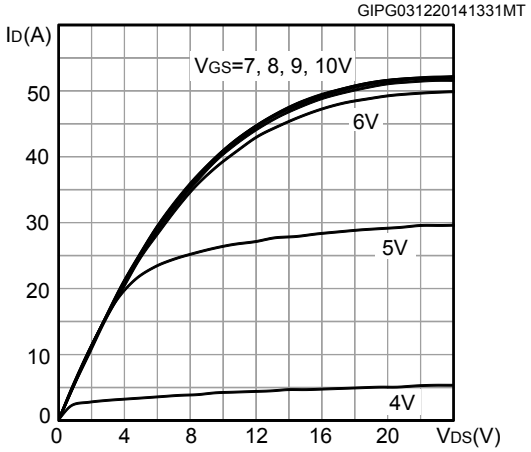


Figure 4. Typical transfer characteristics

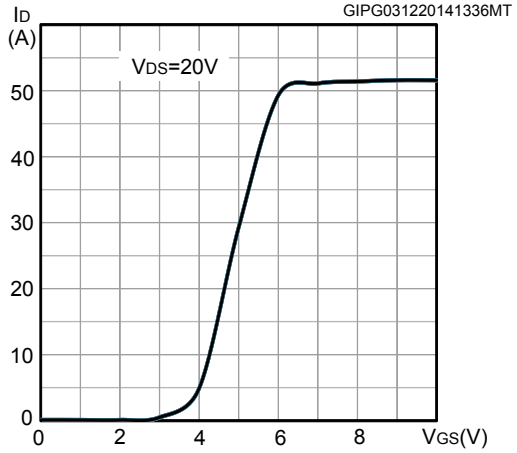


Figure 5. Normalized gate threshold vs temperature

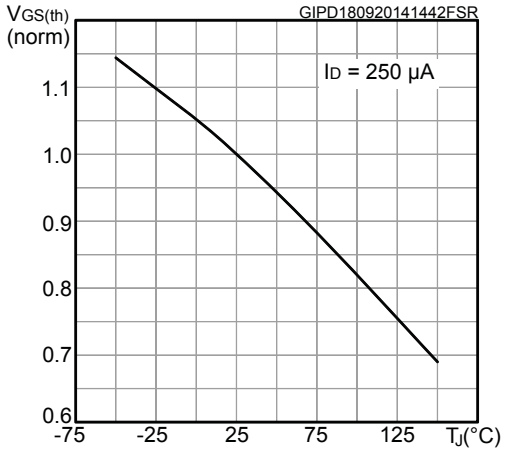


Figure 6. Normalized breakdown voltage vs temperature

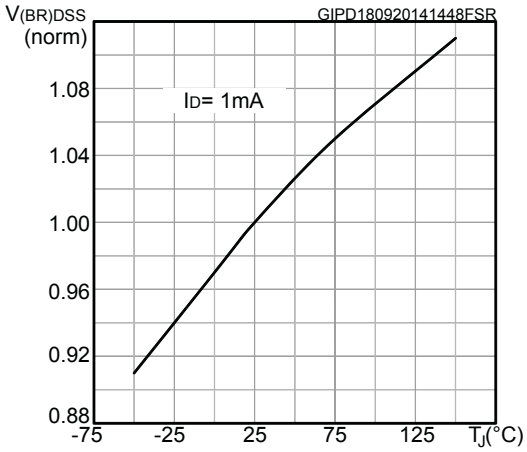


Figure 7. Typical drain-source on-resistance

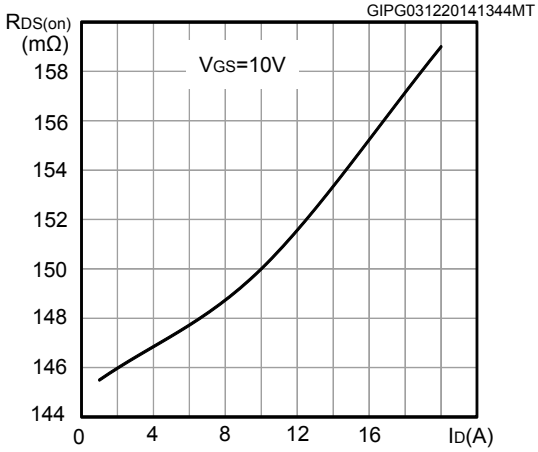


Figure 8. Normalized on-resistance vs temperature

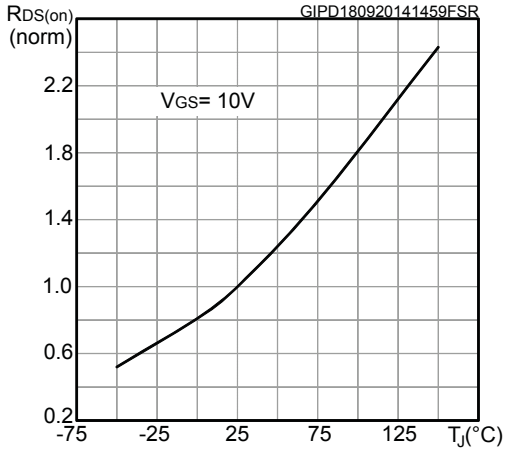


Figure 9. Typical gate charge characteristics

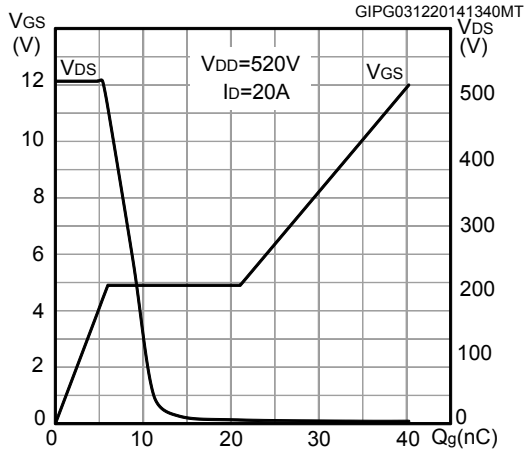


Figure 10. Typical capacitance characteristics

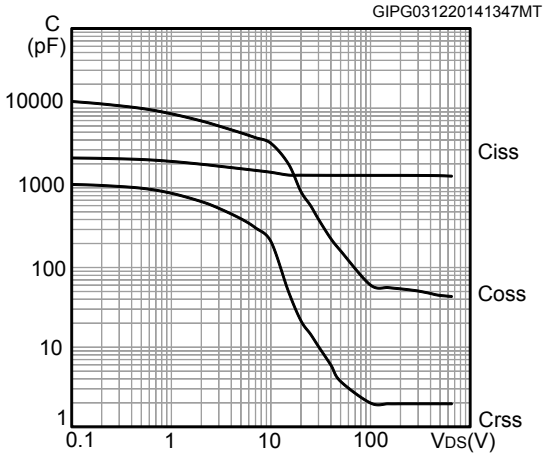


Figure 11. Typical output capacitance stored energy

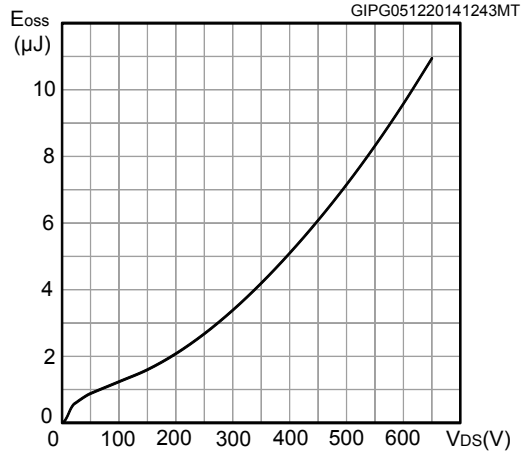
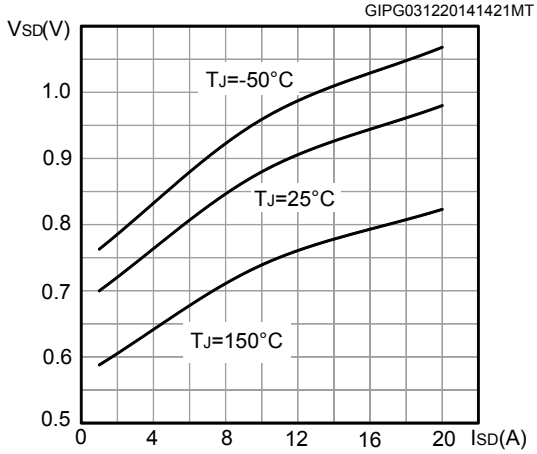


Figure 12. Typical reverse diode forward characteristics



3 Test circuits

Figure 13. Test circuit for resistive load switching times

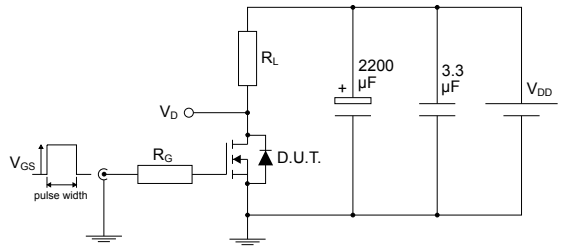


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Figure 14. Test circuit for gate charge behavior

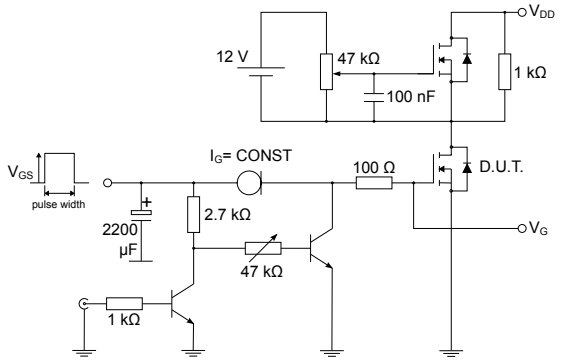

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Figure 15. Test circuit for inductive load switching and diode recovery times

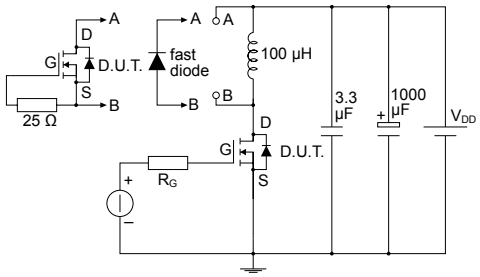

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Figure 16. Unclamped inductive load test circuit

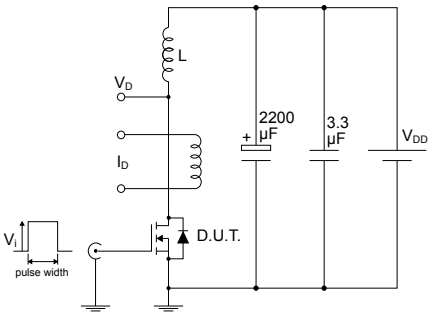

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Figure 17. Unclamped inductive waveform

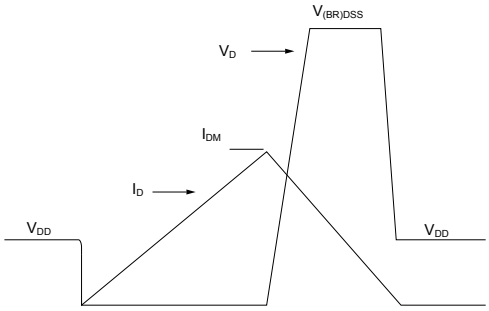

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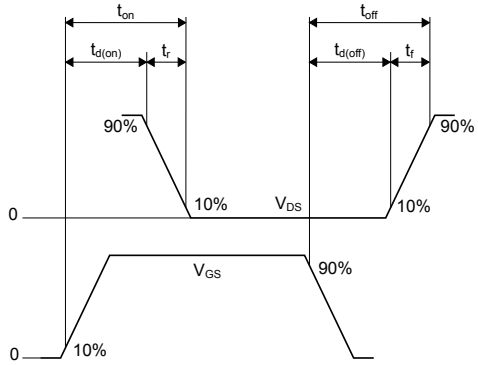
Figure 18. Switching time waveform



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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP ultra narrow leads package information

Figure 19. TO-220FP ultra narrow leads package outline

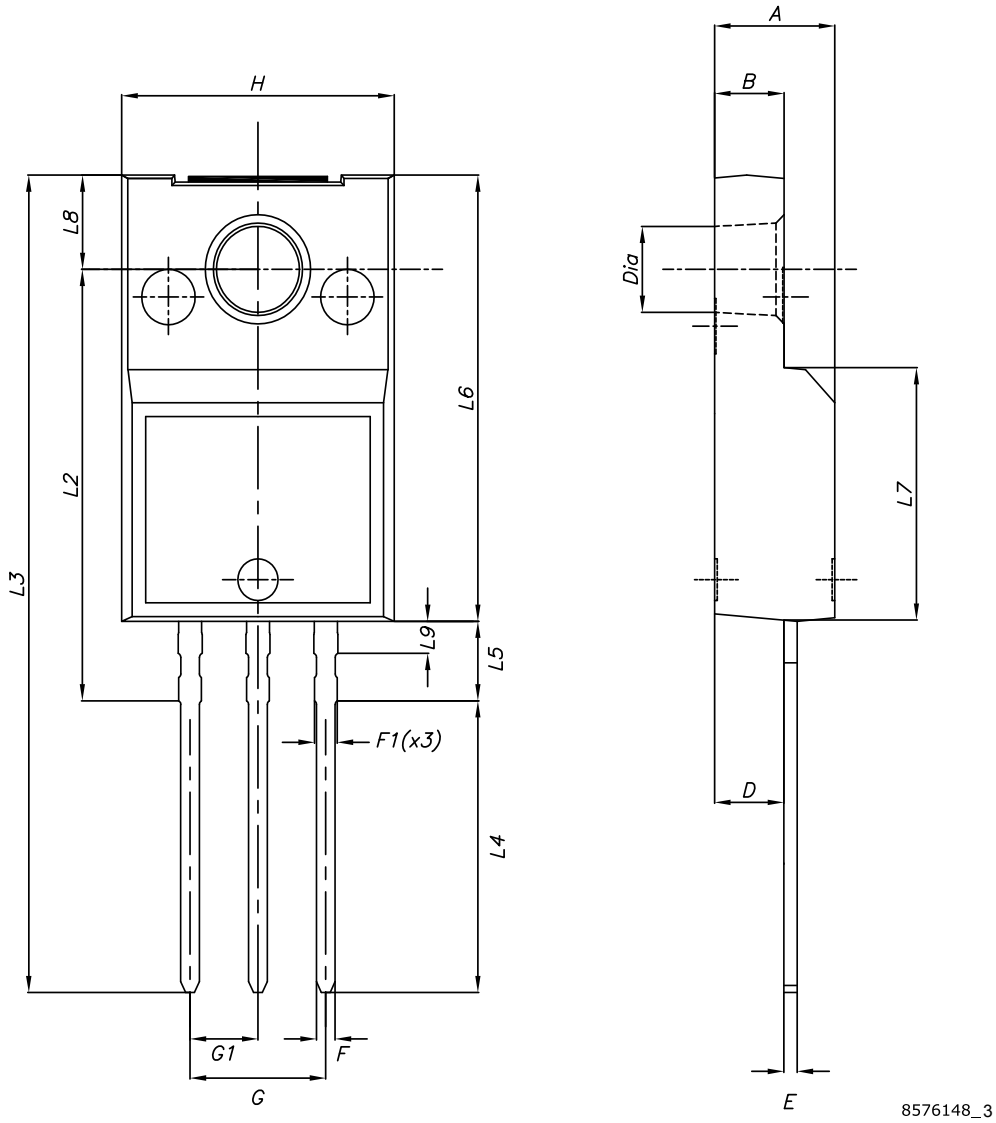

Table 8. **TO-220FP ultra narrow leads mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.60
F	0.65		0.75
F1	-		0.90
G	4.95		5.20
G1	2.40	2.54	2.70
H	10.00		10.40
L2	15.10		15.90
L3	28.50		30.50
L4	10.20		11.00
L5	2.50		3.10
L6	15.60		16.40
L7	9.00		9.30
L8	3.20		3.60
L9	-		1.30
Dia.	3.00		3.20

Revision history

Table 9. Document revision history

Date	Revision	Changes
09-Mar-2015	1	Initial release.
07-Oct-2015	2	Document status promoted from preliminary to production data.
12-Nov-2015	3	Updated *Figure 1: "Internal schematic diagram"* in cover page. Updated *Table 3: "Thermal data"*. Minor text changes.
08-Apr-2026	4	Updated Section 4.1: TO-220FP ultra narrow leads package information. Minor text changes.

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