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I3G4250D

Datasheet

MEMS motion sensor: 3-axis digital output gyroscope



LGA-16L
4 x 4 x 1.1 mm³

Product status link
I3G4250D

Product summary	
Order code	I3G4250DTR
Temperature range [°C]	-40 to +85
Package	LGA-16L (4 x 4 x 1.1 mm³)
Packing	Tape and reel

Product resources
TN0018 (design and soldering)

Product label
LONGEVITY 10 YEARS COMMITMENT

Features

- Wide supply voltage: 2.4 V to 3.6 V
- Selectable full scale (±245/±500/±2000 dps)
- I²C/SPI digital output interface
- 16-bit rate value data output
- 8-bit temperature data output
- Two digital output lines (interrupt and data ready)
- Integrated low-pass and high-pass filters with user-selectable bandwidth
- Ultrastable over temperature and time
- Low-voltage-compatible I/Os (1.8 V)
- Embedded power-down and sleep mode
- Embedded temperature sensor
- Embedded FIFO
- High shock survivability
- Extended operating temperature range (-40°C to +85°C)
- ECOPACK and RoHS compliant

Applications

- Industrial applications
- Navigation systems and telematics
- Motion control with MMI (man-machine interface)
- Appliances and robotics

Description

The I3G4250D is a low-power 3-axis angular rate sensor able to provide unprecedented stability at zero-rate level and sensitivity over temperature and time. It includes a sensing element and an IC interface capable of providing the measured angular rate to the application through a standard SPI digital interface. An I²C compatible interface is also available.

The sensing element is manufactured using a dedicated micromachining process developed by STMicroelectronics to produce inertial sensors and actuators on silicon wafers.

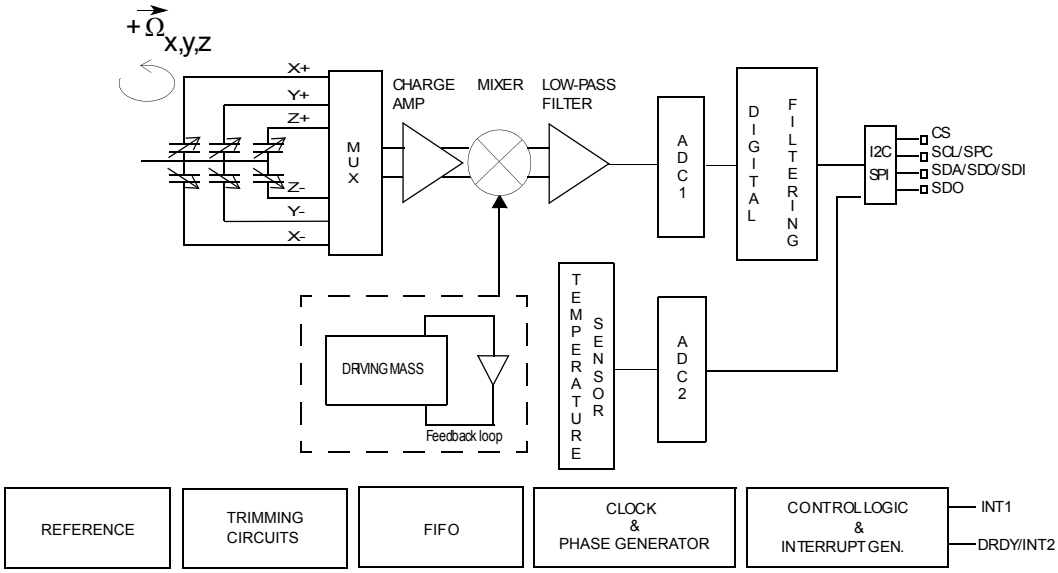
The IC interface is manufactured using a CMOS process that allows a high level of integration to design a dedicated circuit that is trimmed to better match the characteristics of the sensing element.

The device has a selectable full scale (±245/±500/±2000 dps) and is capable of measuring rates with a user-selectable bandwidth.

The I3G4250D is available in a plastic, land grid array (LGA) package and operates within a temperature range of -40°C to +85°C.

1 Block diagram and pin description

Figure 1. Block diagram



The vibration of the structure is maintained by the drive circuitry in a feedback loop. The sensing signal is filtered and appears as a digital signal at the output.

1.1 Pin description

Figure 2. **Pin connections**

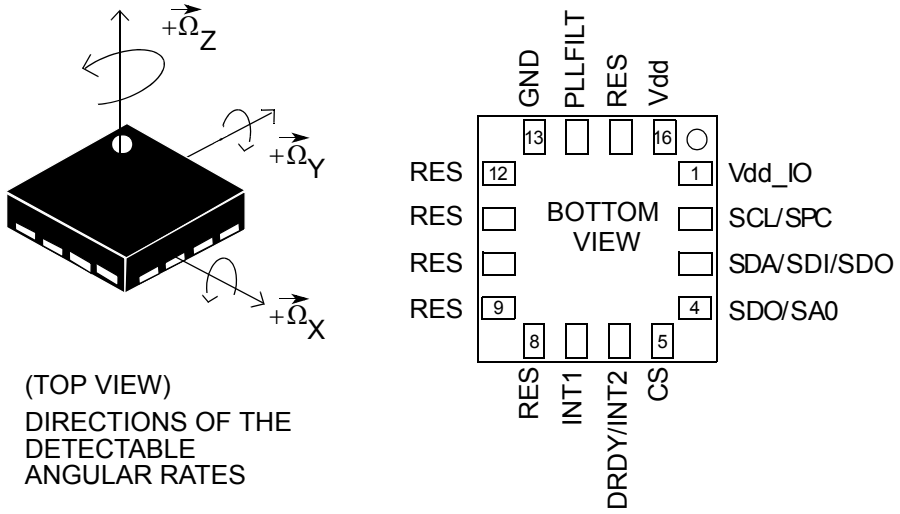
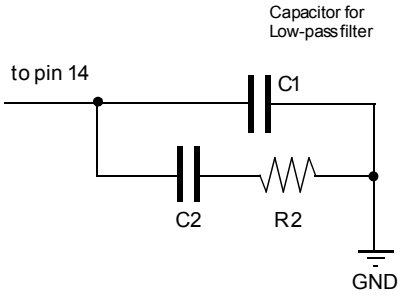


Table 1. **Pin description**

Pin#	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	SCL SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
3	SDA SDI SDO	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
4	SDO SA0	SPI serial data output (SDO) I²C least significant bit of the device address (SA0)
5	CS	Enable SPI I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)
6	DRDY/INT2	Data ready / FIFO interrupt
7	INT1	Programmable interrupt
8	Reserved	Connect to GND
9	Reserved	Connect to GND
10	Reserved	Connect to GND
11	Reserved	Connect to GND
12	Reserved	Connect to GND
13	GND	0 V supply
14	PLLFILT	Phase-locked loop filter (see Figure 3)
15	Reserved	Connect to Vdd
16	Vdd	Power supply

Figure 3. **I3G4250D external low-pass filter**



Note: Pin 14 PLLFILT maximum voltage level is equal to Vdd.

Table 2. **Filter values**

Parameter	Typical value
C1	10 nF
C2	470 nF
R2	10 kΩ

2 Mechanical and electrical characteristics

2.1 Mechanical characteristics

@Vdd = 3.0 V, T = +25°C, unless otherwise noted. The product is factory calibrated at 3.0 V. The operational power supply range is specified in the following table.

Table 3. Mechanical characteristics

Symbol	Parameter	Test condition	Min.(1)	Typ.(2)	Max.(1)	Unit
FS	Measurement range(3)	User-selectable		±245		dps
				±500		
				±2000		
So	Sensitivity(4)	FS = ±245 dps	7.4	8.75	10.1	mdps/digit
		FS = ±500 dps	14.8	17.50	19.8	
		FS = ±2000 dps	59.2	70	79.3	
SoDr	Sensitivity change vs. temperature	From -40°C to +85°C		±2		%
DVoff	Digital zero-rate level(4)	FS = ±245 dps	-25	±10	+25	dps
		FS = ±500 dps	-37.5	±15	+37.5	
		FS = ±2000 dps	-187.5	±75	+187.5	
OffDr	Zero-rate level change vs. temperature	FS = ±245 dps		±0.03		dps/°C
		FS = ±2000 dps		±0.04		
NL	Nonlinearity(3)	Best-fit straight line	-5	0.2	+5	% FS
DST	Self-test output change	FS = ±245 dps		130		dps
		FS = ±500 dps		200		
		FS = ±2000 dps		530		
Rn	Rate noise density	BW = 50 Hz		0.03		dps/√Hz
ODR	Digital output data rate			105/208/ 420/840		Hz
Top	Operating temperature range		-40		+85	°C

1. *Minimum and maximum values are not guaranteed; based on characterization data.*
2. *Typical specifications are not guaranteed; typical values at +25°C.*
3. *Guaranteed by design.*
4. *Min/Max values for DVoff are across temperature (-40°C to 85°C) and after MSL3 preconditioning. Based on characterization data. Not guaranteed and not tested in production.*

2.2 Electrical characteristics

@Vdd = 3.0 V, T = +25°C, unless otherwise noted. The product is factory calibrated at 3.0 V.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.(1)	Typ.(2)	Max.(1)	Unit
Vdd	Supply voltage		2.4	3.0	3.6	V
Vdd_IO	I/O pins supply voltage(3)		1.71		Vdd+0.1	V
Idd	Supply current			6.1		mA
IddSL	Supply current in sleep mode(4)	Selectable by digital interface		1.5		mA
IddPdn	Supply current in power-down mode(5)	Selectable by digital interface		5		µA
Top	Operating temperature range		-40		+85	°C

1. *Minimum and maximum values are not guaranteed, based on characterization data.*
2. *Typical specifications are not guaranteed; typical values at +25°C.*
3. *It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses, in this condition the measurement chain is powered off.*
4. *Sleep mode introduces a faster turn-on time compared to power-down mode.*
5. *Verified at wafer level*

2.3 Temperature sensor characteristics

@Vdd = 3.0 V, T = 25°C, unless otherwise noted. The product is factory calibrated at 3.0 V.

Table 5. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
TSDr	Temperature sensor output change vs. temperature			-1		°C/digit
TODR	Temperature refresh rate			1		Hz
Top	Operating temperature range		-40		+85	°C

1. *Typical specifications are not guaranteed; typical values at +25°C.*

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

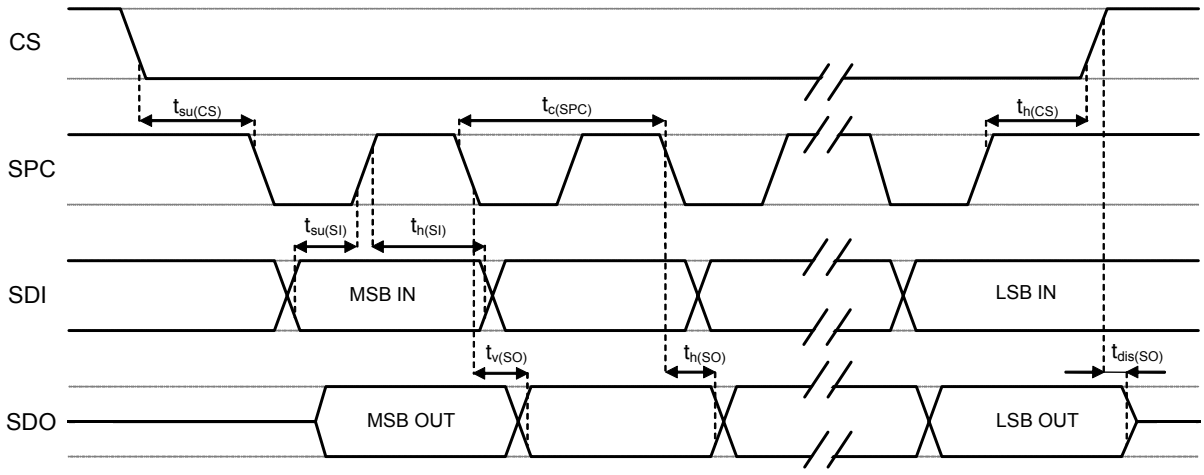
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min.	Max.	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$ts_{u(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	6		
$t_{dis(SO)}$	SDO output disable time		50	

1. *Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.*

Figure 4. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO for both input and output ports.

2.4.2 I²C - inter IC control interface

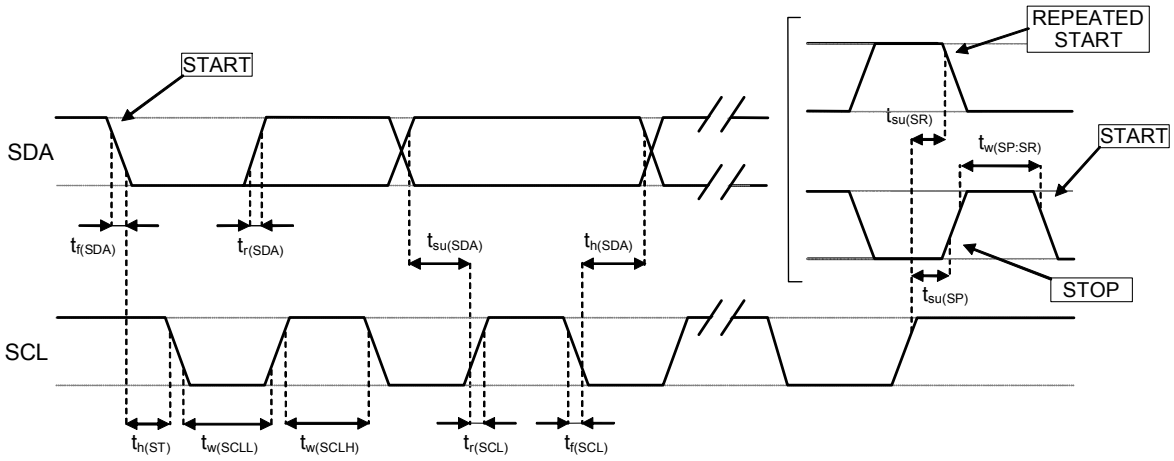
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode(1)		I²C fast mode(1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. *Data based on standard I²C protocol requirement, not tested in production.*

Figure 5. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO for both ports.

2.5 Absolute maximum ratings

Any stress above that listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to +4.8	V
T_{STG}	Storage temperature range	-40 to +125	°C
Sg	Acceleration *g* for 0.1 ms	10000	*g*
ESD	Electrostatic discharge protection	2 (HBM)	kV



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

2.6 Terminology

2.6.1 Sensitivity

An angular rate gyroscope is a device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

2.6.2 Zero-rate level

The zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and, therefore, the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

2.6.3 Stability over temperature and time

Thanks to the unique single-driving mass approach and optimized design, ST gyroscopes are able to guarantee a perfect match of the MEMS mechanical mass and the ASIC interface, and deliver unprecedented levels of stability over temperature and time.

With the zero-rate level and sensitivity performance, up to ten times better than equivalent products currently available on the market, the I3G4250D allows the user to avoid any further compensation and calibration during production for a faster time-to-market, easy implementation in applications, higher performance, and cost saving.

2.7 Soldering information

The LGA package is compliant with the ECOPACK and RoHS standard.

It is qualified for soldering heat resistance according to JEDEC J-STD-020.

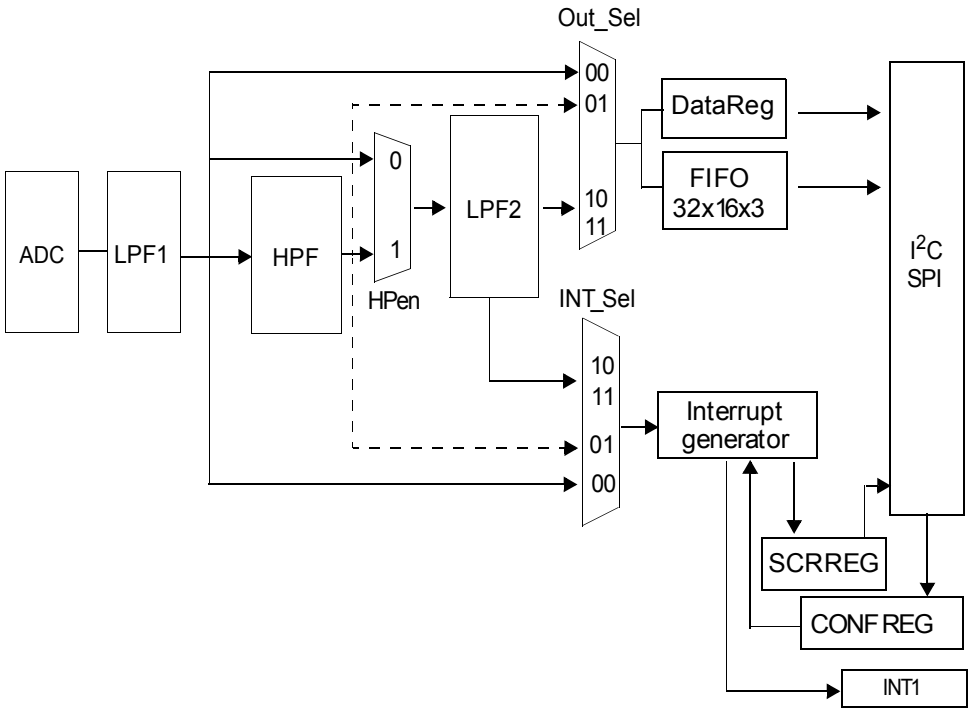
Leave “pin 1 indicator” unconnected during soldering.

For land pattern and soldering recommendations, consult technical note TN0018 available on www.st.com.

3 Main digital blocks

3.1 Block diagram

Figure 6. **Block diagram**



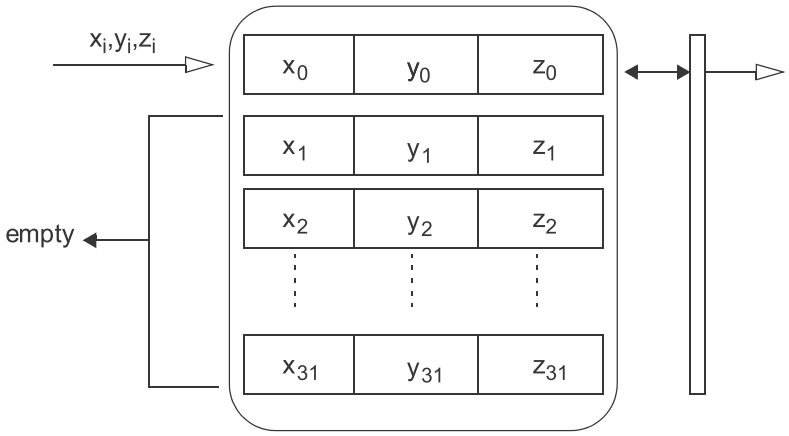
3.2 FIFO

The I3G4250D embeds a 32-slot, 16-bit data FIFO for each of the three output channels: yaw, pitch, and roll. This allows consistent power saving for the system, as the host processor does not need to continuously poll data from the sensor. Instead, it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work in three different modes. Each mode is selected by the FIFO_MODE bits in FIFO_CTRL_REG (2Eh). Programmable watermark level, FIFO_empty or FIFO_Full events can be enabled to generate dedicated interrupts on the DRDY/INT2 pin (configured through CTRL_REG3 (22h), and event detection information is available in FIFO_SRC_REG (2Fh). The watermark level can be configured using the WTM4:0 bits in FIFO_CTRL_REG (2Eh).

3.2.1 Bypass mode

In bypass mode, the FIFO is not operational and for this reason it remains empty. As illustrated in the following figure, only the first address is used for each channel. The remaining FIFO slots are empty. When new data is available, the old data is overwritten.

Figure 7. Bypass mode

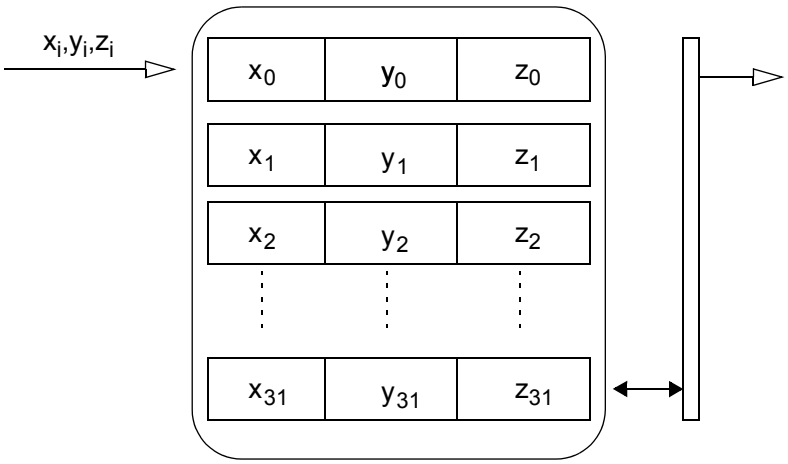


3.2.2 FIFO mode

In FIFO mode, data from the yaw, pitch, and roll channels are stored in the FIFO. A watermark interrupt can be enabled (I2_WMK bit in CTRL_REG3 (22h)), which is triggered when the FIFO is filled to the level specified by the WTM4:0 bits of FIFO_CTRL_REG (2Eh). The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch, and roll). When full, the FIFO stops collecting data from the input channels. To restart data collection, it is necessary to write FIFO_CTRL_REG (2Eh) back to bypass mode.

FIFO mode is represented in the following figure.

Figure 8. FIFO mode

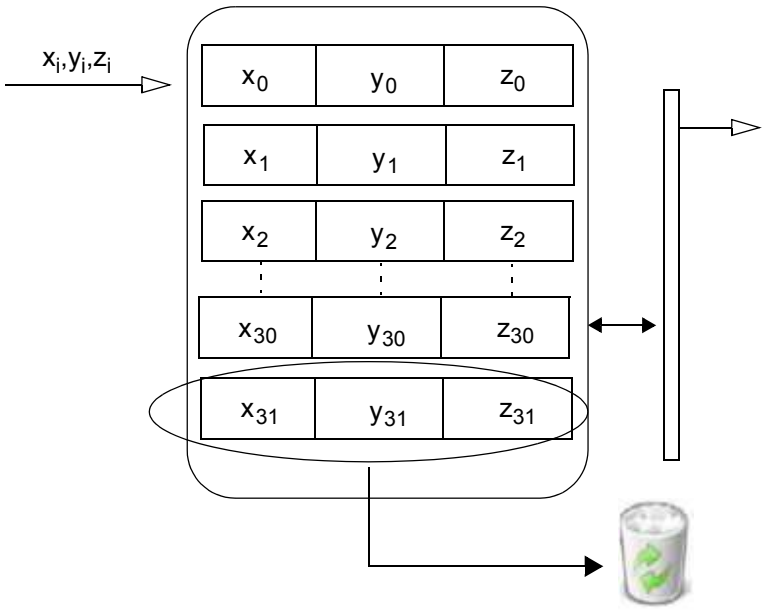


3.2.3 Stream mode

In stream mode, data from yaw, pitch, and roll measurements are stored in the FIFO. A watermark interrupt can be enabled and set as in FIFO mode. The FIFO continues filling until full (32 slots of 16-bit data for yaw, pitch, and roll). When full, the FIFO discards the older data as the new data arrives. Programmable watermark level events can be enabled to generate dedicated interrupts on the DRDY/INT2 pin (configured through CTRL_REG3 (22h)).

Stream mode is represented in the following figure.

Figure 9. Stream mode



3.2.4 Retrieving data from FIFO

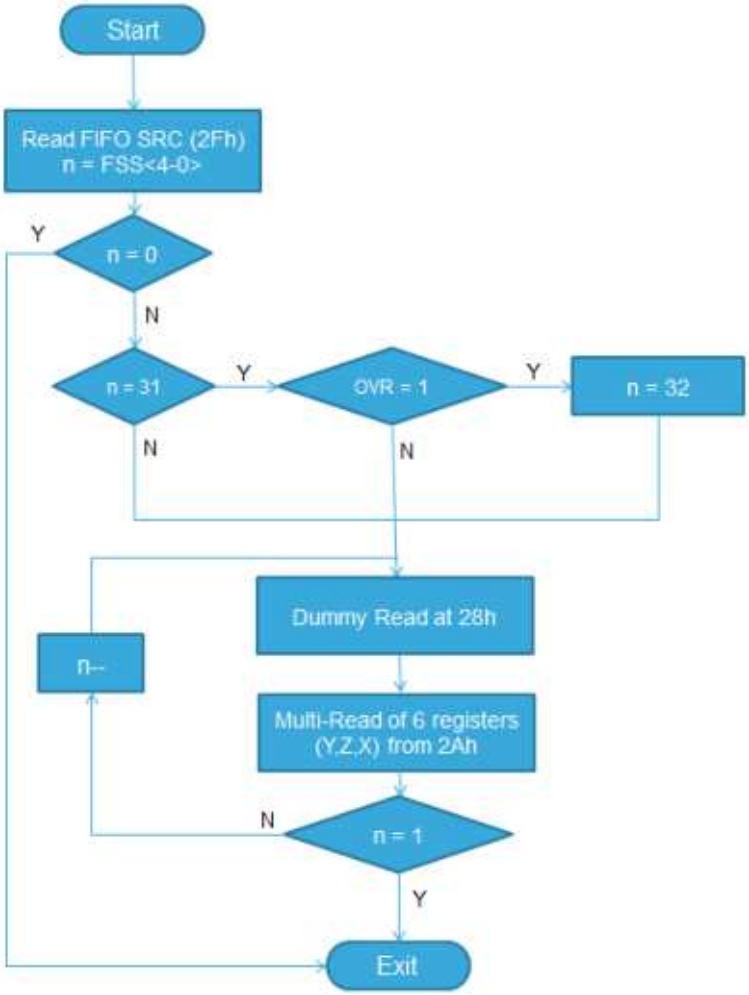
FIFO data is read from the OUT_X, OUT_Y, and OUT_Z registers. When the FIFO is in stream, bypass or FIFO mode, a read operation to the OUT_X, OUT_Y or OUT_Z registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest pitch, roll, and yaw data are placed in the OUT_X, OUT_Y and OUT_Z registers, and both single read and read-burst (X, Y & Z with auto-incremental address) operations can be used. In read-burst mode, when data included in OUT_Z_H is read, the system again starts to read information from OUT_X_L.

The read from FIFO may be executed either in synchronous or asynchronous mode. For correct data acquisition, the following steps must be respected:

1. If reading is synchronous, all data should be acquired within one ODR cycle
2. If reading is asynchronous, an appropriate FIFO access sequence must be applied:
   a. Single read from register 28h
   b. Multiread: sequentially reading 2Ah, 2Bh, 2Ch, 2Dh, 28h, 29h
   c. This procedure must be repeated for each dataset (X/Y/Z) in the FIFO:
      -FSS times, if FSS ≤ 31
      -(FSS + 1) times, if (FSS = 31) & (OVR = 1)

The following figure illustrates the correct sequence with a flow diagram.

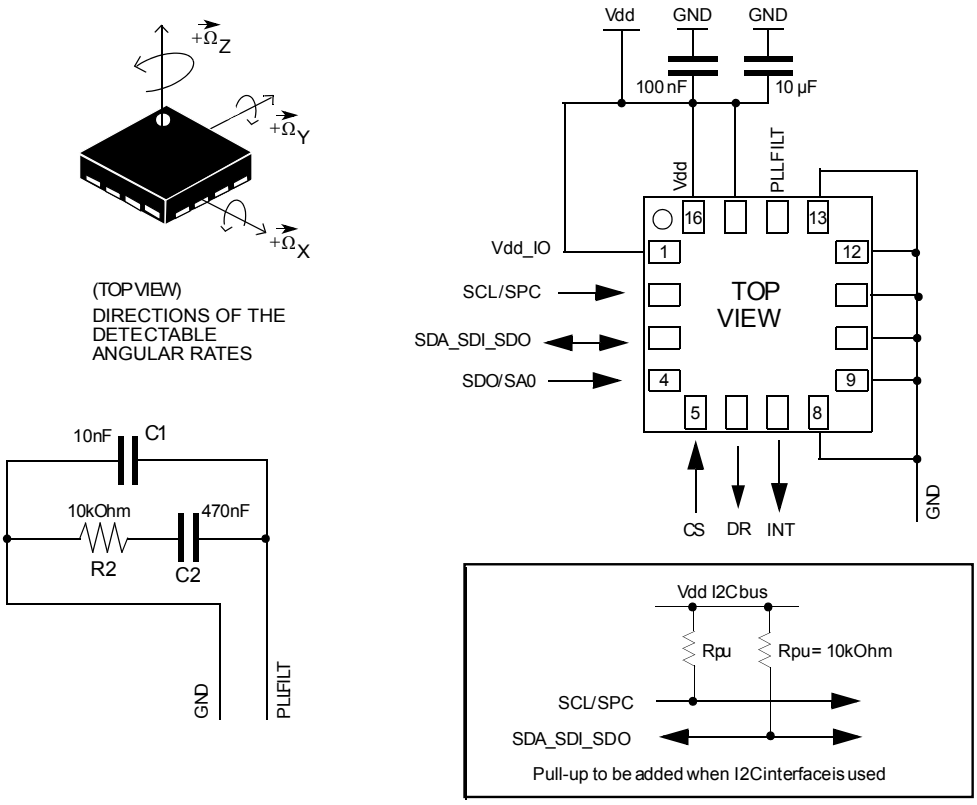
Figure 10. FIFO access sequence in asynchronous mode



If the above sequence is not followed, the acquisition from FIFO may lead to corrupted data.

4 Application hints

Figure 11. **I3G4250D electrical connections and external component values**



Power supply decoupling capacitors (100 nF ceramic or polyester +10 µF) should be placed as near as possible to the device (common design practice).

If Vdd and Vdd_IO are not connected together, power supply decoupling capacitors (100 nF and 10 µF between Vdd and common ground, 100 nF between Vdd_IO and common ground) should be placed as near as possible to the device (common design practice).

The I3G4250D IC includes a PLL (phase-locked loop) circuit to synchronize driving and sensing interfaces. Capacitors and resistors must be connected to the PLLFILT pin (as shown in Figure 11) to implement a second-order low-pass filter. The following table summarizes the PLL low-pass filter component values.

Table 9. **PLL low-pass filter component values**

Component	Value
C1	10 nF ± 10%
C2	470 nF ± 10%
R2	10 kΩ ± 10%

5 Digital interfaces

The registers embedded in the I3G4250D may be accessed through both the I²C and SPI serial interfaces. The latter may be software-configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped to the same pins. To select/exploit the I²C interface, the CS line must be tied high (that is, connected to Vdd_IO).

Table 10. Serial interface pin description

Pin name	Pin description
CS	Enable SPI I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)
SCL/SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI/SDO	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO	SPI serial data output (SDO) I²C least significant bit of the device address

5.1 I²C serial interface

The I3G4250D I²C is a bus slave. The I²C is employed to write data to registers whose content can also be read back.

The relevant I²C terminology is given in the table below.

Table 11. I²C terminology

Term	Description
Transmitter	The device that sends data to the bus
Receiver	The device that receives data from the bus
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free both the lines are high.

The I²C interface supports fast mode (400 kHz) I²C standards as well as normal mode.

5.1.1 I²C operation

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a high to low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first 7 bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated with the I3G4250D is 110100xb. The SDO pin can be used to modify the least significant bit (LSb) of the device address. If the SDO pin is connected to the voltage supply, LSb is 1 (address 1101001b). Otherwise, when the SDO pin is connected to ground, the LSb value is 0 (address 1101000b). This solution permits the connection and addressing of two different gyroscopes to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver that has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded in the I3G4250D behaves like a slave device, and the following protocol must be adhered to. After the start (ST) condition, a slave address is sent. Once a slave acknowledge (SAK) has been returned, an 8-bit subaddress is transmitted. The 7 LSb represent the actual register address while the MSb enables address auto-increment. If the MSb of the SUB field is 1, the SUB (register address) is automatically incremented to allow multiple data read/write.

The slave address is completed with a read/write bit. If the bit is 1 (read), a repeated start (SR) condition must be issued after the two subaddress bytes; if the bit is 0 (write) the master transmits to the slave with the direction unchanged. The following table describes how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 12. SAD+read/write patterns

Command	SAD[6:1]	SAD[0]= SA0	R/W	SAD+R/W
Read	110100	0	1	11010001 (D1h)
Write	110100	0	0	11010000 (D0h)
Read	110100	1	1	11010011 (D3h)
Write	110100	1	0	11010010 (D2h)

Table 13. Transfer when master is writing one byte to slave

Master	ST	SAD+ W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 14. Transfer when master is writing multiple bytes to slave

Master	ST	SAD+ W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 15. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD+ W		SUB		SR	SAD+ R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 16. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+ W		SUB		SR	SAD+ R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (that is, it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low to high transition on the SDA line while the SCL line is high is defined as a stop condition. Each data transfer must be terminated by the generation of a stop (SP) condition.

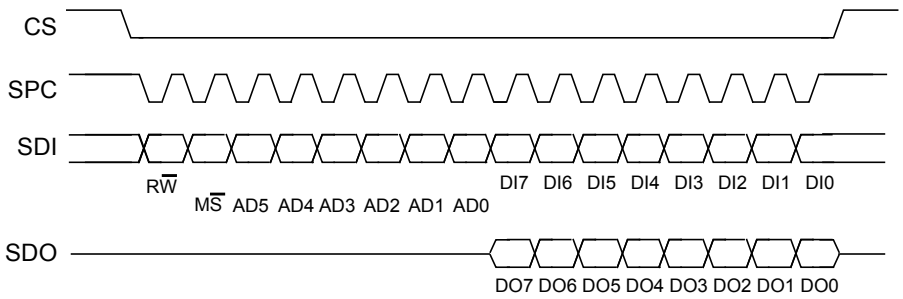
In order to read multiple bytes, it is necessary to assert the most significant bit of the subaddress field. In other words, SUB(7) must be equal to 1, while SUB(6-0) represents the address of the first register to be read.

In the presented communication format, MAK is “master acknowledge” and NMAK is “no master acknowledge”.

5.2 SPI bus interface

The SPI is a bus slave. The SPI allows writing to and reading from the device registers. The serial interface interacts with the application using four wires: **CS, SPC, SDI, and SDO**.

Figure 12. Read and write protocol



CS enables the serial port and is controlled by the SPI master. It goes low at the start of the transmission and returns to high at the end. **SPC** is the serial port clock and is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. These lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses, or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, and so forth) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

Bit 0: $R\overline{W}$ bit. When 0, the data DI(7:0) is written to the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

Bit 1: $M\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address is auto-incremented in multiple read/write commands.

Bit 2-7: address AD(5:0). This is the address field of the indexed register.

Bit 8-15: data DI(7:0) (write mode). This is the data that is written to the device (MSb first).

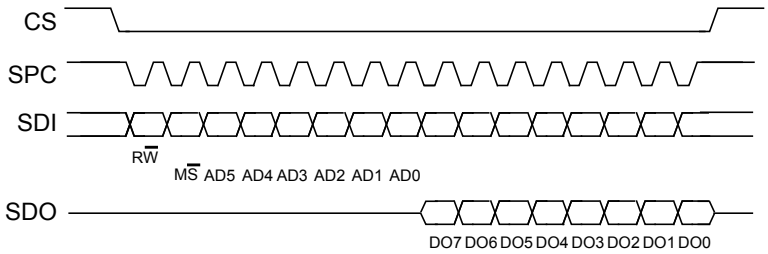
Bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods are added. When the MS bit is 0, the address used to read/write data remains the same for every block. When the MS bit is 1, the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.2.1 SPI read

Figure 13. **SPI read protocol**



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

Bit 0: READ bit. The value is 1.

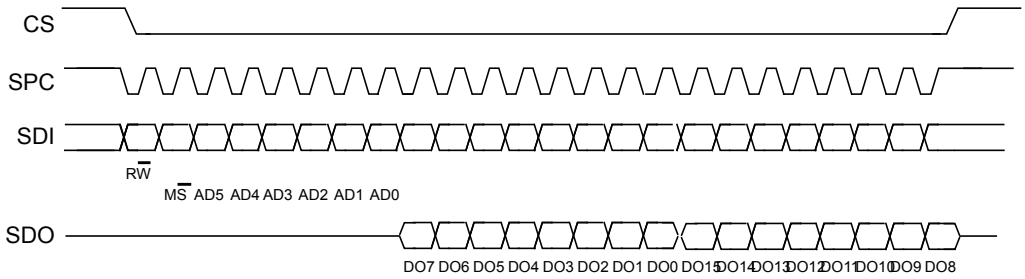
Bit 1: MS bit. When 0, does not increment address; when 1, increments address in multiple reads.

Bit 2-7: address AD(5:0). This is the address field of the indexed register.

Bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

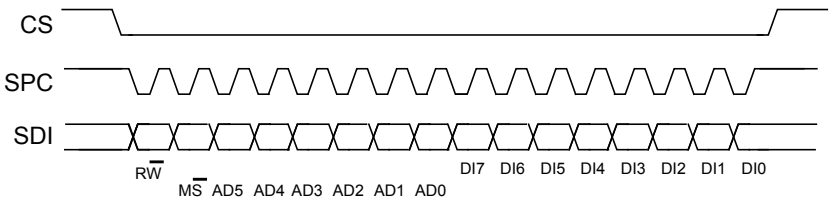
Bit 16-...: data DO(...-8). Further data in multiple byte reads.

Figure 14. **Multiple byte SPI read protocol (2-byte example)**



5.2.2 SPI write

Figure 15. **SPI write protocol**



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

Bit 0: WRITE bit. The value is 0.

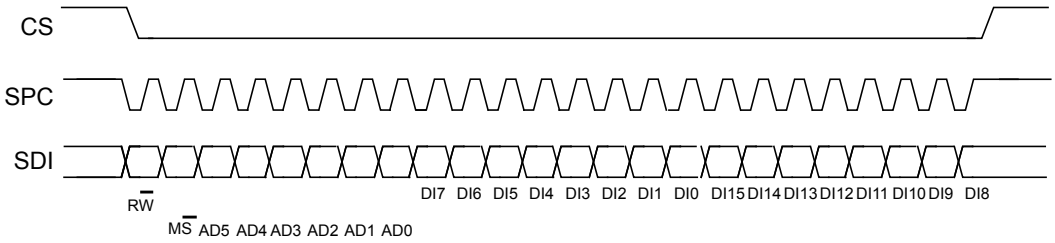
Bit 1: MS bit. When 0, does not increment address; when 1, increments address in multiple writes.

Bit 2-7: address AD(5:0). This is the address field of the indexed register.

Bit 8-15: data DI(7:0) (write mode). This is the data that is written to the device (MSb first).

Bit 16-...: data DI(...-8). Further data in multiple byte writes.

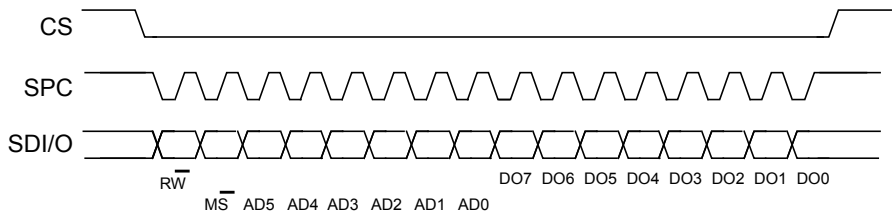
Figure 16. **Multiple byte SPI write protocol (2-byte example)**



5.2.3 SPI read in 3-wire mode

Enter 3-wire mode by setting the SIM (SPI serial interface mode selection) bit to 1 in CTRL_REG2 (21h).

Figure 17. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

Bit 0: READ bit. The value is 1.

Bit 1: MS bit. When 0, does not increment address; when 1, increments address in multiple reads.

Bit 2-7: address AD(5:0). This is the address field of the indexed register.

Bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

Note: *If the I3G4250D is used in a multi-SPI slave environment (several devices sharing the same SPI bus), the gyroscope can be forced by software to remain in SPI mode. This objective can be achieved by sending, at the beginning of the SPI communication, the following sequence to the device:*

a = read(0x05)

write(0x05, (0x20 OR a))

The programming of this register makes it possible to enhance the robustness of the SPI.

6 Output register mapping

The following table provides a list of the 8-bit registers embedded in the device and the corresponding addresses.

Table 17. Register address map

Name	Type	Register address		Default
		Hex	Binary	
Reserved	-	00-0E	-	-
WHO_AM_I	R	0F	000 1111	11010011
Reserved	-	10-1F	-	-
CTRL_REG1	R/W	20	010 0000	00000111
CTRL_REG2	R/W	21	010 0001	00000000
CTRL_REG3	R/W	22	010 0010	00000000
CTRL_REG4	R/W	23	010 0011	00000000
CTRL_REG5	R/W	24	010 0100	00000000
REFERENCE/DATACAPTURE	R/W	25	010 0101	00000000
OUT_TEMP	R	26	010 0110	Output
STATUS_REG	R	27	010 0111	Output
OUT_X_L	R	28	010 1000	Output
OUT_X_H	R	29	010 1001	Output
OUT_Y_L	R	2A	010 1010	Output
OUT_Y_H	R	2B	010 1011	Output
OUT_Z_L	R	2C	010 1100	Output
OUT_Z_H	R	2D	010 1101	Output
FIFO_CTRL_REG	R/W	2E	010 1110	00000000
FIFO_SRC_REG	R	2F	010 1111	Output
INT1_CFG	R/W	30	011 0000	00000000
INT1_SRC	R	31	011 0001	Output
INT1_THS_XH	R/W	32	011 0010	00000000
INT1_THS_XL	R/W	33	011 0011	00000000
INT1_THS_YH	R/W	34	011 0100	00000000
INT1_THS_YL	R/W	35	011 0101	00000000
INT1_THS_ZH	R/W	36	011 0110	00000000
INT1_THS_ZL	R/W	37	011 0111	00000000
INT1_DURATION	R/W	38	011 1000	00000000

Reserved registers must not be changed. Writing to those registers may change calibration data and therefore lead to device malfunction.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve rate data. The register addresses, made up of 7 bits, are used to identify them and to write the data through the serial interface.

7.1 WHO_AM_I (0Fh)

Table 18. WHO_AM_I register

1	1	0	1	0	0	1	1

Device identification register

7.2 CTRL_REG1 (20h)

Table 19. CTRL_REG1 register

DR1	DR0	BW1	BW0	PD	Zen	Yen	Xen

Table 20. CTRL_REG1 description

DR1-DR0	Output data rate selection. Refer to Table 21.
BW1-BW0	Bandwidth selection. Refer to Table 21.
PD	Enables power-down mode. Default value: 0 (0: power-down mode, 1: normal mode or sleep mode)
Zen	Enables Z-axis. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
Yen	Enables Y-axis. Default value: 1 (0: Y-axis disabled; 1: Y-axis enabled)
Xen	Enables X-axis. Default value: 1 (0: X-axis disabled; 1: X-axis enabled)

DR[1:0] is used to set the ODR selection. **BW [1:0]** is used to set the bandwidth selection.
In the following table, all frequencies resulting from a combination of the DR / BW bits are indicated.

Table 21. DR and BW configuration

DR [1:0]	BW [1:0]	ODR [Hz]	Cutoff
00	00	100	12.5
00	01	100	25
00	10	100	25
00	11	100	25
01	00	200	12.5
01	01	200	25
01	10	200	50
01	11	200	70
10	00	400	20
10	01	400	25
10	10	400	50
10	11	400	110
11	00	800	30
11	01	800	35
11	10	800	50
11	11	800	110

A combination of **PD, Zen, Yen,** and **Xen** are used to set the device in different modes (power-down / normal / sleep mode) according to the following table.

Table 22. Configuration of power mode selection

Mode	PD	Zen	Yen	Xen
Power-down	0	-	-	-
Sleep	1	0	0	0
Normal	1	-	-	-

7.3 CTRL_REG2 (21h)

Table 23. CTRL_REG2 register

0(1)	0(1)	HPM1	HPM0	HPCF3	HPCF2	HPCF1	HPCF0

1. *Value loaded at boot. This value must not be changed.*

Table 24. CTRL_REG2 description

HPM1-HPM0	High-pass filter mode selection. Default value: 00 Refer to Table 25
HPCF3-HPCF0	High-pass filter cutoff frequency selection Refer to Table 26

Table 25. High-pass filter mode configuration

HPM1	HPM0	High-pass filter mode
0	0	Normal mode (reset by reading the REFERENCE/DATACAPTURE (25h) register)
0	1	Reference signal for filtering
1	0	Normal mode (reset by reading the REFERENCE/DATACAPTURE (25h) register)
1	1	Autoreset on interrupt event

Table 26. High-pass filter cutoff frequency configuration [Hz]

HPCF[3:0]	ODR = 100 Hz	ODR = 200 Hz	ODR = 400 Hz	ODR = 800 Hz
0000	8	15	30	56
0001	4	8	15	30
0010	2	4	8	15
0011	1	2	4	8
0100	0.5	1	2	4
0101	0.2	0.5	1	2
0110	0.1	0.2	0.5	1
0111	0.05	0.1	0.2	0.5
1000	0.02	0.05	0.1	0.2
1001	0.01	0.02	0.05	0.1

7.4 CTRL_REG3 (22h)

Table 27. **CTRL_REG3 register**

I1_Int1	I1_Boot	H_Lactive	PP_OD	I2_DRDY	I2_WTM	I2_ORun	I2_Empty

Table 28. **CTRL_REG3 description**

I1_Int1	Enables nterrupt on the INT1 pin. Default value 0. (0: disable; 1: enable)
I1_Boot	Boot status available on INT1. Default value 0. (0: disable; 1: enable)
H_Lactive	Interrupt active configuration on INT1. Default value 0. (0: high; 1: low)
PP_OD	Push-pull / open drain. Default value: 0. (0: push-pull; 1: open drain)
I2_DRDY	Date ready on DRDY/INT2. Default value 0. (0: disable; 1: enable)
I2_WTM	FIFO watermark interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)
I2_ORun	FIFO overrun interrupt on DRDY/INT2 Default value: 0. (0: disable; 1: enable)
I2_Empty	FIFO empty interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)

7.5 CTRL_REG4 (23h)

Table 29. **CTRL_REG4 register**

0	BLE	FS1	FS0	-	ST1	ST0	SIM

Table 30. **CTRL_REG4 description**

BLE	Big/little endian data selection. Default value 0. (0: data LSB @ lower address; 1: data MSB @ lower address)
FS1-FS0	Full-scale selection. Default value: 00 (00: ±245 dps; 01: ±500 dps; 10: ±2000 dps; 11: ±2000 dps)
ST1-ST0	Enables self-test. Default value: 00 (00: self-test disabled; other: see Table 31
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)

Table 31. **Self-test mode configuration**

ST1	ST0	Self-test mode
0	0	Normal mode
0	1	Self-test 0 (+)(1)
1	0	--
1	1	Self-test 1 (-)(1)

1. *DST sign (absolute value in Table 3).*

7.6 CTRL_REG5 (24h)

Table 32. **CTRL_REG5 register**

BOOT	FIFO_EN	--	HPen	INT1_Sel1	INT1_Sel0	Out_Sel1	Out_Sel0

Table 33. **CTRL_REG5 description**

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
FIFO_EN	Enable FIFO. Default value: 0 (0: FIFO disabled; 1: FIFO enabled)
HPen	Enable high-pass filter (see Figure 18). Default value: 0 (0: HPF disabled; 1: HPF enabled
INT1_Sel[1:0]	INT1 selection configuration (see Figure 18). Default value: 0
Out_Sel[1:0]	Out selection configuration (see Figure 18). Default value: 0

Figure 18. **INT1_Sel and Out_Sel configuration block diagram**

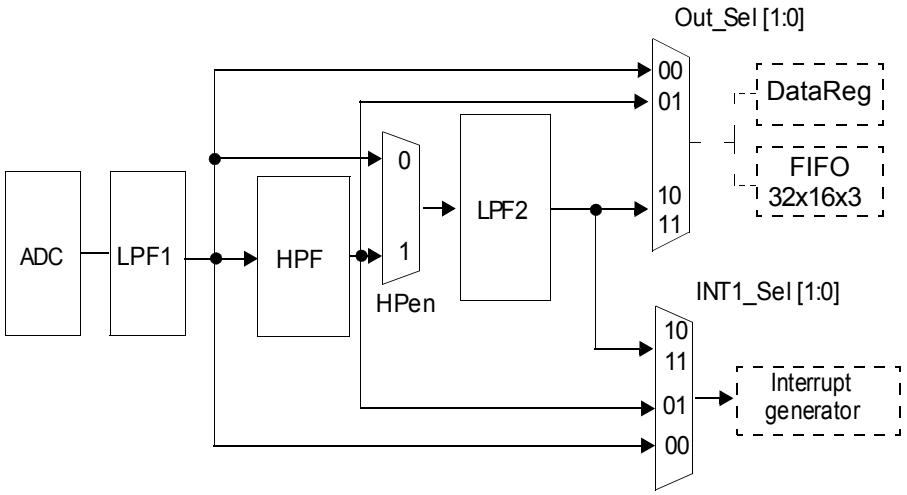


Table 34. **Out_Sel configuration settings**

HPen	Out_Sel1	Out_Sel0	Description
x	0	0	Data in DataReg and FIFO are not high-pass filtered
x	0	1	Data in DataReg and FIFO are high-pass filtered
0	1	x	Data in DataReg and FIFO are low-pass filtered by LPF2
1	1	x	Data in DataReg and FIFO are high-pass and low-pass filtered by LPF2

Table 35. **INT_SEL configuration settings**

HPen	INT_Sel1	INT_Sel2	Description
x	0	0	Non-high-pass-filtered data are used for interrupt generation
x	0	1	High-pass-filtered data are used for interrupt generation
0	1	x	Low-pass-filtered data are used for interrupt generation
1	1	x	High-pass and low-pass-filtered data are used for interrupt generation

7.7 REFERENCE/DATACAPTURE (25h)

Table 36. **REFERENCE register**

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0

Table 37. **REFERENCE register description**

Ref 7-Ref0	Reference value for interrupt generation. Default value: 0

7.8 OUT_TEMP (26h)

Table 38. **OUT_TEMP register**

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 39. **OUT_TEMP register description**

Temp7-Temp0	Temperature data

7.9 STATUS_REG (27h)

Table 40. **STATUS_REG register**

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 41. **STATUS_REG description**

ZYXOR	X-, Y-, Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data has overwritten the previous data before it was read)
ZOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the Y-axis has overwritten the previous data)
XOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the X-axis has overwritten the previous data)
ZYXDA	X, Y, Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XDA	X-axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

7.10 OUT_X_L (28h), OUT_X_H (29h)

X-axis angular rate data. The value is expressed as two's complement.

7.11 OUT_Y_L (2Ah), OUT_Y_H (2Bh)

Y-axis angular rate data. The value is expressed as two's complement.

7.12 OUT_Z_L (2Ch), OUT_Z_H (2Dh)

Z-axis angular rate data. The value is expressed as two's complement.

7.13 FIFO_CTRL_REG (2Eh)

Table 42. FIFO_CTRL_REG register

FM2	FM1	FM0	WTM4	WTM3	WTM2	WTM1	WTM0

Table 43. FIFO_CTRL_REG register description

FM2-FM0	FIFO mode selection. Default value: 000
WTM4-WTM0	FIFO threshold. Watermark level setting.

Table 44. FIFO mode configuration

FM2	FM1	FM0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode

7.14 FIFO_SRC_REG (2Fh)

Table 45. FIFO_SRC_REG register

WTM	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 46. FIFO_SRC register description

WTM	Watermark status. (0: FIFO filling is lower than WTM level; 1: FIFO filling is equal to or higher than WTM level)
OVRN	Overrun bit status. (0: FIFO is not completely filled; 1: FIFO is completely filled)
EMPTY	FIFO empty bit. (0: FIFO not empty; 1: FIFO empty)
FSS4-FSS1	FIFO stored data level

7.15 INT1_CFG (30h)

Table 47. **INT1_CFG register**

AND/OR	LIR	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 48. **INT1_CFG description**

AND/OR	AND/OR combination of interrupt events. Default value: 0 (0: OR combination of interrupt events 1: AND combination of interrupt events
LIR	Latch interrupt request. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched) Cleared by reading INT1_SRC (31h).
ZHIE	Enables interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured rate value higher than preset threshold)
ZLIE	Enables interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured rate value lower than preset threshold)
YHIE	Enables interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured rate value higher than preset threshold)
YLIE	Enables interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured rate value lower than preset threshold)
XHIE	Enables interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured rate value higher than preset threshold)
XLIE	Enables interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured rate value lower than preset threshold)

Configuration register for interrupt source

7.16 INT1_SRC (31h)

Table 49. **INT1_SRC register**

0	IA	ZH	ZL	YH	YL	XH	XL

Table 50. **INT1_SRC description**

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Interrupt source register. Read-only register.

Reading at this address clears the INT1_SRC IA bit (and eventually the interrupt signal on the INT1 pin) and allows the refresh of data in the INT1_SRC register if the latched option is chosen.

7.17 INT1_THS_XH (32h)

Table 51. **INT1_THS_XH register**

-	THSX14	THSX13	THSX12	THSX11	THSX10	THSX9	THSX8

Table 52. **INT1_THS_XH description**

THSX14 - THSX8	Interrupt threshold. Default value: 0000 0000

7.18 INT1_THS_XL (33h)

Table 53. **INT1_THS_XL register**

THSX7	THSX6	THSX5	THSX4	THSX3	THSX2	THSX1	THSX0

Table 54. **INT1_THS_XL description**

THSX7 - THSX0	Interrupt threshold. Default value: 0000 0000

7.19 INT1_THS_YH (34h)

Table 55. **INT1_THS_YH register**

-	THSY14	THSY13	THSY12	THSY11	THSY10	THSY9	THSY8

Table 56. **INT1_THS_YH description**

THSY14 - THSY8	Interrupt threshold. Default value: 0000 0000

7.20 INT1_THS_YL (35h)

Table 57. **INT1_THS_YL register**

THSY7	THSY6	THSY5	THSY4	THSY3	THSY2	THSY1	THSY0

Table 58. **INT1_THS_YL description**

THSY7 - THSY0	Interrupt threshold. Default value: 0000 0000

7.21 INT1_THS_ZH (36h)

Table 59. **INT1_THS_ZH register**

-	THSZ14	THSZ13	THSZ12	THSZ11	THSZ10	THSZ9	THSZ8

Table 60. **INT1_THS_ZH description**

THSZ14 - THSZ8	Interrupt threshold. Default value: 0000 0000

7.22 INT1_THS_ZL (37h)

Table 61. **INT1_THS_ZL register**

THSZ7	THSZ6	THSZ5	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0

Table 62. **INT1_THS_ZL description**

THSZ7 - THSZ0	Interrupt threshold. Default value: 0000 0000

7.23 INT1_DURATION (38h)

Table 63. **INT1_DURATION register**

WAIT	D6	D5	D4	D3	D2	D1	D0

Table 64. **INT1_DURATION description**

WAIT	Enables WAIT bit. Default value: 0 (0: disable; 1: enable)
D6-D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

The **WAIT** bit has the following meaning:

Wait = 0: the interrupt falls immediately if the signal crosses the selected threshold.

Wait = 1: if the signal crosses the selected threshold, the interrupt falls only after the duration has counted a number of samples at the selected data rate, written into the duration counter register.

Figure 19. **Wait disabled**

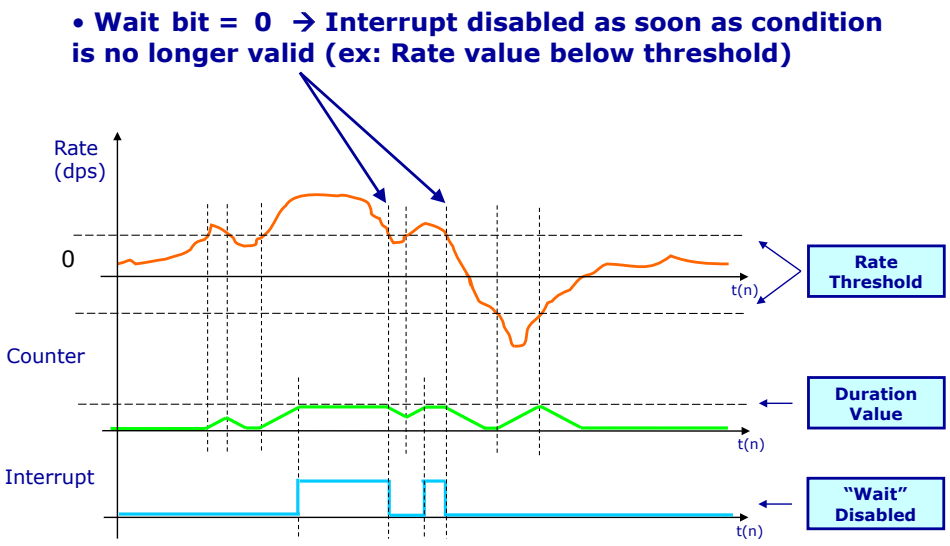
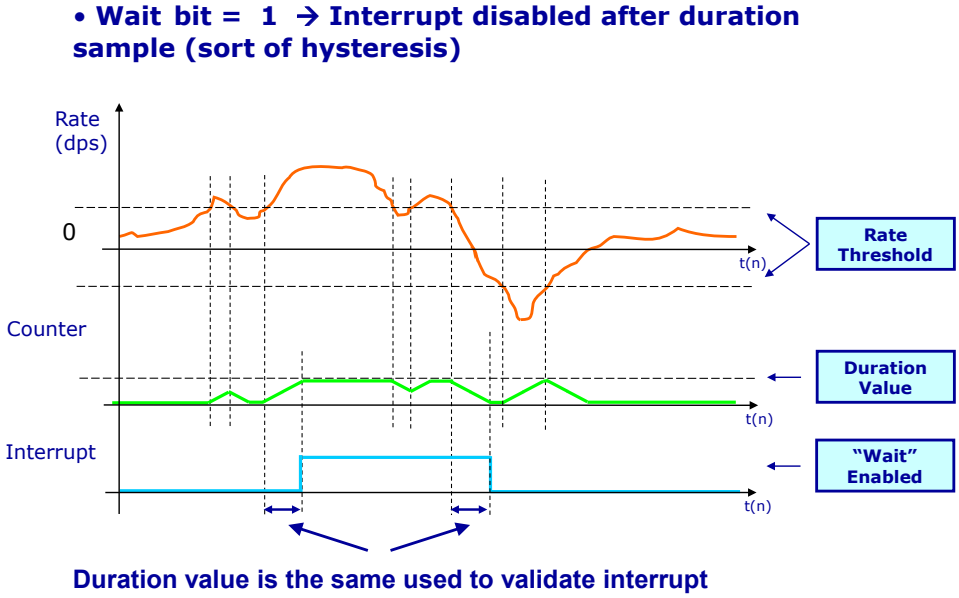


Figure 20. Wait enabled



8 Package information

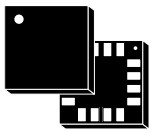
To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 LGA-16L package information

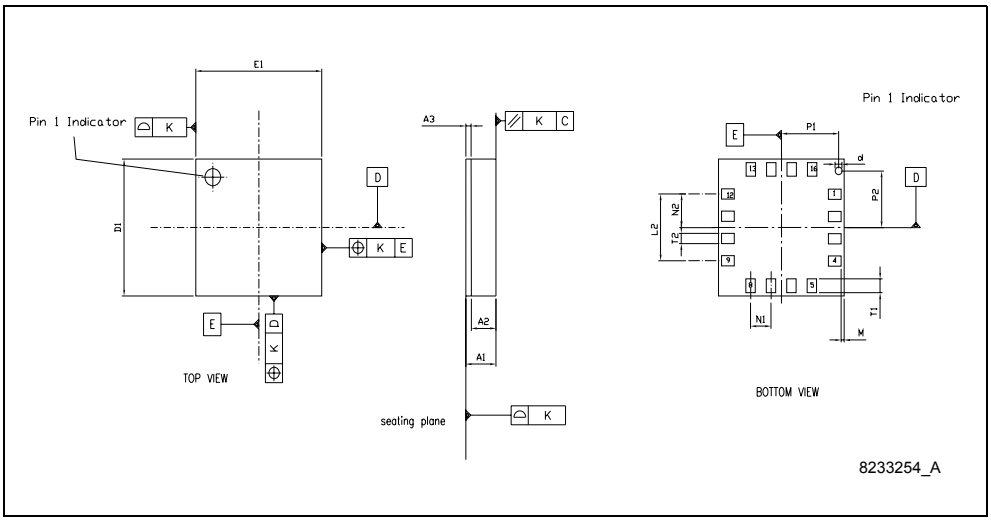
Figure 21. LGA-14L 4 x 4 x 1.1 mm package outline and mechanical data

Dimensions			
Ref.	mm		
	Min.	Typ.	Max.
A1			1.100
A2		0.855	
A3		0.200	
d		0.300	
D1	3.850	4.000	4.150
E1	3.850	4.000	4.150
L2		1.950	
M		0.100	
N1		0.650	
N2		0.975	
P1		1.750	
P2		1.525	
T1		0.400	
T2		0.300	
k		0.050	

Outline and mechanical data



LGA-16 (4x4x1.1 mm ^{3})
Land Grid Array Package



Revision history

Table 65. **Document revision history**

Date	Version	Changes
20-Apr-2015	1	Initial release
21-Apr-2015	2	First public release
15-Oct-2024	3	Updated product summary table Added 10-year longevity product label

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