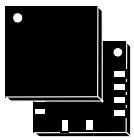
# IIS2DH

## Ultra-low-power high-performance 3-axis accelerometer with digital output for industrial applications

**Datasheet - production data**



**LGA-12 (2.0x2.0x1 mm)**

## Features

- Wide supply voltage, 1.71 V to 3.6 V
- Independent IOs supply (1.8 V) and supply voltage compatible
- Ultra-low power consumption down to 2 µA
- ±2*g*/±4*g*/±8*g*/±16*g* selectable full scales
- $I^2C$/SPI digital output interface
- 3 operating modes: low-power, normal, high-resolution mode
- 2 independent programmable interrupt generators for free-fall and motion detection
- 6D/4D orientation detection
- Motion detection & free-fall detection
- “Sleep-to-wake” and “return-to-sleep” functions
- Embedded FIFO
- Embedded self-test
- Embedded temperature sensor
- ECOPACK®, RoHS and “Green” compliant

## Applications

- Robotics
- Anti-tampering devices
- Vibration monitoring
- Tilt/inclination measurements
- Impact recognition and logging
- Industrial tools and factory equipment
- Motion-activated functions

## Description

The IIS2DH is an ultra-low-power high-performance three-axis linear accelerometer with digital $I^2C$/SPI serial interface standard output.

The IIS2DH has user-selectable full scales of ±2*g*/±4*g*/±8*g*/±16*g* and is capable of measuring accelerations with output data rates from 1 Hz to 5.3 kHz.

The device may be configured to generate interrupt signals by two independent inertial wake-up/free-fall events as well as by the position of the device itself.

The self-test capability allows the user to check the functionality of the sensor in the final application.

The IIS2DH is available in a small thin plastic land grid array package (LGA) and is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

**Table 1. Device summary**

| Order code | Temperature range [°C] | Package | Packaging |
|---|---|---|---|
| IIS2DHTR | -40 to +85 | LGA-12 | Tape and reel |



This is information on a product in full production. www.st.com

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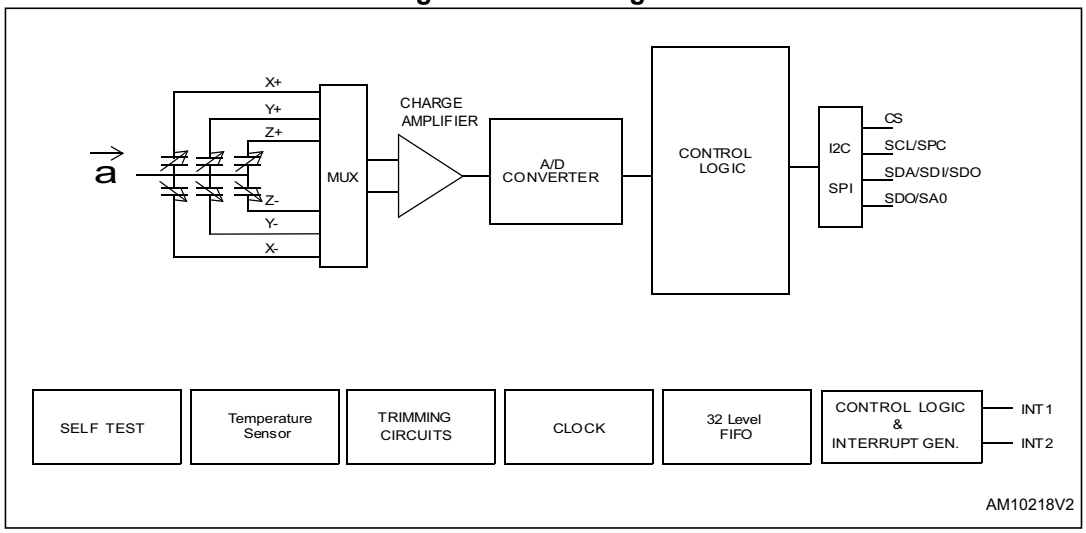
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# 1 Block diagram and pin description

## 1.1 Block diagram

**Figure 1. Block diagram**




## 1.2 Pin description

**Figure 2. Pin connections**

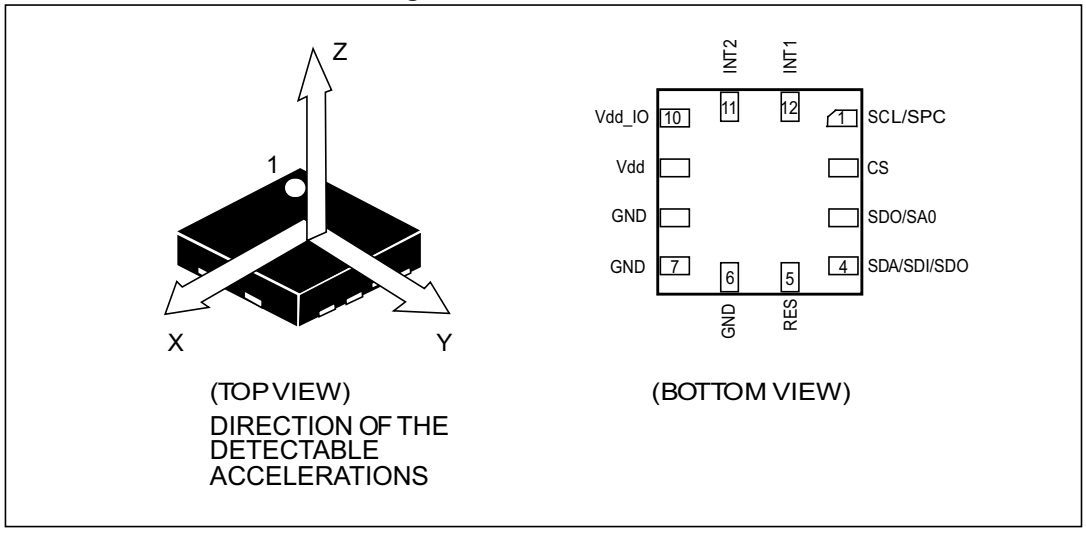


**Table 2. Pin description**

| Pin# | Name | Function |
|---|---|---|
| 1 | SCL<br>SPC | $I^2C$ serial clock (SCL)<br>SPI serial port clock (SPC) |
| 2 | CS | SPI enable<br>$I^2C$/SPI mode selection:<br>1: SPI idle mode / $I^2C$ communication enabled<br>0: SPI communication mode / $I^2C$ disabled |
| 3 | SDO<br>SA0 | SPI serial data output (SDO)<br>$I^2C$ less significant bit of the device address (SA0) |
| 4 | SDA<br>SDI<br>SDO | $I^2C$ serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) |
| 5 | Res | Connect to GND |
| 6 | GND | 0 V supply |
| 7 | GND | 0 V supply |
| 8 | GND | 0 V supply |
| 9 | Vdd | Power supply |
| 10 | Vdd_IO | Power supply for I/O pins |
| 11 | INT2 | Interrupt pin 2 |
| 12 | INT1 | Interrupt pin 1 |

# 2 Mechanical and electrical specifications

## 2.1 Mechanical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted[a]

**Table 3. Mechanical characteristics**

| Symbol | Parameter | Test conditions | Min.[1] | Typ.[2] | Max.[1] | Unit |
|---|---|---|---|---|---|---|
| FS | Measurement range[3] | FS bits set to 00 | | ±2.0 | | *g* |
| | | FS bits set to 01 | | ±4.0 | | |
| | | FS bits set to 10 | | ±8.0 | | |
| | | FS bits set to 11 | | ±16.0 | | |
| So | Sensitivity | FS bits set to 00; Normal mode | 3.52 | 3.91 | 4.30 | mg/digit |
| | | FS bits set to 00; High-resolution mode | 0.88 | 0.98 | 1.07 | |
| | | FS bits set to 00; Low-power mode | 14.06 | 15.63 | 17.19 | |
| | | FS bits set to 01; Normal mode | 7.03 | 7.81 | 8.59 | mg/digit |
| | | FS bits set to 01; High-resolution mode | 1.76 | 1.95 | 2.15 | |
| | | FS bits set to 01; Low-power mode | 28.13 | 31.25 | 34.38 | |
| | | FS bits set to 10; Normal mode | 14.06 | 15.63 | 17.19 | mg/digit |
| | | FS bits set to 10; High-resolution mode | 3.52 | 3.91 | 4.30 | |
| | | FS bits set to 10; Low-power mode | 56.25 | 62.50 | 68.75 | |
| | | FS bits set to 11; Normal mode | 42.25 | 46.95 | 51.64 | mg/digit |
| | | FS bits set to 11; High-resolution mode | 10.55 | 11.72 | 12.90 | |
| | | FS bits set to 11; Low-power mode | 169.81 | 188.68 | 207.55 | |
| TCSo | Sensitivity change vs. temperature | FS bits set to 00 | | ±0.01 | | %/°C |
| TyOff | Typical zero-*g* level offset accuracy[4] | FS bits set to 00 | -90 | ±40 | +90 | mg |

a. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.

**Table 3. Mechanical characteristics (continued)**

| Symbol | Parameter | Test conditions | Min.(1) | Typ.(2) | Max.(1) | Unit |
|---|---|---|---|---|---|---|
| TCOff | Zero-*g* level change vs. temperature | Max delta from 25 °C | | ±0.5 | | m*g*/°C |
| Vst | Self-test output change(5) (6) (7) | FS bits set to 00<br>X-axis; Normal mode | 17 | | 360 | LSb |
| | | FS bits set to 00<br>Y-axis; Normal mode | 17 | | 360 | LSb |
| | | FS bits set to 00<br>Z-axis; Normal mode | 17 | | 360 | LSb |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. Minimum and maximum values are based on characterization data and are not guaranteed
2. Typical specifications are not guaranteed.
3. Verified by wafer level test and measurement of initial offset and sensitivity.
4. Typical zero-g level offset value after factory calibration test at socket level.
5. The sign of “Self-test output change” is defined by the ST bit in *CTRL_REG4 (23h)*, for all axes.
6. “Self-test output change” is defined as the absolute value of:
$OUTPUT[LSb]_{(Self\ test\ enabled)}$ - $OUTPUT[LSb]_{(Self\ test\ disabled)}$. 1LSb = 4 m*g* at 10-bit representation, ±2 *g* full scale
7. After enabling the ST bit, correct data is obtained after two samples (low-power mode / normal mode) or after eight samples (high-resolution mode).

## 2.2 Temperature sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted(b)

**Table 4. Temperature sensor characteristics**

| Symbol | Parameter | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|
| TSDr | Temperature sensor output change vs. temperature | | 1 | | digit/°C(2) |
| TODR | Temperature refresh rate | | ODR(3) | | Hz |
| Top | Operating temperature range | -40 | | +85 | °C |

1. Typical specifications are not guaranteed.
2. 8-bit resolution.
3. Refer to *Table 28*.

b. The product is factory calibrated at 2.5 V. Temperature sensor operation is guaranteed in the range 2 V - 3.6 V.

## 2.3 Electrical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted[c]

**Table 5. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ.[1] | Max. | Unit |
|---|---|---|---|---|---|---|
| Vdd | Supply voltage | | 1.71 | 2.5 | 3.6 | V |
| Vdd_IO | I/O pins supply voltage[2] | | 1.71 | | Vdd+0.1 | V |
| Idd | Current consumption in normal mode | 50 Hz ODR | | 11 | | µA |
| Idd | Current consumption in normal mode | 1 Hz ODR | | 2 | | µA |
| IddLP | Current consumption in low-power mode | 50 Hz ODR | | 6 | | µA |
| IddPdn | Current consumption in power-down mode | | | 0.5 | | µA |
| VIH | Digital high-level input voltage | | 0.8*Vdd_IO | | | V |
| VIL | Digital low-level input voltage | | | | 0.2*Vdd_IO | V |
| VOH | High-level output voltage | | 0.9*Vdd_IO | | | V |
| VOL | Low-level output voltage | | | | 0.1*Vdd_IO | V |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. Typical specification are not guaranteed.
2. It is possible to remove Vdd, maintaining Vdd_IO without blocking the communication busses, in this condition the measurement chain is powered off.

c. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.

## 2.4 Communication interface characteristics

### 2.4.1 SPI - serial peripheral interface

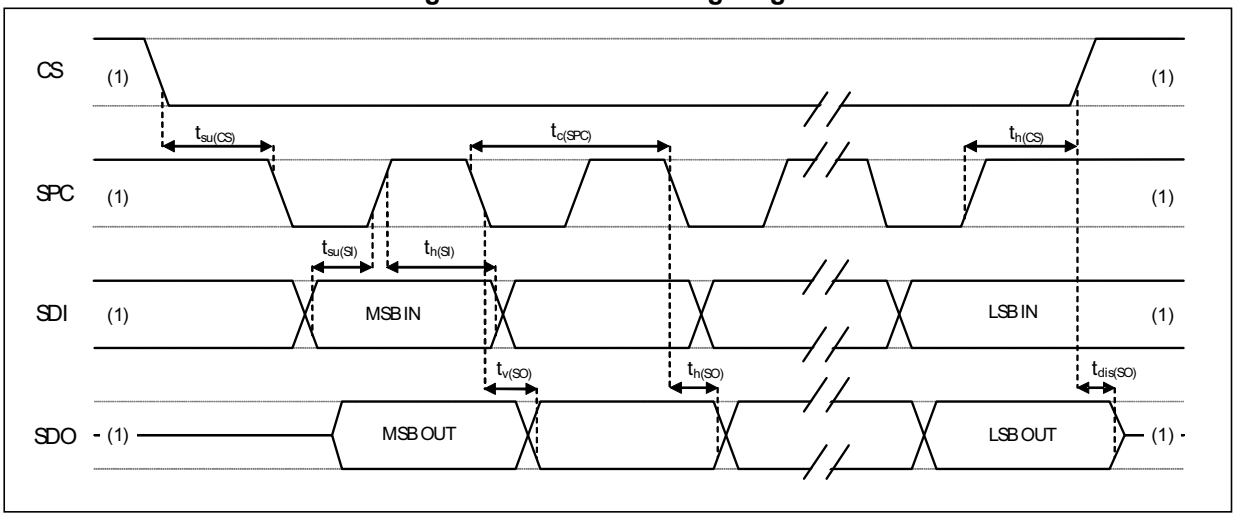
Subject to general operating conditions for Vdd and Top.

**Table 6. SPI slave timing values**

| Symbol | Parameter | Value (1) | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{c(SPC)}$ | SPI clock cycle | 100 | | ns |
| $f_{c(SPC)}$ | SPI clock frequency | | 10 | MHz |
| $t_{su(CS)}$ | CS setup time | 5 | | ns |
| $t_{h(CS)}$ | CS hold time | 20 | | |
| $t_{su(SI)}$ | SDI input setup time | 5 | | |
| $t_{h(SI)}$ | SDI input hold time | 15 | | |
| $t_{v(SO)}$ | SDO valid output time | | 50 | |
| $t_{h(SO)}$ | SDO output hold time | 5 | | |
| $t_{dis(SO)}$ | SDO output disable time | | 50 | |

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

**Figure 3. SPI slave timing diagram**




1. When no communication is ongoing, data on SDO is driven by internal pull-up resistors.

*Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.*

### 2.4.2 I²C - inter-IC control interface

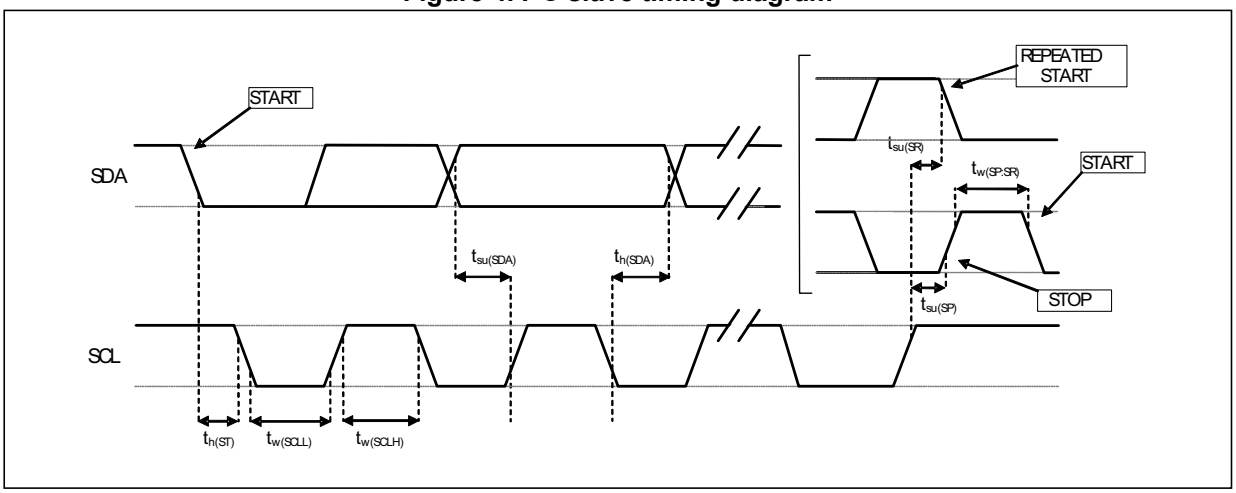
Subject to general operating conditions for Vdd and top.

**Table 7. I²C slave timing values**

| Symbol | Parameter | I²C standard mode (1) | | I²C fast mode (1) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $f_{(SCL)}$ | SCL clock frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | | 1.3 | | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | | 0.6 | | |
| $t_{su(SDA)}$ | SDA setup time | 250 | | 100 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 | 3.45 | 0 | 0.9 | µs |
| $t_{h(ST)}$ | START condition hold time | 4 | | 0.6 | | µs |
| $t_{su(SR)}$ | Repeated START condition setup time | 4.7 | | 0.6 | | |
| $t_{su(SP)}$ | STOP condition setup time | 4 | | 0.6 | | |
| $t_{w(SP:SR)}$ | Bus free time between STOP and START condition | 4.7 | | 1.3 | | |

1. Data based on standard I²C protocol requirement, not tested in production.

**Figure 4. I²C slave timing diagram**




*Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.*

## 2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 8. Absolute maximum ratings**

| Symbol | Ratings | Maximum value | Unit |
|---|---|---|---|
| Vdd | Supply voltage | -0.3 to 4.8 | V |
| Vdd_IO | Supply voltage on I/O pins | -0.3 to 4.8 | V |
| Vin | Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0) | -0.3 to Vdd_IO +0.3 | V |
| $A_{POW}$ | Acceleration (any axis, powered, Vdd = 2.5 V) | 3000 *g* for 0.5 ms | |
| | | 10000 *g* for 0.1 ms | |
| $A_{UNP}$ | Acceleration (any axis, unpowered) | 3000 *g* for 0.5 ms | |
| | | 10000 *g* for 0.1 ms | |
| $T_{OP}$ | Operating temperature range | -40 to +85 | °C |
| $T_{STG}$ | Storage temperature range | -40 to +125 | °C |
| ESD | Electrostatic discharge protection (HBM) | 2 | kV |

*Note: Supply voltage on any pin should never exceed 4.8 V*



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

## 2.6 Terminology and functionality

### Terminology

#### 2.6.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations, this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

#### 2.6.2 Zero-*g* level

The zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* for the X-axis and 0 *g* for the Y-axis whereas the Z-axis will measure 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset. Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor on a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see *Table 3* "Zero-*g* level change vs. temperature" (TCOff). The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a population of sensors.

### Functionality

#### 2.6.3 High-resolution, normal mode, low-power mode

The IIS2DH provides three different operating modes: *high-resolution mode*, *normal mode* and *low-power mode*.

The table below summarizes how to select the different operating modes.

**Table 9. Operating mode selection**

| Operating mode | CTRL_REG1[3] (LPen bit) | CTRL_REG4[3] (HR bit) | BW [Hz] | Turn-on time [ms] | So @ ±2 *g* [mg/digit] |
|---|---|---|---|---|---|
| Low-power mode (8-bit data output) | 1 | 0 | ODR/2 | 1 | 16 |
| Normal mode (10-bit data output) | 0 | 0 | ODR/2 | 1.6 | 4 |
| High-resolution mode (12-bit data output) | 0 | 1 | ODR/9 | 7/ODR | 1 |
| Not allowed | 1 | 1 | -- | -- | -- |

The turn-on time to transition to another operating mode is given in *Table 10*.

**Table 10. Turn-on time for operating mode transition**

| Operating mode change | Turn-on time [ms] |
|---|---|
| 12-bit mode to 8-bit mode | 1/ODR |
| 12-bit mode to 10-bit mode | 1/ODR |
| 10-bit mode to 8-bit mode | 1/ODR |
| 10-bit mode to 12-bit mode | 7/ODR |
| 8-bit mode to 10-bit mode | 1/ODR |
| 8-bit mode to 12-bit mode | 7/ODR |

**Table 11. Current consumption of operating modes**

| Operating mode [Hz] | Low-power mode (8-bit data output) [µA] | Normal mode (10-bit data output) [µA] | High resolution (12-bit data output) [µA] |
|---|---|---|---|
| 1 | 2 | 2 | 2 |
| 10 | 3 | 4 | 4 |
| 25 | 4 | 6 | 6 |
| 50 | 6 | 11 | 11 |
| 100 | 10 | 20 | 20 |
| 200 | 18 | 38 | 38 |
| 400 | 36 | 73 | 73 |
| 1344 | -- | 185 | 185 |
| 1620 | 100 | -- | -- |
| 5376 | 185 | -- | -- |

### 2.6.4 Self-test

The self-test allows the user to check the sensor functionality without moving it. When the self-test is enabled, an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs will exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified inside *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

### 2.6.5 6D / 4D orientation detection

The IIS2DH includes 6D / 4D orientation detection.

#### 6D / 4D orientation recognition

In this configuration the interrupt is generated when the device is stable in a known direction. In 4D configuration, detection of the position of the Z-axis is disabled.

### 2.6.6 “Sleep-to-wake” and “Return-to-sleep”

The IIS2DH can be programmed to automatically switch to low-power mode upon recognition of a determined event.
Once the event condition is over, the device returns back to the preset normal or high-resolution mode.

To enable this function the desired threshold value must be stored inside the *Act_THS (3Eh)* register while the duration value is written inside the *Act_DUR (3Fh)* register.

When the acceleration falls below the threshold value, the device automatically switches to low-power mode (10Hz ODR).
During this condition, the ODR[3:0] bits and the LPen bit inside *CTRL_REG1 (20h)* and the HR bit in *CTRL_REG3 (22h)* are not considered.

As soon as the acceleration rises above threshold, the module restores the operating mode and ODRs as determined by the *CTRL_REG1 (20h)* and *CTRL_REG3 (22h)* settings.

## 2.7 Sensing element

A proprietary process is used to create a surface micromachined accelerometer. The technology processes suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. To be compatible with traditional packaging techniques, a cap is placed on top of the sensing element to avoid blocking the moving parts during the molding phase of the plastic encapsulation.

When an acceleration is applied to the sensor, the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.

At steady state the nominal value of the capacitors are a few pF and when an acceleration is applied, the maximum variation of the capacitive load is in the fF range.

## 2.8 IC interface

The complete measurement chain is composed of a low-noise capacitive amplifier which converts the capacitive unbalance of the MEMS sensor into an analog voltage that will be available to the user through an analog-to-digital converter.

The acceleration data may be accessed through an $I^2C$/SPI interface, thus making the device particularly suitable for direct interfacing with a microcontroller.

The IIS2DH features a data-ready signal (DRDY) which indicates when a new set of measured acceleration data is available, thus simplifying data synchronization in the digital system that uses the device.

The IIS2DH may also be configured to generate an inertial wake-up and free-fall interrupt signal according to a programmed acceleration event along the enabled axes. Both free-fall and wake-up can be available simultaneously on two different pins.

## 2.9 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and zero-*g* level (TyOff).

The trim values are stored inside the device in non-volatile memory. Any time the device is turned on, these values are downloaded into the registers to be used during active operation. This allows using the device without further calibration.

## 2.10 FIFO

The IIS2DH contains a 10-bit, 32-level FIFO. Buffered output allows the following operation modes: FIFO, Stream, Stream-to-FIFO and FIFO bypass. When FIFO bypass mode is activated, FIFO is not operating and remains empty. In FIFO mode, measurement data from acceleration detection on the x, y, and z axes are stored in the FIFO buffer.

## 2.11 Temperature sensor

The IIS2DH is supplied with an internal temperature sensor. Temperature data can be enabled by setting the TEMP_EN[1:0] bits to ‘1’ in the *TEMP_CFG_REG (1Fh)* register.

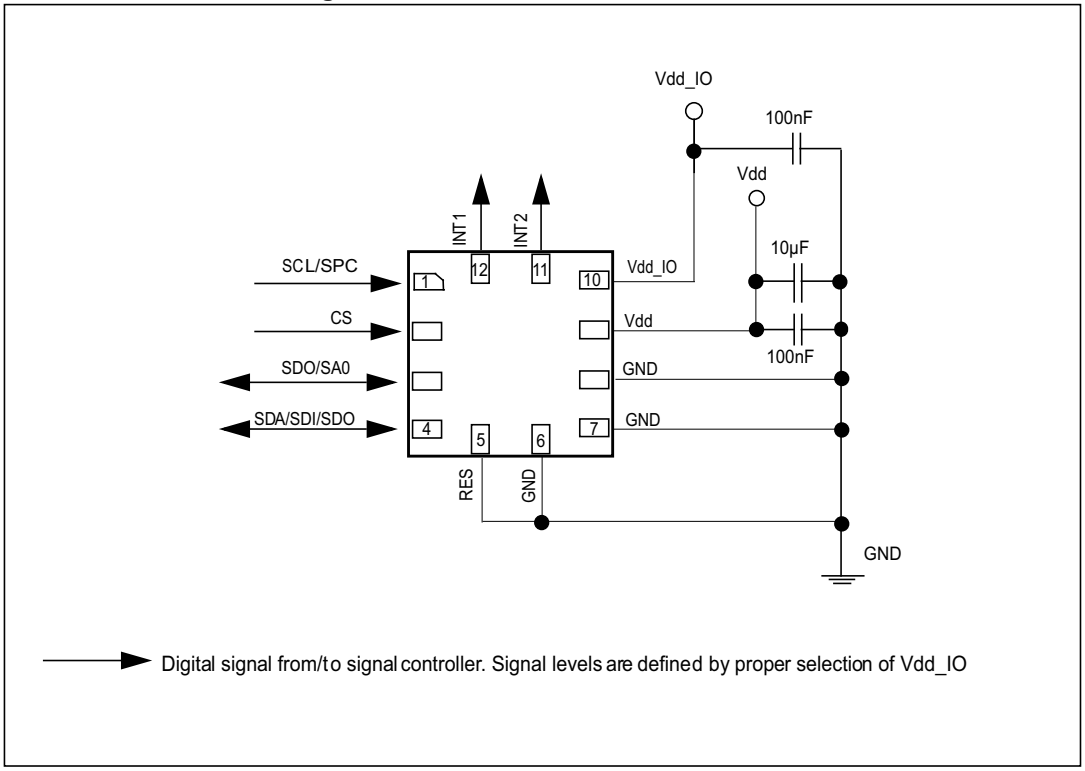
To retrieve the temperature sensor data the BDU bit in *CTRL_REG4 (23h)* must be set to ‘1’.

Both the *OUT_TEMP_L (0Ch), OUT_TEMP_H (0Dh)* registers must be read.

Temperature data is stored inside OUT_TEMP_H as two’s complement data in 8-bit format left-justified.

# 3 Application hints

**Figure 5. IIS2DH electrical connections**




The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 9 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 5*). It is possible to remove Vdd while maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data is selectable and accessible through the $I^2C$ or SPI interfaces. When using the $I^2C$, CS must be tied high.

The functions, the threshold and the timing of the two interrupt pins (INT1 and INT2) can be completely programmed by the user through the $I^2C$/SPI interface.

## 3.1 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com.

# 4 Digital main blocks

## 4.1 FIFO

The IIS2DH embeds a 32-level FIFO for each of the three output channels, X, Y and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

In order to enable the FIFO buffer, the FIFO_EN bit in *CTRL_REG5 (24h)* must be set to '1'.

This buffer can work according to the following different modes: Bypass mode, FIFO mode, Stream mode and Stream-to-FIFO mode. Each mode is selected by the FM [1:0] bits in *FIFO_CTRL_REG (2Eh)*. Programmable FIFO watermark level, FIFO empty or FIFO overrun events can be enabled to generate dedicated interrupts on the INT1 pin (configuration through *CTRL_REG3 (22h)*).

In the *FIFO_SRC_REG (2Fh)* register the EMPTY bit is equal to '1' when all FIFO samples are ready and FIFO is empty.

In the *FIFO_SRC_REG (2Fh)* register the WTM bit goes to '1' if new data is written in the buffer and *FIFO_SRC_REG (2Fh)* (FSS [4:0]) is greater than or equal to *FIFO_CTRL_REG (2Eh)* (FTH [4:0]). *FIFO_SRC_REG (2Fh)* (WTM) goes to '0' if reading an X, Y, Z data slot from FIFO and *FIFO_SRC_REG (2Fh)* (FSS [4:0]) is less than or equal to *FIFO_CTRL_REG (2Eh)* (FTH [4:0]).

In the *FIFO_SRC_REG (2Fh)* register the OVRN_FIFO bit is equal to '1' if the FIFO slot is overwritten.

### 4.1.1 Bypass mode

In Bypass mode the FIFO is not operational and for this reason it remains empty. For each channel only the first address is used. The remaining FIFO levels are empty.

Bypass mode must be used in order to reset the FIFO buffer when a different mode is operating (i.e. FIFO mode).

### 4.1.2 FIFO mode

In FIFO mode, the buffer continues filling data from the X, Y and Z accelerometer channels until it is full (a set of 32 samples stored). When the FIFO is full, it stops collecting data from the input channels and the FIFO content remains unchanged.

An overrun interrupt can be enabled, I1_OVERRUN = '1' in the *CTRL_REG3 (22h)* register, in order to be raised when the FIFO stops collecting data. When the overrun interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input channels.

After the last read it is necessary to exit Bypass mode in order to reset the FIFO content. After this reset command, it is possible to restart FIFO mode just by selecting the FIFO mode configuration (FM[1:0] bits) in register *FIFO_CTRL_REG (2Eh)*.

### 4.1.3 Stream mode

In Stream mode the FIFO continues filling data from the X, Y, and Z accelerometer channels until the buffer is full (a set of 32 samples stored) at which point the FIFO buffer index restarts from the beginning and older data is replaced by the current data. The oldest values continue to be overwritten until a read operation frees the FIFO slots.

An overrun interrupt can be enabled, I1_OVERRUN = '1' in the *CTRL_REG3 (22h)* register, in order to read the entire contents of the FIFO at once. If, in the application, it is mandatory not to lose data and it is not possible to read at least one sample for each axis within one ODR period, a watermark interrupt can be enabled in order to read partially the FIFO and leave memory slots free for incoming data.

Setting the FTH [4:0] bit in the *FIFO_CTRL_REG (2Eh)* register to an N value, the number of X, Y and Z data samples that should be read at the rise of the watermark interrupt is up to (N+1).

### 4.1.4 Stream-to-FIFO mode

In Stream-to-FIFO mode, data from the X, Y and Z accelerometer channels are collected in a combination of Stream mode and FIFO mode. The FIFO buffer starts operating in Stream mode and switches to FIFO mode when the selected interrupt occurs.

The FIFO operating mode changes according to the INT1 pin value if the TR bit is set to ‘0’ in the *FIFO_CTRL_REG (2Eh)* register or the INT2 pin value if the TR bit is set to‘1’ in the *FIFO_CTRL_REG (2Eh)* register.

When the interrupt pin is selected and the interrupt event is configured on the corresponding pin, the FIFO operates in Stream mode if the pin value is equal to ‘0’ and it operates in FIFO mode if the pin value is equal to ‘1’. Switching modes is dynamically performed according to the pin value.

Stream-to-FIFO can be used in order to analyze the sampling history that generates an interrupt. The standard operation is to read the contents of FIFO when the FIFO mode is triggered and the FIFO buffer is full and stopped.

### 4.1.5 Retrieving data from FIFO

FIFO data is read from *OUT_X_L (28h), OUT_X_H (29h)*, *OUT_Y_L (2Ah), OUT_Y_H (2Bh)* and *OUT_Z_L (2Ch), OUT_Z_H (2Dh)*. When the FIFO is in Stream, Stream-to-FIFO or FIFO mode, a read operation to the *OUT_X_L (28h), OUT_X_H (29h)*, *OUT_Y_L (2Ah), OUT_Y_H (2Bh)* or *OUT_Z_L (2Ch), OUT_Z_H (2Dh)* registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed in the *OUT_X_L (28h), OUT_X_H (29h)*, *OUT_Y_L (2Ah), OUT_Y_H (2Bh)* and *OUT_Z_L (2Ch), OUT_Z_H (2Dh)* registers and both single read and read-burst operations can be used.

The address to be read is automatically updated by the device and it rolls back to 0x28 when register 0x2D is reached. In order to read all FIFO levels in a multiple byte read, 192 bytes (6 output registers of 32 levels) have to be read.

# 5 Digital interfaces

The registers embedded inside the IIS2DH may be accessed through both the $I^2C$ and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped to the same pads. To select/exploit the $I^2C$ interface, the CS line must be tied high (i.e. connected to Vdd_IO).

**Table 12. Serial interface pin description**

| Pin name | Pin description |
|---|---|
| CS | SPI enable<br>$I^2C$/SPI mode selection:<br>1: SPI idle mode / $I^2C$ communication enabled<br>0: SPI communication mode / $I^2C$ disabled |
| SCL<br>SPC | $I^2C$ serial clock (SCL)<br>SPI serial port clock (SPC) |
| SDA<br>SDI<br>SDO | $I^2C$ serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) |
| SA0<br>SDO | $I^2C$ less significant bit of the device address (SA0)<br>SPI serial data output (SDO) |

## 5.1 $I^2C$ serial interface

The IIS2DH $I^2C$ is a bus slave. The $I^2C$ is employed to write data into registers whose content can also be read back.

The relevant $I^2C$ terminology is given in the table below.

**Table 13. $I^2C$ terminology**

| Term | Description |
|---|---|
| Transmitter | The device which sends data to the bus |
| Receiver | The device which receives data from the bus |
| Master | The device which initiates a transfer, generates clock signals and terminates a transfer |
| Slave | The device addressed by the master |

There are two signals associated with the $I^2C$ bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving data to/from the interface. Both the lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free, both the lines are high.

The $I^2C$ interface is compliant with fast mode (400 kHz) $I^2C$ standards as well as with the normal mode.

### 5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a high-to-low transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The Slave ADdress (SAD) associated to the IIS2DH is 001100xb. The **SDO**/**SA0** pad can be used to modify the less significant bit of the device address. If the SA0 pad is connected to the voltage supply, LSb is ‘1’ (address 0011001b), else if the SA0 pad is connected to ground, the LSb value is ‘0’ (address 0011000b). This solution permits to connect and address two different accelerometers to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the IIS2DH behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represent the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is ‘1’, the SUB (register address) is automatically increased to allow multiple data read/writes.

The slave address is completed with a Read/Write bit. If the bit was ‘1’ (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is ‘0’ (Write) the master will transmit to the slave with direction unchanged. *Table 14* explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

**Table 14. SAD+read/write patterns**

| Command | SAD[6:1] | SAD[0] = SA0 | R/W | SAD+R/W |
|---|---|---|---|---|
| Read | 001100 | 0 | 1 | 00110001 (31h) |
| Write | 001100 | 0 | 0 | 00110000 (30h) |
| Read | 001100 | 1 | 1 | 00110011 (33h) |
| Write | 001100 | 1 | 0 | 00110010 (32h) |

**Table 15. Transfer when master is writing one byte to slave**

| Master | ST | SAD + W | | SUB | | DATA | | SP |
|---|---|---|---|---|---|---|---|---|
| Slave | | | SAK | | SAK | | SAK | |

**Table 16. Transfer when master is writing multiple bytes to slave**

| Master | ST | SAD + W | | SUB | | DATA | | DATA | | SP |
|---|---|---|---|---|---|---|---|---|---|---|
| Slave | | | SAK | | SAK | | SAK | | SAK | |

**Table 17. Transfer when master is receiving (reading) one byte of data from slave**

| Master | ST | SAD + W | | SUB | | SR | SAD + R | | | NMAK | SP |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Slave | | | SAK | | SAK | | | SAK | DATA | | |

**Table 18. Transfer when master is receiving (reading) multiple bytes of data from slave**

| Master | ST | SAD+W | | SUB | | SR | SAD+R | | | MAK | | MAK | | NMAK | SP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Slave | | | SAK | | SAK | | | SAK | DATA | | DATA | | DATA | | |

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A low-to-high transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

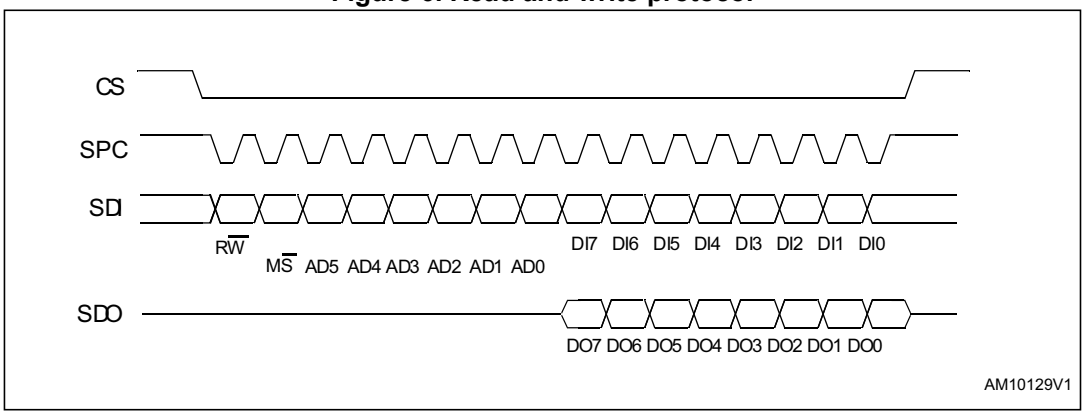
In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

## 5.2 SPI bus interface

The IIS2DH SPI is a bus slave. The SPI allows writing to and reading from the registers of the device.

The serial interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

**Figure 6. Read and write protocol**




**CS** is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. These lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

***bit 0***: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip will drive **SDO** at the start of bit 8.

***bit 1***: M$\overline{S}$ bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address is auto incremented in multiple read/write commands.

***bit 2-7***: address AD(5:0). This is the address field of the indexed register.

***bit 8-15***: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

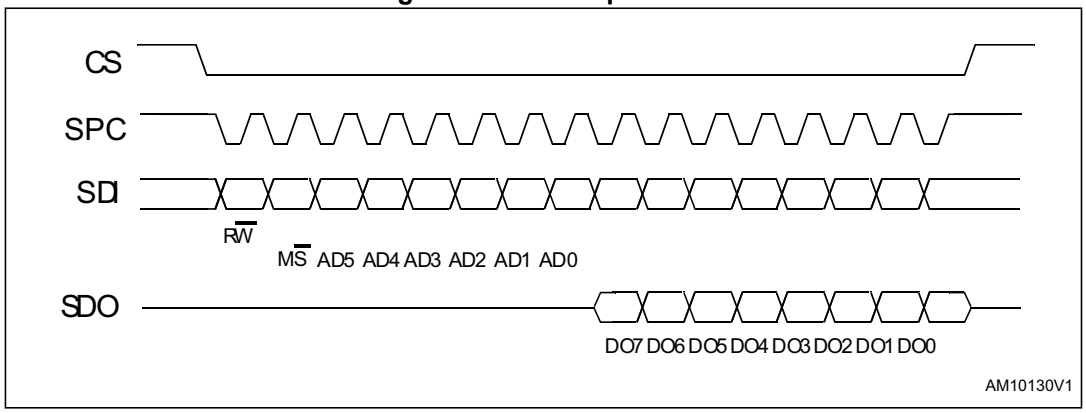
***bit 8-15***: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When the M$\overline{S}$ bit is ‘0’, the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is ‘1’, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

### 5.2.1 SPI read

**Figure 7. SPI read protocol**




The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

***bit 0***: READ bit. The value is 1.

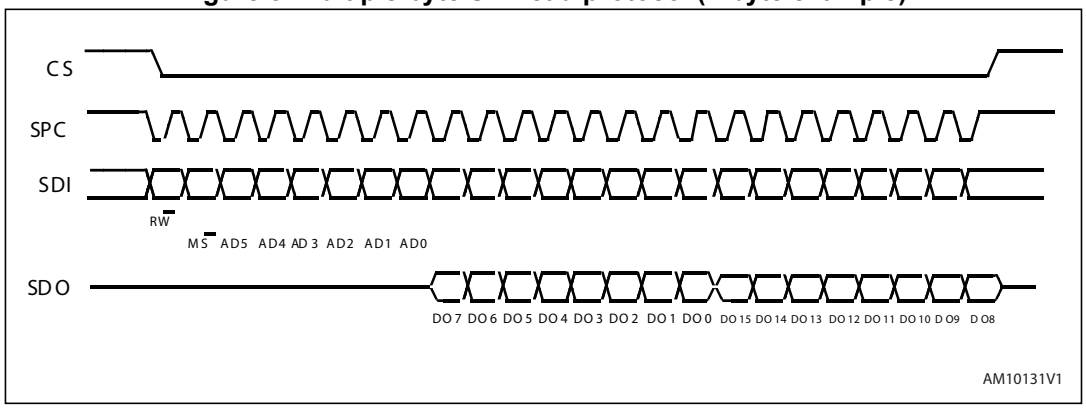
***bit 1***: MS bit. When 0, does not increment the address, when 1, increments the address in multiple reads.

***bit 2-7***: address AD(5:0). This is the address field of the indexed register.

***bit 8-15***: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

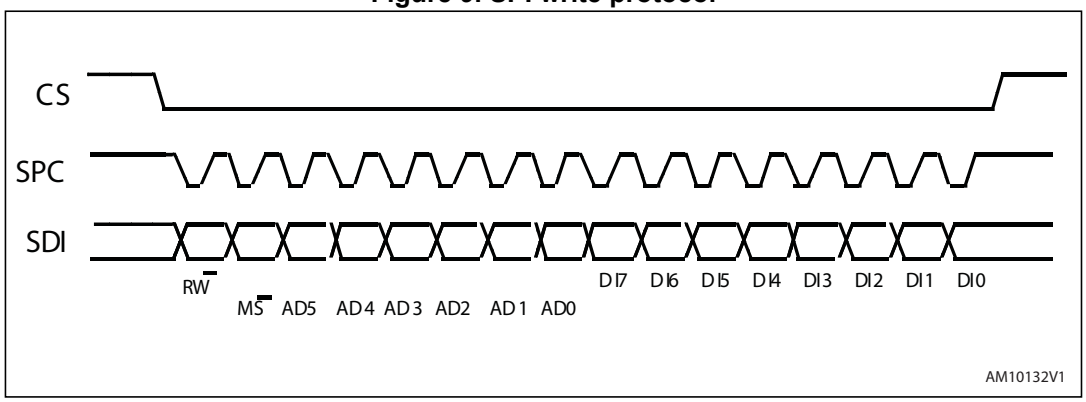
***bit 16-...*** : data DO(...-8). Further data in multiple byte reads.

**Figure 8. Multiple byte SPI read protocol (2-byte example)**



### 5.2.2 SPI write

**Figure 9. SPI write protocol**




The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

***bit 0***: WRITE bit. The value is 0.

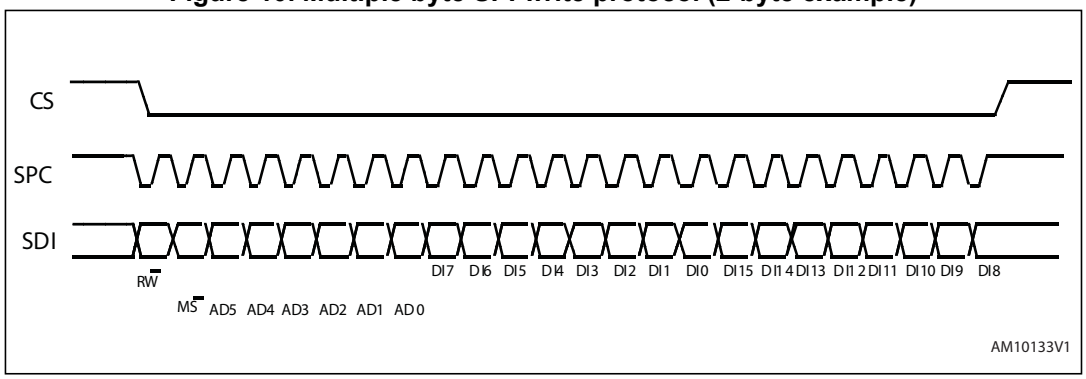
***bit 1***: MS bit. When 0, does not increment the address, when 1, increments the address in multiple writes.

***bit 2 -7***: address AD(5:0). This is the address field of the indexed register.

***bit 8-15***: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

***bit 16-...*** : data DI(...-8). Further data in multiple byte writes.

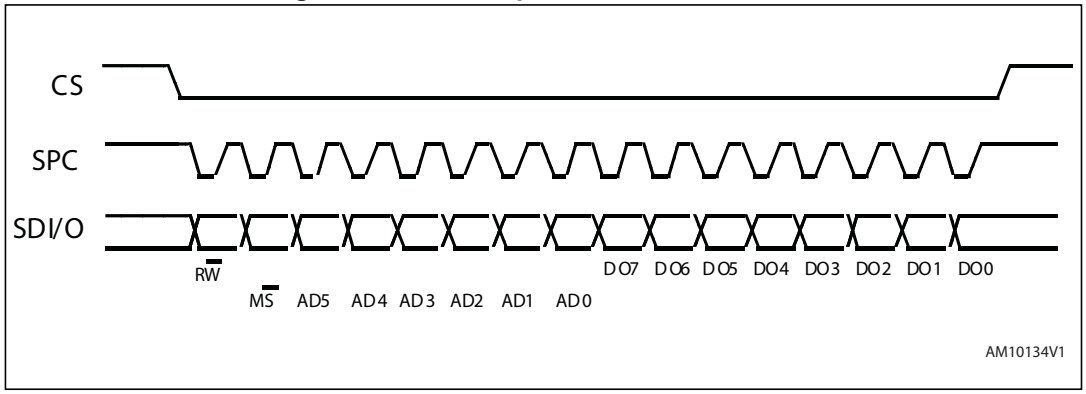
**Figure 10. Multiple byte SPI write protocol (2-byte example)**



### 5.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting bit SIM (SPI serial interface mode selection) to '1' in *CTRL_REG4 (23h)*.

**Figure 11. SPI read protocol in 3-wire mode**




The SPI read command is performed with 16 clock pulses.

***bit 0***: READ bit. The value is 1.

***bit 1***: $M\overline{S}$ bit. When 0, does not increment the address, when 1, increments the address in multiple reads.

***bit 2-7***: address AD(5:0). This is the address field of the indexed register.

***bit 8-15***: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

The multiple read command is also available in 3-wire mode.

# 6 Register mapping

The table given below provides a listing of the 8-bit registers embedded in the device and the corresponding addresses.

**Table 19. Register address map**

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| Reserved | | 00 - 06 | | | Reserved |
| STATUS_REG_AUX | r | 07 | 000 0111 | | |
| Reserved | r | 08-0B | | | Reserved |
| OUT_TEMP_L | r | 0C | 000 1100 | Output | |
| OUT_TEMP_H | r | 0D | 000 1101 | Output | |
| INT_COUNTER_REG | r | 0E | 000 1110 | | |
| WHO_AM_I | r | 0F | 000 1111 | 00110011 | Dummy register |
| Reserved | | 10 - 1E | | | Reserved |
| TEMP_CFG_REG | rw | 1F | 001 1111 | | |
| CTRL_REG1 | rw | 20 | 010 0000 | 00000111 | |
| CTRL_REG2 | rw | 21 | 010 0001 | 00000000 | |
| CTRL_REG3 | rw | 22 | 010 0010 | 00000000 | |
| CTRL_REG4 | rw | 23 | 010 0011 | 00000000 | |
| CTRL_REG5 | rw | 24 | 010 0100 | 00000000 | |
| CTRL_REG6 | rw | 25 | 010 0101 | 00000000 | |
| REFERENCE/DATACAPTURE | rw | 26 | 010 0110 | 00000000 | |
| STATUS_REG | r | 27 | 010 0111 | 00000000 | |
| OUT_X_L | r | 28 | 010 1000 | Output | |
| OUT_X_H | r | 29 | 010 1001 | Output | |
| OUT_Y_L | r | 2A | 010 1010 | Output | |
| OUT_Y_H | r | 2B | 010 1011 | Output | |
| OUT_Z_L | r | 2C | 010 1100 | Output | |
| OUT_Z_H | r | 2D | 010 1101 | Output | |
| FIFO_CTRL_REG | rw | 2E | 010 1110 | 00000000 | |
| FIFO_SRC_REG | r | 2F | 010 1111 | 0010000 | |
| INT1_CFG | rw | 30 | 011 0000 | 00000000 | |
| INT1_SRC | r | 31 | 011 0001 | 00000000 | |
| INT1_THS | rw | 32 | 011 0010 | 00000000 | |
| INT1_DURATION | rw | 33 | 011 0011 | 00000000 | |

Table 19. Register address map (continued)

| Name | Type | Register address | | Default | Comment |
|---|---|---|---|---|---|
| | | Hex | Binary | | |
| INT2_CFG | rw | 34 | 011 0100 | 00000000 | |
| INT2_SRC | r | 35 | 011 0101 | 00000000 | |
| INT2_THS | rw | 36 | 011 0110 | 00000000 | |
| INT2_DURATION | rw | 37 | 011 0111 | 00000000 | |
| CLICK_CFG | rw | 38 | 011 1000 | 00000000 | |
| CLICK_SRC | r | 39 | 011 1001 | 00000000 | |
| CLICK_THS | rw | 3A | 011 1010 | 00000000 | |
| TIME_LIMIT | rw | 3B | 011 1011 | 00000000 | |
| TIME_LATENCY | rw | 3C | 011 1100 | 00000000 | |
| TIME_WINDOW | rw | 3D | 011 1101 | 00000000 | |
| Act_THS | rw | 3E | 011 1110 | 00000000 | |
| Act_DUR | rw | 3F | 011 1111 | 00000000 | |

Registers marked as *Reserved* or not listed in the table above must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

The boot procedure is complete about 5 milliseconds after device power-up.

# 7 Register description

## 7.1 STATUS_REG_AUX (07h)

**Table 20. STATUS_REG_AUX register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| -- | TOR | -- | -- | -- | TDA | -- | -- |

**Table 21. STATUS_REG_AUX description**

| | |
|---|---|
| TOR | Temperature data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: new temperature data has overwritten the previous data) |
| TDA | Temperature new data available. Default value: 0<br>(0: new temperature data is not yet available;<br>1: new temperature data is available) |

## 7.2 OUT_TEMP_L (0Ch), OUT_TEMP_H (0Dh)

Temperature sensor data. Refer to *Section 2.11: Temperature sensor* for details on how to enable and read the temperature sensor output data.

## 7.3 INT_COUNTER_REG (0Eh)

**Table 22. INT_COUNTER_REG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| IC7 | IC6 | IC5 | IC4 | IC3 | IC2 | IC1 | IC0 |

## 7.4 WHO_AM_I (0Fh)

Device identification register.

**Table 23. WHO_AM_I register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

## 7.5 TEMP_CFG_REG (1Fh)

**Table 24. TEMP_CFG_REG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| TEMP_EN1 | TEMP_EN0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table 25. TEMP_CFG_REG description**

| | |
|---|---|
| TEMP_EN[1:0] | Temperature sensor (T) enable. Default value: 00<br>(00: T disabled; 11: T enabled) |

## 7.6 CTRL_REG1 (20h)

**Table 26. CTRL_REG1 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ODR3 | ODR2 | ODR1 | ODR0 | LPen | Zen | Yen | Xen |

**Table 27. CTRL_REG1 description**

| | |
|---|---|
| ODR[3:0] | Data rate selection. Default value: 0000<br>(0000: power-down mode; others: refer to *Table 28*) |
| LPen | Low-power mode enable. Default value: 0<br>(0: normal mode, 1: low-power mode)<br>(Refer to section *2.6.3: High-resolution, normal mode, low-power mode*) |
| Zen | Z-axis enable. Default value: 1<br>(0: Z-axis disabled; 1: Z-axis enabled) |
| Yen | Y-axis enable. Default value: 1<br>(0: Y-axis disabled; 1: Y-axis enabled) |
| Xen | X-axis enable. Default value: 1<br>(0: X-axis disabled; 1: X-axis enabled) |

**ODR[3:0]** is used to set the power mode and ODR selection. The following table indicates the frequency of each combination of ODR[3:0].

**Table 28. Data rate configuration**

| ODR3 | ODR2 | ODR1 | ODR0 | Power mode selection |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Power-down mode |
| 0 | 0 | 0 | 1 | HR / Normal / Low-power mode (1 Hz) |
| 0 | 0 | 1 | 0 | HR / Normal / Low-power mode (10 Hz) |
| 0 | 0 | 1 | 1 | HR / Normal / Low-power mode (25 Hz) |
| 0 | 1 | 0 | 0 | HR / Normal / Low-power mode (50 Hz) |
| 0 | 1 | 0 | 1 | HR / Normal / Low-power mode (100 Hz) |
| 0 | 1 | 1 | 0 | HR / Normal / Low-power mode (200 Hz) |
| 0 | 1 | 1 | 1 | HR/ Normal / Low-power mode (400 Hz) |
| 1 | 0 | 0 | 0 | Low-power mode (1.620 kHz) |
| 1 | 0 | 0 | 1 | HR/ Normal (1.344 kHz);<br>Low-power mode (5.376 kHz) |

## 7.7 CTRL_REG2 (21h)

**Table 29. CTRL_REG2 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| HPM1 | HPM0 | HPCF2 | HPCF1 | FDS | HPCLICK | HPIS2 | HPIS1 |

**Table 30. CTRL_REG2 description**

| | |
|---|---|
| HPM[1:0] | High-pass filter mode selection. Default value: 00<br>Refer to *Table 31* for filter mode configuration |
| HPCF[2:1] | High-pass filter cutoff frequency selection. Refer to *Table 32*. |
| FDS | Filtered data selection. Default value: 0<br>(0: internal filter bypassed; 1: data from internal filter sent to output register and FIFO) |
| HPCLICK | High-pass filter enable for CLICK function.<br>(0: filter bypassed; 1: filter enabled) |
| HPIS2 | High-pass filter enable for AOI function on Interrupt 2.<br>(0: filter bypassed; 1: filter enabled) |
| HPIS1 | High-pass filter enable for AOI function on Interrupt 1.<br>(0: filter bypassed; 1: filter enabled) |

**Table 31. High-pass filter mode configuration**

| HPM1 | HPM0 | High-pass filter mode |
|---|---|---|
| 0 | 0 | Normal mode (reset by reading *REFERENCE/DATACAPTURE (26h)* register) |
| 0 | 1 | Reference signal for filtering |
| 1 | 0 | Normal mode |
| 1 | 1 | Autoreset on interrupt event |

The bandwidth of the high-pass filter depends on the selected ODR and on the settings of the HPCFx bits of CTRL_REG2. The high-pass filter cutoff frequencies ($f_t$) are shown in *Table 32*.

**Table 32. Low-power mode - high-pass filter cutoff frequency**

| HPCF[2:1] | $f_t$ [Hz] @ 1 Hz | $f_t$ [Hz] @ 10 Hz | $f_t$ [Hz] @ 25 Hz | $f_t$ [Hz] @ 50 Hz | $f_t$ [Hz] @ 100 Hz | $f_t$ [Hz] @ 200Hz | $f_t$ [Hz] @ 400 Hz | $f_t$ [Hz] @ 1.6kHz | $f_t$ [Hz] @ 5kHz |
|---|---|---|---|---|---|---|---|---|---|
| 00 | 0.02 | 0.2 | 0.5 | 1 | 2 | 4 | 8 | 32 | 100 |
| 01 | 0.008 | 0.08 | 0.2 | 0.5 | 1 | 2 | 4 | 16 | 50 |
| 10 | 0.004 | 0.04 | 0.1 | 0.2 | 0.5 | 1 | 2 | 8 | 25 |
| 11 | 0.002 | 0.02 | 0.05 | 0.1 | 0.2 | 0.5 | 1 | 4 | 12 |

## 7.8 CTRL_REG3 (22h)

**Table 33. CTRL_REG3 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| I1_CLICK | I1_AOI1 | I1_AOI2 | I1_DRDY1 | I1_DRDY2 | I1_WTM | I1_OVERRUN | -- |

**Table 34. CTRL_REG3 description**

| | |
|---|---|
| I1_CLICK | CLICK interrupt on INT1 pin. Default value 0.<br>(0: disable; 1: enable) |
| I1_AOI1 | AOI1 interrupt on INT1 pin. Default value 0.<br>(0: disable; 1: enable) |
| I1_AOI2 | AOI2 interrupt on INT1 pin. Default value 0.<br>(0: disable; 1: enable) |
| I1_DRDY1 | DRDY1 interrupt on INT1 pin. Default value 0.<br>(0: disable; 1: enable) |
| I1_DRDY2 | DRDY2 interrupt on INT1 pin. Default value 0.<br>(0: disable; 1: enable) |
| I1_WTM | FIFO watermark interrupt on INT1 pin. Default value 0.<br>(0: disable; 1: enable) |
| I1_OVERRUN | FIFO overrun interrupt on INT1 pin. Default value 0.<br>(0: disable; 1: enable) |

## 7.9 CTRL_REG4 (23h)

**Table 35. CTRL_REG4 register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BDU | BLE(1) | FS1 | FS0 | HR | ST1 | ST0 | SIM |

1. The BLE function can be activated only in high-resolution mode

**Table 36. CTRL_REG4 description**

| | |
|---|---|
| BDU | Block data update. Default value: 0<br>(0: continuous update; 1: output registers not updated until MSB and LSB have been read) |
| BLE | Big/Little Endian data selection. Default value: 0<br>(0: data LSb at lower address; 1: data MSb at lower address)<br>The BLE function can be activated only in high-resolution mode |
| FS[1:0] | Full-scale selection. Default value: 00<br>(00: ±2 *g*; 01: ±4 *g*; 10: ±8 *g*; 11: ±16 *g*) |
| HR | Operating mode selection (refer to section *2.6.3: High-resolution, normal mode, low-power mode*) |
| ST[1:0] | Self-test enable. Default value: 00<br>(00: self-test disabled; other: see *Table 37*) |
| SIM | SPI serial interface mode selection. Default value: 0<br>(0: 4-wire interface; 1: 3-wire interface). |

Table 37. Self-test mode configuration

| ST1 | ST0 | Self-test mode |
|---|---|---|
| 0 | 0 | Normal mode |
| 0 | 1 | Self test 0 |
| 1 | 0 | Self test 1 |
| 1 | 1 | -- |

## 7.10 CTRL_REG5 (24h)

Table 38. CTRL_REG5 register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| BOOT | FIFO_EN | -- | -- | LIR_INT1 | D4D_INT1 | LIR_INT2 | D4D_INT2 |

Table 39. CTRL_REG5 description

| | |
|---|---|
| BOOT | Reboot memory content. Default value: 0<br>(0: normal mode; 1: reboot memory content) |
| FIFO_EN | FIFO enable. Default value: 0<br>(0: FIFO disabled; 1: FIFO enabled) |
| LIR_INT1 | Latch interrupt request on *INT1_SRC (31h)*, with *INT1_SRC (31h)* register cleared by reading *INT1_SRC (31h)* itself. Default value: 0.<br>(0: interrupt request not latched; 1: interrupt request latched) |
| D4D_INT1 | 4D enable: 4D detection is enabled on INT1 pin when 6D bit on *INT1_CFG (30h)* is set to 1. |
| LIR_INT2 | Latch interrupt request on *INT2_SRC (35h)* register, with *INT2_SRC (35h)* register cleared by reading *INT2_SRC (35h)* itself. Default value: 0.<br>(0: interrupt request not latched; 1: interrupt request latched) |
| D4D_INT2 | 4D enable: 4D detection is enabled on INT2 pin when 6D bit on *INT2_CFG (34h)* is set to 1. |

## 7.11 CTRL_REG6 (25h)

Table 40. CTRL_REG6 register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| I2_CLICKen | I2_INT1 | I2_INT2 | BOOT_I2 | P2_ACT | - - | H_LACTIVE | -- |

Table 41. CTRL_REG6 description

| | |
|---|---|
| I2_CLICKen | Click interrupt on INT2 pin. Default value: 0<br>(0: disabled; 1: enabled) |
| I2_INT1 | Interrupt 1 function enable on INT2 pin. Default value: 0<br>(0: function disabled; 1: function enabled) |

Table 41. CTRL_REG6 description (continued)

| | |
|---|---|
| I2_INT2 | Interrupt 2 function enable on INT2 pin. Default value: 0<br>(0: function disabled; 1: function enabled) |
| BOOT_I2 | Boot on INT2 pin enable. Default value: 0<br>(0: disabled; 1:enabled) |
| P2_ACT | Activity interrupt enable on INT2 pin. Default value: 0.<br>(0: disabled; 1:enabled) |
| H_LACTIVE | Interrupt active. Default value: 0.<br>(0: interrupt active-high; 1: interrupt active-low) |

## 7.12 REFERENCE/DATACAPTURE (26h)

Table 42. REFERENCE/DATACAPTURE register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Ref7 | Ref6 | Ref5 | Ref4 | Ref3 | Ref2 | Ref1 | Ref0 |

Table 43. REFERENCE/DATACAPTURE description

| | |
|---|---|
| Ref [7:0] | Reference value for interrupt generation. Default value: 0 |

## 7.13 STATUS_REG (27h)

Table 44. STATUS_REG register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ZYXOR | ZOR | YOR | XOR | ZYXDA | ZDA | YDA | XDA |

Table 45. STATUS_REG description

| | |
|---|---|
| ZYXOR | X-, Y- and Z-axis data overrun. Default value: 0<br>(0: no overrun has occurred; 1: a new set of data has overwritten the previous set) |
| ZOR | Z-axis data overrun. Default value: 0<br>(0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data) |
| YOR | Y-axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: new data for the Y-axis has overwritten the previous data) |
| XOR | X-axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: new data for the X-axis has overwritten the previous data) |
| ZYXDA | X-, Y- and Z-axis new data available. Default value: 0<br>(0: a new set of data is not yet available; 1: a new set of data is available) |
| ZDA | Z-axis new data available. Default value: 0<br>(0: new data for the Z-axis is not yet available;<br>1: new data for the Z-axis is available) |
| YDA | Y-axis new data available. Default value: 0<br>(0: new data for the Y-axis is not yet available;<br>1: new data for the Y-axis is available) |

## 7.14 OUT_X_L (28h), OUT_X_H (29h)

X-axis acceleration data. The value is expressed as two's complement left-justified.
Please refer to *Section 2.6.3: High-resolution, normal mode, low-power mode*.

## 7.15 OUT_Y_L (2Ah), OUT_Y_H (2Bh)

Y-axis acceleration data. The value is expressed as two's complement left-justified.
Please refer to *Section 2.6.3: High-resolution, normal mode, low-power mode*.

## 7.16 OUT_Z_L (2Ch), OUT_Z_H (2Dh)

Z-axis acceleration data. The value is expressed as two's complement left-justified.
Please refer to *Section 2.6.3: High-resolution, normal mode, low-power mode*.

## 7.17 FIFO_CTRL_REG (2Eh)

**Table 46. FIFO_CTRL_REG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| FM1 | FM0 | TR | FTH4 | FTH3 | FTH2 | FTH1 | FTH0 |

**Table 47. FIFO_CTRL_REG description**

| | |
|---|---|
| FM[1:0] | FIFO mode selection. Default value: 00 (see *Table 48*) |
| TR | Trigger selection. Default value: 0<br>0: trigger event allows triggering signal on INT1<br>1: trigger event allows triggering signal on INT2 |
| FTH[4:0] | Default value: 00000 |

**Table 48. FIFO mode configuration**

| FM1 | FM0 | FIFO mode |
|---|---|---|
| 0 | 0 | Bypass mode |
| 0 | 1 | FIFO mode |
| 1 | 0 | Stream mode |
| 1 | 1 | Stream-to-FIFO mode |

## 7.18 FIFO_SRC_REG (2Fh)

**Table 49. FIFO_SRC_REG register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| WTM | OVRN_FIFO | EMPTY | FSS4 | FSS3 | FSS2 | FSS1 | FSS0 |

Table 50. FIFO_SRC_REG description

| | |
|---|---|
| WTM | WTM bit is set high when FIFO content exceeds watermark level. |
| OVRN_FIFO | OVRN bit is set high when FIFO buffer is full; this means that the FIFO buffer contains 32 unread samples. At the following ODR a new sample set replaces the oldest FIFO value. The OVRN bit is set to 0 when the first sample set has been read. |
| EMPTY | EMPTY flag is set high when all FIFO samples have been read and FIFO is empty. |
| FSS [4:0] | FSS [4:0] field always contains the current number of unread samples stored in the FIFO buffer. When FIFO is enabled, this value increases at ODR frequency until the buffer is full, whereas, it decreases every time one sample set is retrieved from FIFO. |

## 7.19 INT1_CFG (30h)

Table 51. INT1_CFG register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| AOI | 6D | ZHIE/ ZUPE | ZLIE/ ZDOWNE | YHIE/ YUPE | YLIE/ YDOWNE | XHIE/ XUPE | XLIE/ XDOWNE |

Table 52. INT1_CFG description

| | |
|---|---|
| AOI | And/Or combination of interrupt events. Default value: 0. Refer to *Table 53* |
| 6D | 6-direction detection function enabled. Default value: 0. Refer to *Table 53* |
| ZHIE/ ZUPE | Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request) |
| ZLIE/ ZDOWNE | Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request) |
| YHIE/ YUPE | Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.) |
| YLIE/ YDOWNE | Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.) |
| XHIE/ XUPE | Enable interrupt generation on X high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.) |
| XLIE/ XDOWNE | Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.) |

The content of this register is loaded at boot.

A write operation to this address is possible only after system boot.

Table 53. Interrupt mode

| AOI | 6D | Interrupt mode |
|---|---|---|
| 0 | 0 | OR combination of interrupt events |
| 0 | 1 | 6-direction movement recognition |
| 1 | 0 | AND combination of interrupt events |
| 1 | 1 | 6-direction position recognition |

The difference between AOI-6D = ‘01’ and AOI-6D = ‘11’.

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when the orientation moves from an unknown zone to a known zone. The interrupt signal remains for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when the orientation is inside a known zone. The interrupt signal remains while the orientation is inside the zone.

## 7.20 INT1_SRC (31h)

**Table 54. INT1_SRC register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | IA | ZH | ZL | YH | YL | XH | XL |

**Table 55. INT1_SRC description**

| | |
|---|---|
| IA | Interrupt active. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupts have been generated) |
| ZH | Z high. Default value: 0<br>(0: no interrupt, 1: Z high event has occurred) |
| ZL | Z low. Default value: 0<br>(0: no interrupt; 1: Z low event has occurred) |
| YH | Y high. Default value: 0<br>(0: no interrupt, 1: Y high event has occurred) |
| YL | Y low. Default value: 0<br>(0: no interrupt, 1: Y low event has occurred) |
| XH | X high. Default value: 0<br>(0: no interrupt, 1: X high event has occurred) |
| XL | X low. Default value: 0<br>(0: no interrupt, 1: X low event has occurred) |

Interrupt 1 source register. Read-only register.

Reading at this address clears the *INT1_SRC (31h)* IA bit (and the interrupt signal on the INT1 pin) and allows the refresh of data in the *INT1_SRC (31h)* register if the latched option was chosen.

## 7.21 INT1_THS (32h)

**Table 56. INT1_THS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | THS6 | THS5 | THS4 | THS3 | THS2 | THS1 | THS0 |

Table 57. INT1_THS description

| | |
|---|---|
| THS[6:0] | Interrupt 1 threshold. Default value: 000 0000<br>1 LSb = 16 mg @ FS = 2 *g*<br>1 LSb = 32 mg @ FS = 4 *g*<br>1 LSb = 62 mg @ FS = 8 *g*<br>1 LSb = 186 mg @ FS = 16 *g* |

## 7.22 INT1_DURATION (33h)

Table 58. INT1_DURATION register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Table 59. INT1_DURATION description

| | |
|---|---|
| D[6:0] | Duration value. Default value: 000 0000<br>1 LSb = 1/ODR |

The **D[6:0]** bits set the minimum duration of the interrupt 1 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

Duration time is measured in N/ODR, where N is the content of the duration register.

## 7.23 INT2_CFG (34h)

Table 60. INT2_CFG register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| AOI | 6D | ZHIE | ZLIE | YHIE | YLIE | XHIE | XLIE |

Table 61. INT2_CFG description

| | |
|---|---|
| AOI | AND/OR combination of interrupt events. Default value: 0<br>(see *Table 62*) |
| 6D | 6-direction detection function enabled. Default value: 0. Refer to *Table 62.* |
| ZHIE | Enable interrupt generation on Z high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| ZLIE | Enable interrupt generation on Z low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |
| YHIE | Enable interrupt generation on Y high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |

Table 61. INT2_CFG description (continued)

| | |
|---|---|
| YLIE | Enable interrupt generation on Y low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |
| XHIE | Enable interrupt generation on X high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| XLIE | Enable interrupt generation on X low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold) |

The content of this register is loaded at boot.

A write operation to this address is possible only after system boot.

Table 62. Interrupt mode

| AOI | 6D | Interrupt mode |
|---|---|---|
| 0 | 0 | OR combination of interrupt events |
| 0 | 1 | 6-direction movement recognition |
| 1 | 0 | AND combination of interrupt events |
| 1 | 1 | 6-direction position recognition |

The difference between AOI-6D = ‘01’ and AOI-6D = ‘11’.

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when the orientation moves from an unknown zone to a known zone. The interrupt signal remains for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when the orientation is inside a known zone. The interrupt signal remains while the orientation is inside the zone.

## 7.24 INT2_SRC (35h)

Table 63. INT2_SRC register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | IA | ZH | ZL | YH | YL | XH | XL |

Table 64. INT2_SRC description

| | |
|---|---|
| IA | Interrupt active. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupts have been generated) |
| ZH | Z high. Default value: 0<br>(0: no interrupt, 1: Z high event has occurred) |
| ZL | Z low. Default value: 0<br>(0: no interrupt; 1: Z low event has occurred) |
| YH | Y high. Default value: 0<br>(0: no interrupt, 1: Y high event has occurred) |

Table 64. INT2_SRC description (continued)

| | |
|---|---|
| YL | Y low. Default value: 0<br>(0: no interrupt, 1: Y low event has occurred) |
| XH | X high. Default value: 0<br>(0: no interrupt, 1: X high event has occurred) |
| XL | X low. Default value: 0<br>(0: no interrupt, 1: X low event has occurred) |

Interrupt 2 source register. Read-only register.

Reading at this address clears the *INT2_SRC (35h)* IA bit (and the interrupt signal on the INT2 pin) and allows the refresh of data in the *INT2_SRC (35h)* register if the latched option was chosen.

## 7.25 INT2_THS (36h)

Table 65. INT2_THS register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | THS6 | THS5 | THS4 | THS3 | THS2 | THS1 | THS0 |

Table 66. INT2_THS description

| | |
|---|---|
| THS[6:0] | Interrupt 2 threshold. Default value: 000 0000<br>1 LSb = 16 m*g* @ FS = 2 *g*<br>1 LSb = 32 m*g* @ FS = 4 *g*<br>1 LSb = 62 m*g* @ FS = 8 *g*<br>1 LSb = 186 m*g* @ FS = 16 *g* |

## 7.26 INT2_DURATION (37h)

Table 67. INT2_DURATION register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Table 68. INT2_DURATION description

| | |
|---|---|
| D[6:0] | Duration value. Default value: 000 0000<br>1 LSb = 1/ODR(1) |

1. Duration time is measured in N/ODR, where N is the content of the duration register.

The **D[6:0]** bits set the minimum duration of the Interrupt 2 event to be recognized. Duration time steps and maximum values depend on the ODR chosen.

## 7.27 CLICK_CFG (38h)

Table 69. CLICK_CFG register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| -- | -- | ZD | ZS | YD | YS | XD | XS |

Table 70. CLICK_CFG description

| | |
|---|---|
| ZD | Enable interrupt double-click on Z-axis. Default value: 0<br>(0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold) |
| ZS | Enable interrupt single-click on Z-axis. Default value: 0<br>(0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold) |
| YD | Enable interrupt double-click on Y-axis. Default value: 0<br>(0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold) |
| YS | Enable interrupt single-click on Y-axis. Default value: 0<br>(0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold) |
| XD | Enable interrupt double-click on X-axis. Default value: 0<br>(0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold) |
| XS | Enable interrupt single-click on X-axis. Default value: 0<br>(0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold) |

## 7.28 CLICK_SRC (39h)

Table 71. CLICK_SRC register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | IA | DClick | SClick | Sign | Z | Y | X |

Table 72. CLICK_SRC description

| | |
|---|---|
| IA | Interrupt active. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupts have been generated) |
| DClick | Double-click enable. Default value: 0 (0: double-click detection disabled,<br>1: double-click detection enabled) |
| SClick | Single-click enable. Default value: 0 (0: single-click detection disabled, 1: single-click detection enabled) |
| Sign | Click sign. 0: positive detection, 1: negative detection |
| Z | Z click detection. Default value: 0<br>(0: no interrupt, 1: Z high event has occurred) |
| Y | Y click detection. Default value: 0<br>(0: no interrupt, 1: Y high event has occurred) |
| X | X click detection. Default value: 0<br>(0: no interrupt, 1: X high event has occurred) |

## 7.29 CLICK_THS (3Ah)

**Table 73. CLICK_THS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| - | Ths6 | Ths5 | Ths4 | Ths3 | Ths2 | Ths1 | Ths0 |

**Table 74. CLICK_SRC description**

| | |
|---|---|
| Ths[6:0] | Click threshold. Default value: 000 0000 |

## 7.30 TIME_LIMIT (3Bh)

**Table 75. TIME_LIMIT register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| - | TLI6 | TLI5 | TLI4 | TLI3 | TLI2 | TLI1 | TLI0 |

**Table 76. TIME_LIMIT description**

| | |
|---|---|
| TLI[6:0] | Click time limit. Default value: 000 0000 |

## 7.31 TIME_LATENCY (3Ch)

**Table 77. TIME_LATENCY register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| TLA7 | TLA6 | TLA5 | TLA4 | TLA3 | TLA2 | TLA1 | TLA0 |

**Table 78. TIME_LATENCY description**

| | |
|---|---|
| TLA[7:0] | Click time latency. Default value: 0000 0000 |

## 7.32 TIME_WINDOW (3Dh)

**Table 79. TIME_WINDOW register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| TW7 | TW6 | TW5 | TW4 | TW3 | TW2 | TW1 | TW0 |

**Table 80. TIME_WINDOW description**

| | |
|---|---|
| TW[7:0] | Click time window |

## 7.33 Act_THS (3Eh)

**Table 81. Act_THS register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| -- | Acth6 | Acth5 | Acth4 | Acth3 | Acth2 | Acth1 | Acth0 |

**Table 82. Act_THS description**

| | |
|---|---|
| Acth[6:0] | Sleep-to-wake, return-to-sleep activation threshold in low-power mode<br>1 LSb = 16 m*g* @ FS = 2 *g*<br>1 LSb = 32 m*g* @ FS = 4 *g*<br>1 LSb = 62 m*g* @ FS = 8 *g*<br>1 LSb = 186 m*g* @ FS = 16 *g* |

## 7.34 Act_DUR (3Fh)

**Table 83. Act_DUR register**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ActD7 | ActD6 | ActD5 | ActD4 | ActD3 | ActD2 | ActD1 | ActD0 |

**Table 84. Act_DUR description**

| | |
|---|---|
| ActD[7:0] | Sleep-to-wake, return-to-sleep duration<br>1 LSb = (8*1[LSb]+1)/ODR |

# 8 Package information

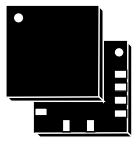
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 8.1 LGA package information

**Figure 12. LGA-12 package outline and mechanical data**

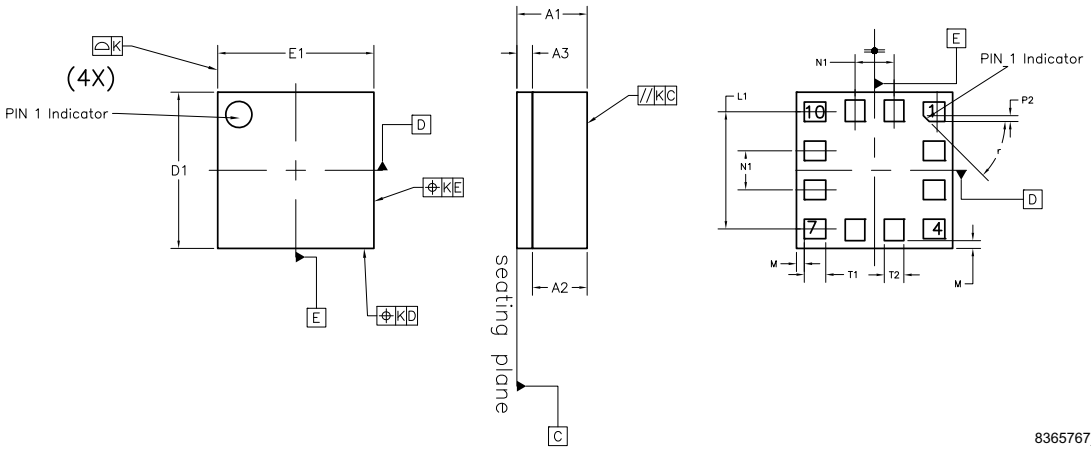
| | Dimensions (mm) | | |
|---|---|---|---|
| Ref. | Min. | Typ. | Max. |
| A1 | | | 1 |
| A2 | | 0.785 | |
| A3 | | 0.200 | |
| D1 | 1.850 | 2.000 | 2.150 |
| E1 | 1.850 | 2.000 | 2.150 |
| L1 | | 1.500 | |
| N1 | | 0.500 | |
| T1 | | 0.275 | |
| T2 | | 0.250 | |
| P2 | | 0.075 | |
| r | | 45° | |
| M | | 0.100 | |
| K | | 0.050 | |

Outline and mechanical data



LGA-12 (2.0x2.0x1 mm)

Land Grid Array Package



# 9 Revision history

Table 85. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 24-Mar-2015 | 1 | Initial release |
| 21-Apr-2015 | 2 | First public release |

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