STL8N6LF6AG

Automotive-grade N-channel 60 V, 21 mΩ typ., 32 A STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

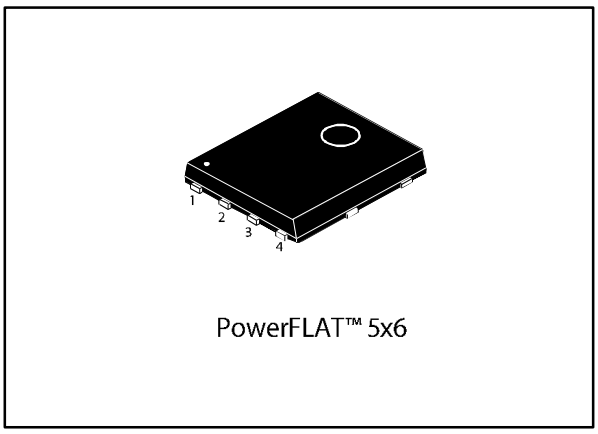
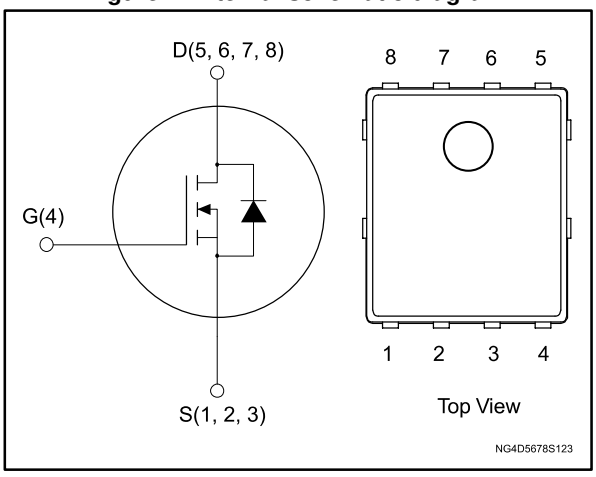


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STL8N6LF6AG	60 V	27 mΩ	32 A	55 W

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flank package

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STL8N6LF6AG	8N6LF6	PowerFLAT™ 5x6	Tape and reel

This is information on a product in full production.

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_{case} = 25 °C	32	A
	Drain current (continuous) at T_{case} = 100 °C	23	
I_D(1)	Drain current (continuous) at T_{pcb} = 25 °C	9.6	A
	Drain current (continuous) at T_{pcb} = 100 °C	6.8	
I_{DM}(1)(2)	Drain current (pulsed)	38	A
I_{DM}(2)	Drain current (pulsed)	128	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	55	W
P_{TOT}	Total dissipation at T_{pcb} = 25 °C	4.8	
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Operating junction temperature		

Notes:

(1) When mounted on a 1-inch² FR-4, 2 Oz copper board, t < 10 s.

(2) Pulse width is limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.7	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	31.3	

Notes:

(1) When mounted on a 1-inch² FR-4, 2 Oz copper board, t < 10 s.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AV}	Avalanche current, not repetitive	32	A
E_{AS}(1)	Single pulse avalanche energy	120	mJ

Notes:

(1) starting T_j = 25 °C, I_D = I_{AV}, V_{DD} = 43.5 V.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 60 V			1	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 9.6 A		21	27	mΩ
		V_{GS} = 4.5 V, I_D = 9.6 A		25	31	

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	1340	-	pF
C_{oss}	Output capacitance		-	90	-	
C_{rss}	Reverse transfer capacitance		-	60	-	
Q_g	Total gate charge	V_{DD} = 30 V, I_D = 9.6 A, V_{GS} = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	27	-	nC
Q_{gs}	Gate-source charge		-	4.6	-	
Q_{gd}	Gate-drain charge		-	4.3	-	

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 12.5 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*)	-	9.6	-	ns
t_r	Rise time		-	20	-	
$t_{d(off)}$	Turn-off delay time		-	56	-	
t_f	Fall time		-	7	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		9.6	A
I_{SDM}(1)	Source-drain current (pulsed)		-		38	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 9.6 A	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 25 A, di/dt = 100 A/µs, V_{DD} = 48 V (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	22.5		ns
Q_{rr}	Reverse recovery charge		-	22.2		nC
I_{RRM}	Reverse recovery current		-	2.0		A

Notes:

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

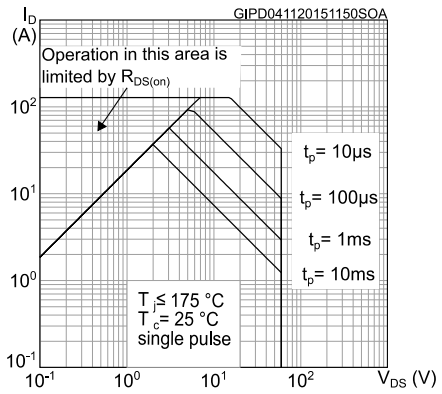


Figure 3: Thermal impedance

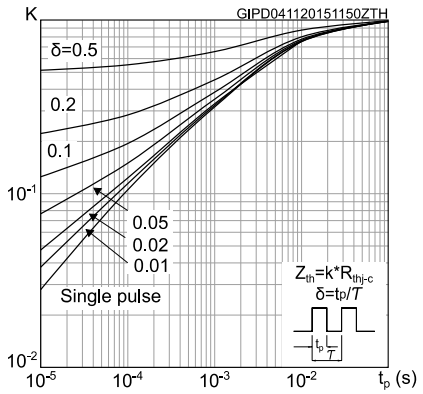


Figure 4: Output characteristics

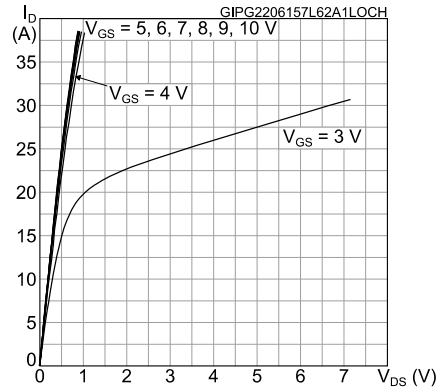


Figure 5: Transfer characteristics

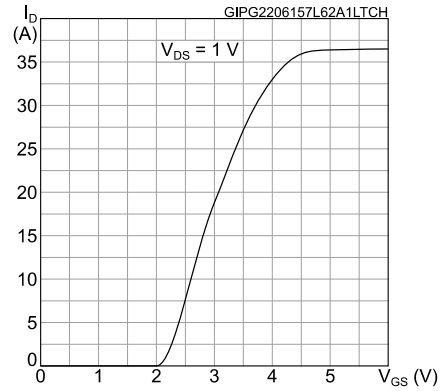


Figure 6: Gate charge vs gate-source voltage

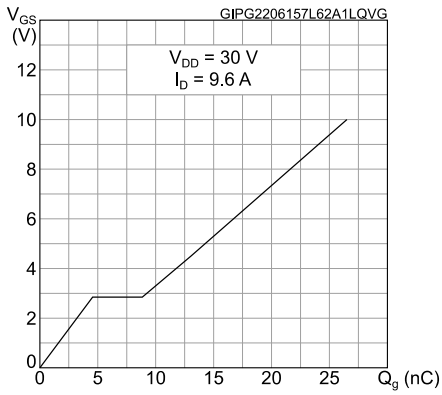


Figure 7: Static drain-source on-resistance

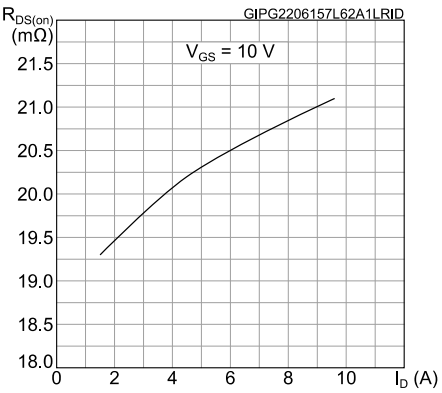


Figure 8: Capacitance variations

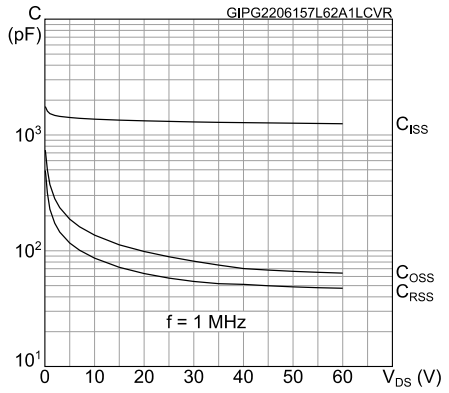


Figure 9: Normalized gate threshold voltage vs temperature

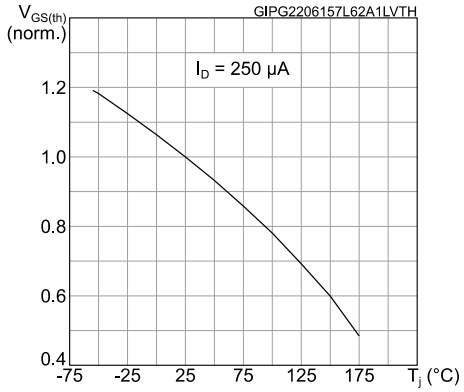


Figure 10: Normalized on-resistance vs temperature

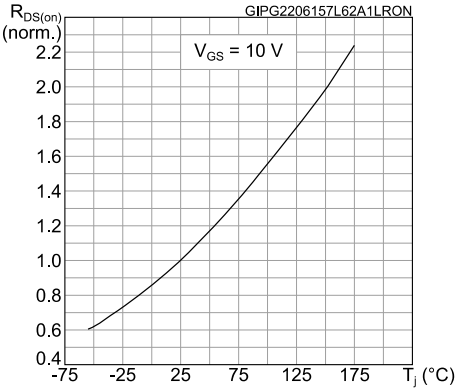


Figure 11: Normalized V(BR)DSS vs temperature

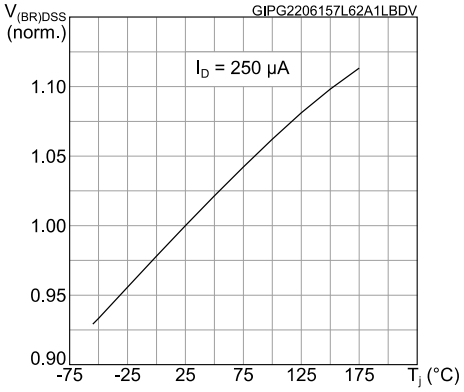
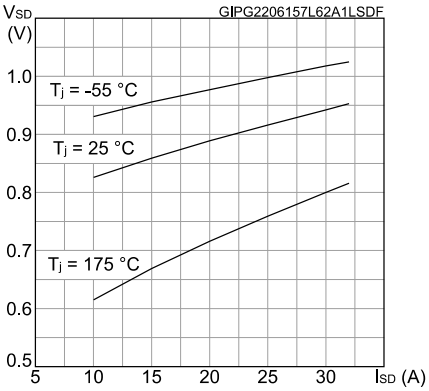


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

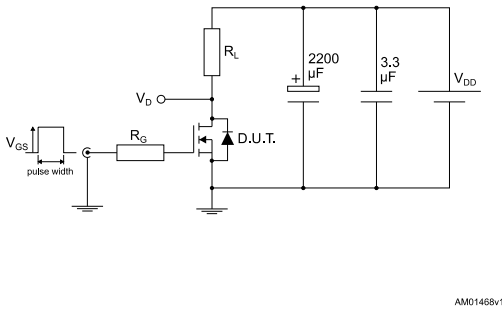


Figure 14: Test circuit for gate charge behavior

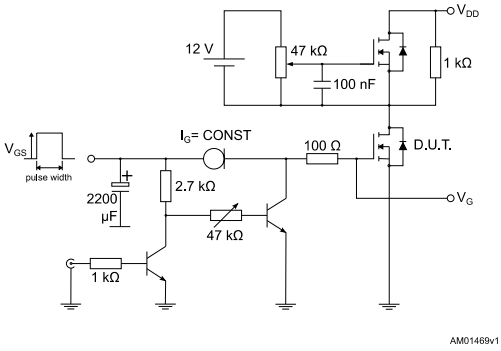


Figure 15: Test circuit for inductive load switching and diode recovery times

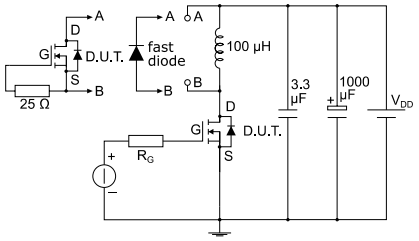


Figure 16: Unclamped inductive load test circuit

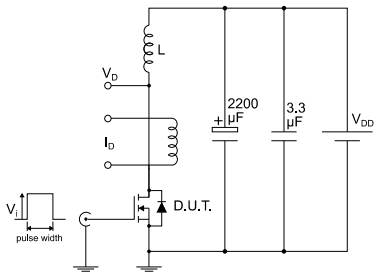


Figure 17: Unclamped inductive waveform

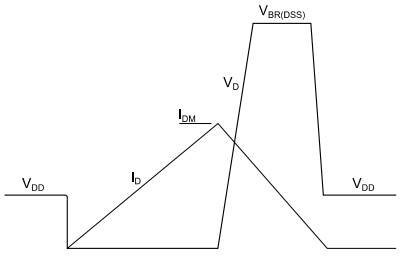
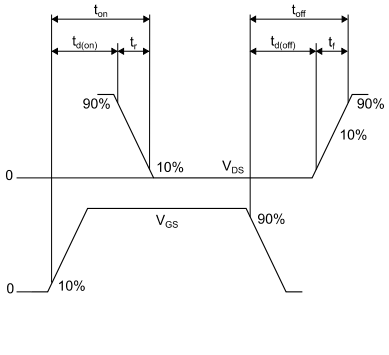


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 WF type R package information

Figure 19: PowerFLAT™ 5x6 WF type R package outline

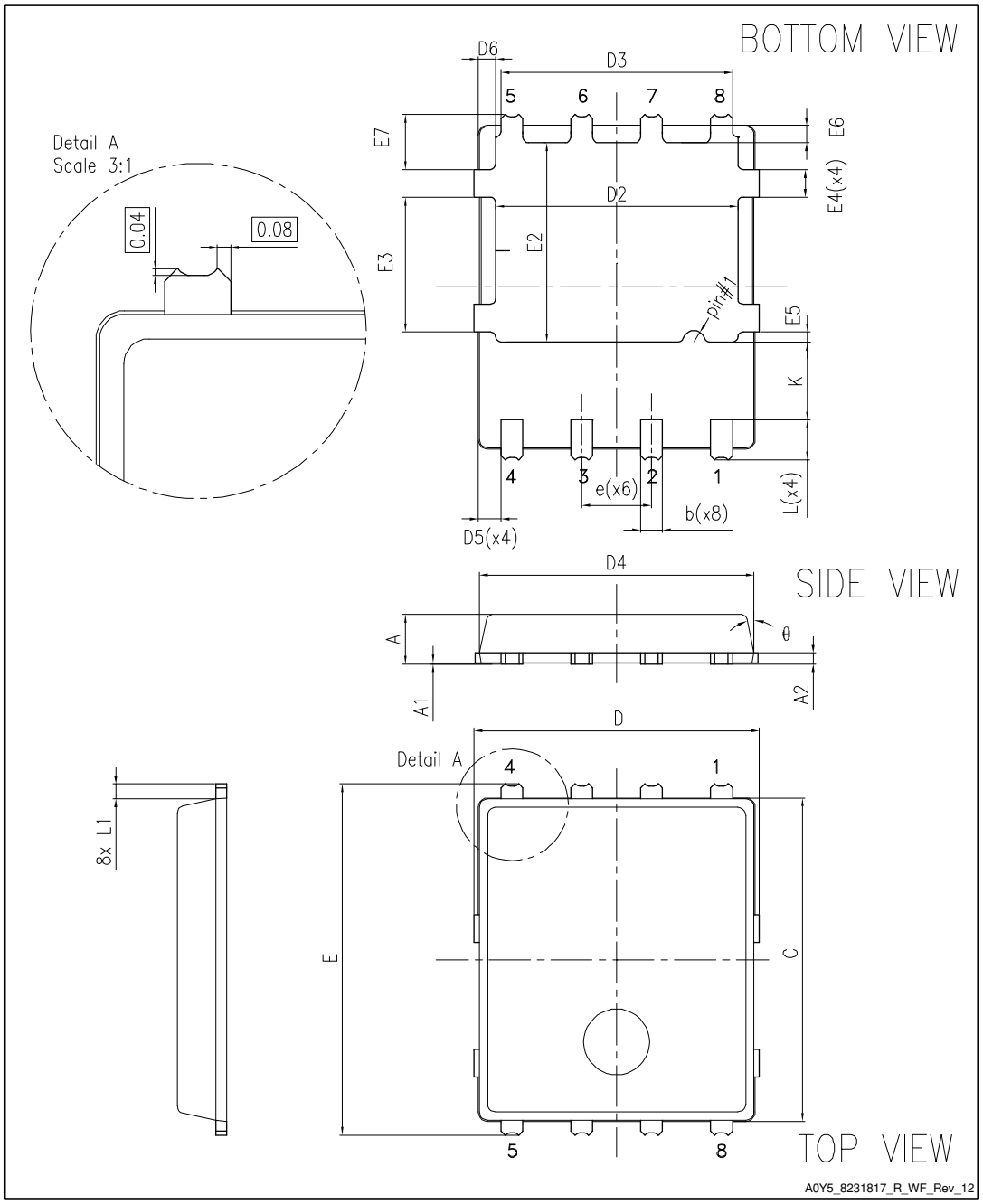
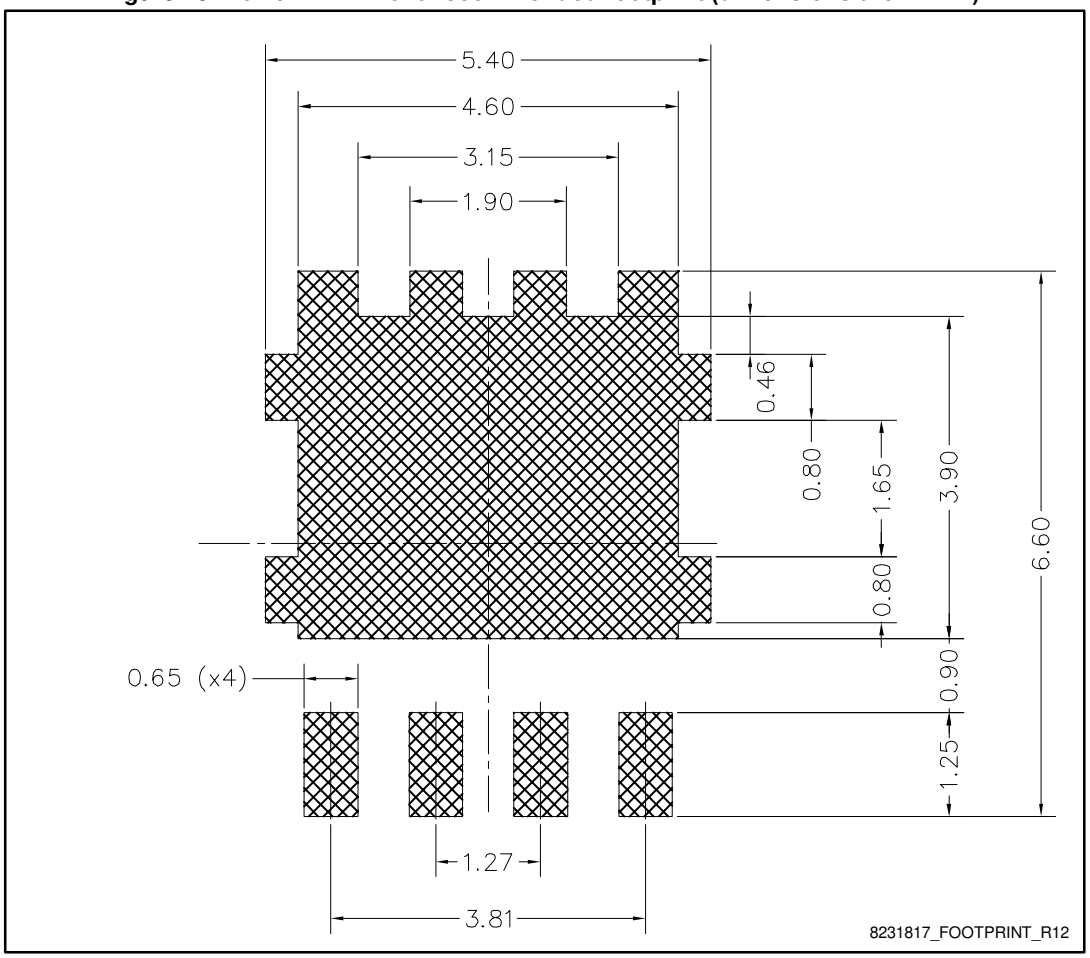


Table 9: PowerFLAT™ 5x6 WF type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.0	5.20
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.175	0.325	0.450
E7	0.85	1.00	1.15
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
Θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 WF packing information

Figure 21: PowerFLAT™ 5x6 WF tape

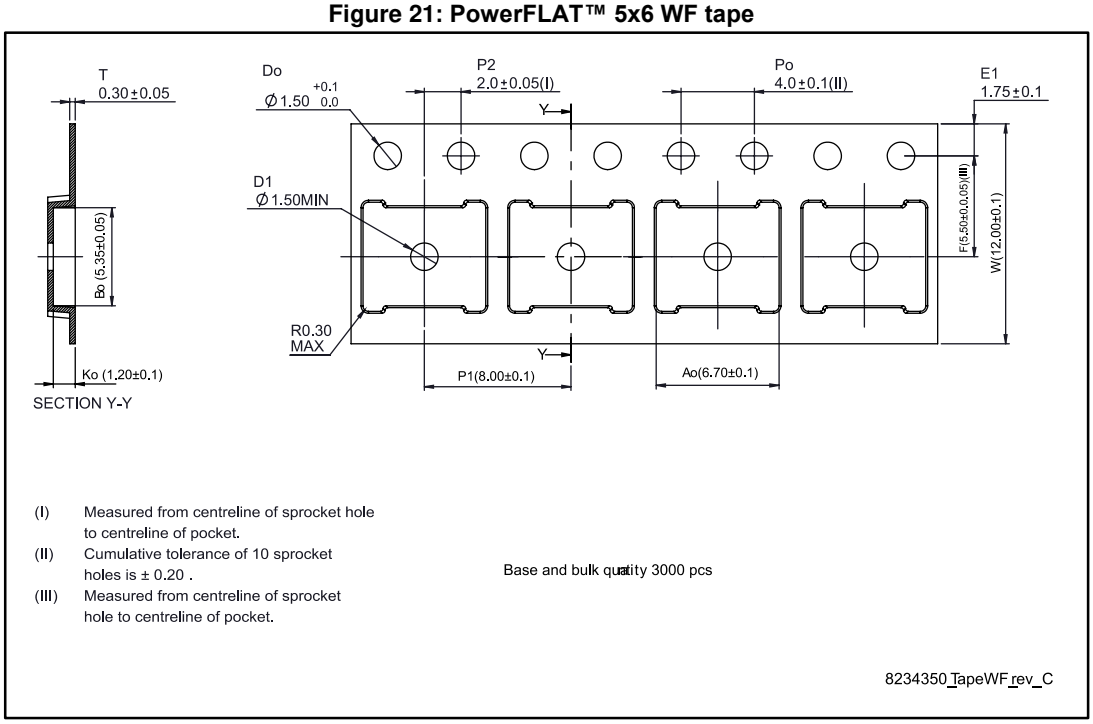


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

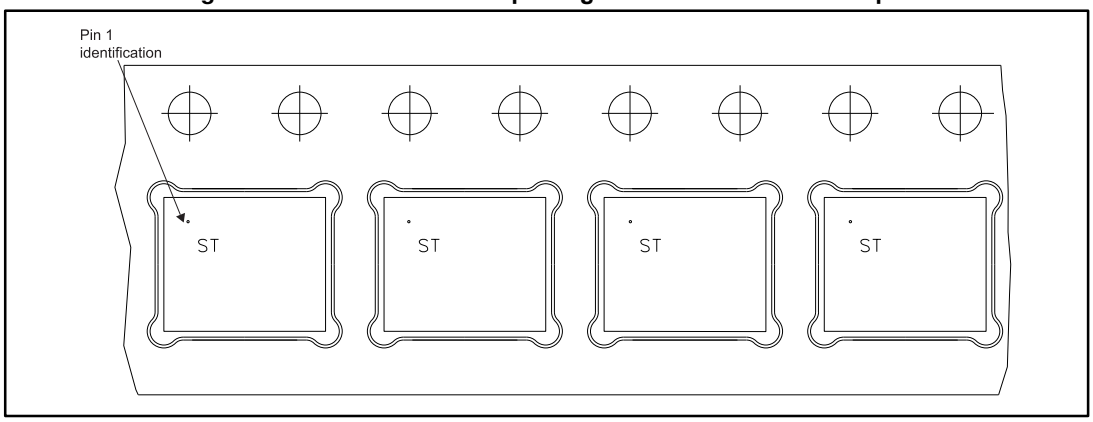
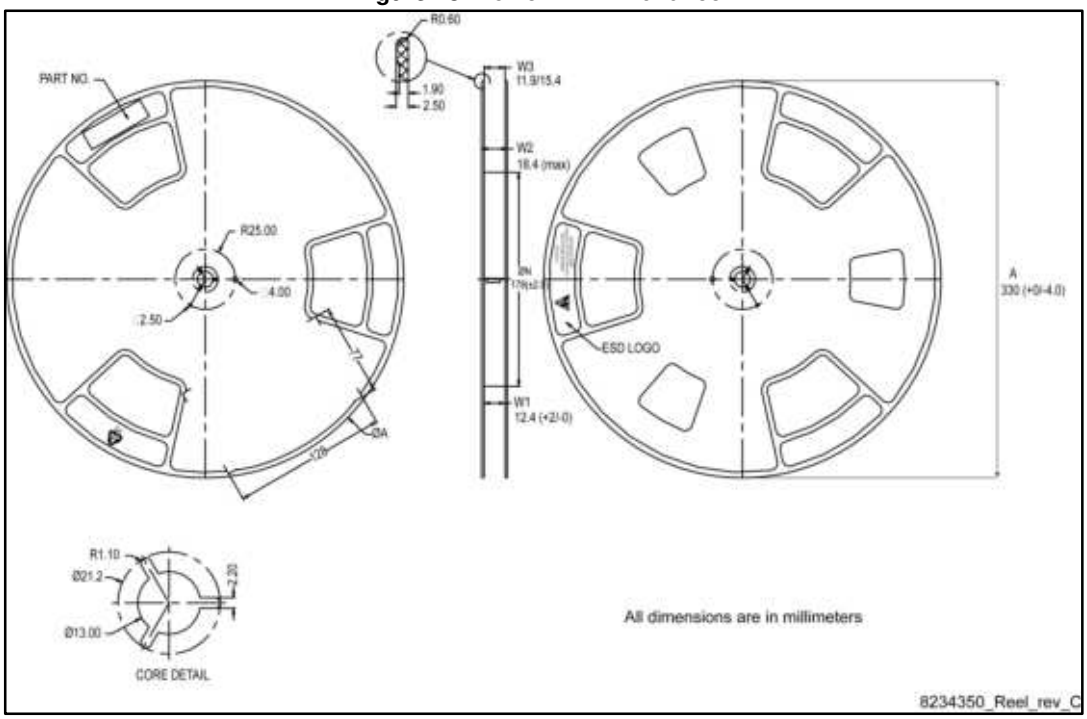


Figure 23: PowerFLAT™ 5x6 reel



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
06-Jul-2015	1	First release.
07-Jan-2016	2	Updated title and features in cover page. Updated *Section 1: "Electrical ratings"*, *Section 2: "Electrical characteristics"* and *Section 4.1: "PowerFLAT™ 5x6 WF type R package information"*.

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