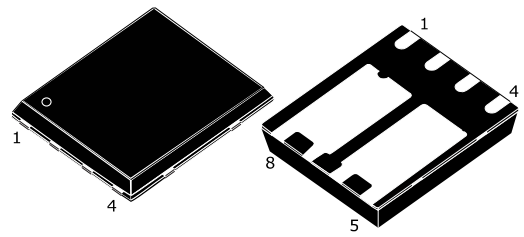
STL50DN6F7

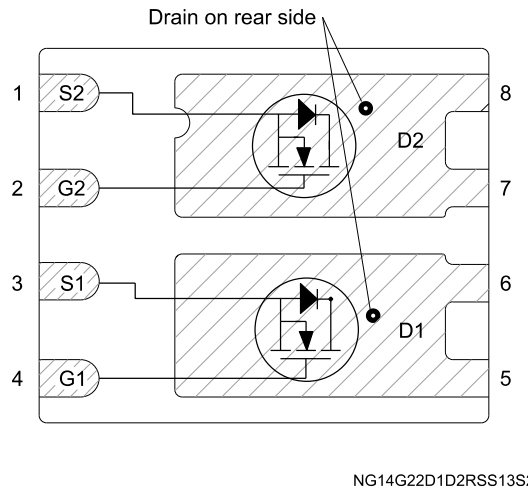
Dual N-channel 60 V, 9 mΩ typ., 57 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 double island package

Datasheet - production data



PowerFLAT™ 5x6 double island

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL50DN6F7	60 V	11 mΩ	57 A

- Among the lowest $R_{DS(on)}$ on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This dual N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL50DN6F7	50DN6F7	PowerFLAT™ 5x6 double island	Tape and reel

This is information on a product in full production. www.st.com

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4.2 PowerFLAT™ 5x6 packing information 12
5 Revision history 14

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate source voltage	±20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	57	A
	Drain current (continuous) at T_C = 100 °C	41	
I_{DM} (1)(2)	Drain current (pulsed)	228	A
I_D (3)	Drain current (continuous) at T_{pcb} = 25 °C	15	A
	Drain current(continuous) at T_{pcb} =100 °C	11	
I_{DM} (2)(3)	Drain current (pulsed)	60	A
P_{TOT}	Total dissipation at T_C = 25 °C	62.5	W
	Total dissipation at T_{pcb} = 25 °C	4.8	
T_J	Operating junction temperature	-55 to 175	°C
T_{stg}	Storage temperature		

Notes:

(1)This value is rated according to $R_{thj\text{-}c}$

(2)Pulse width limited by safe operating area.

(3)This value is rated according to $R_{thj\text{-}pcb}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.4	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	31.3	°C/W

Notes:

(1)When mounted on FR-4 board of 1inc2, 2oz Cu, t < 10 sec

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D= 1 mA	60			V
I_{DSS}	Zero gate voltage drain current	V_{DS}= 60 V,V_{GS}= 0 V			1	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 7.5 A		9	11	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 30V, f = 1 MHz,V_{GS}= 0 V	-	1035	-	pF
C_{oss}	Output capacitance		-	450	-	pF
C_{rss}	Reverse transfer capacitance		-	53	-	pF
Q_g	Total gate charge	V_{DD} = 30 V, I_D = 15 A, V_{GS} = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	17	-	nC
Q_{gs}	Gate-source charge		-	5.7	-	nC
Q_{gd}	Gate-drain charge		-	5.7	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30V, I_D =7.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"*	-	14.5	-	ns
t_r	Rise time		-	15.3	-	ns
$t_{d(off)}$	Turn-off delay time		-	19.4	-	ns
t_f	Fall time		-	8	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 15 A, V_{GS} = 0 V	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 15 A, di/dt = 100 A/µs, V_{DD} = 48 V (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	26.8		ns
Q_{rr}	Reverse recovery charge		-	14.2		nC
I_{RRM}	Reverse recovery current		-	1.06		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics(curve)

Figure 2: Safe operating area

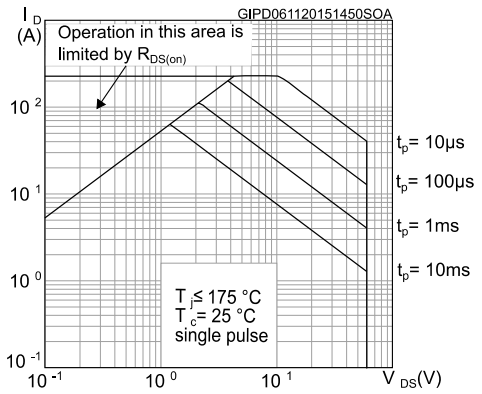


Figure 3: Thermal impedance

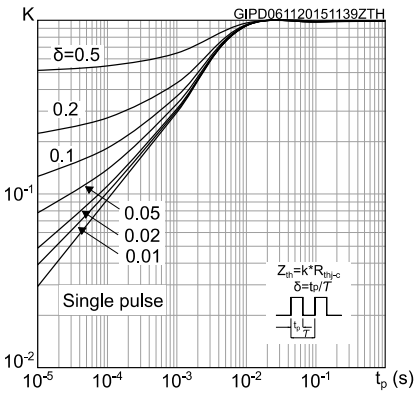


Figure 4: Output characteristics

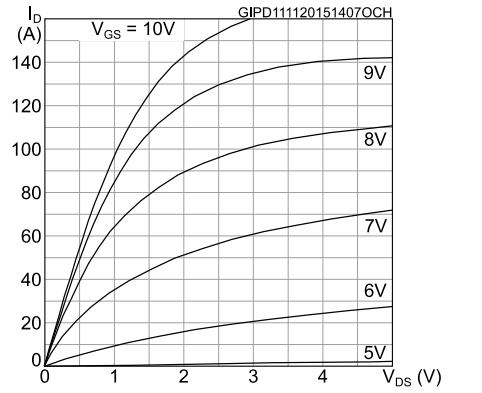


Figure 5: Transfer characteristics

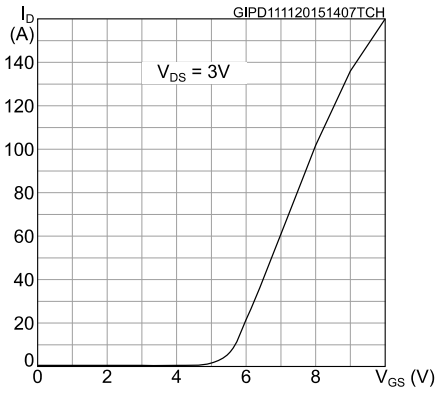


Figure 6: Gate charge vs gate-source voltage

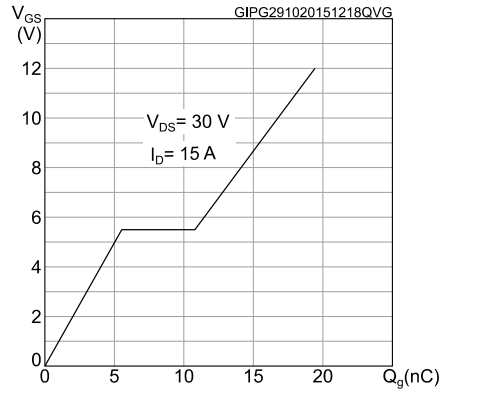


Figure 7: Static drain-source on-resistance

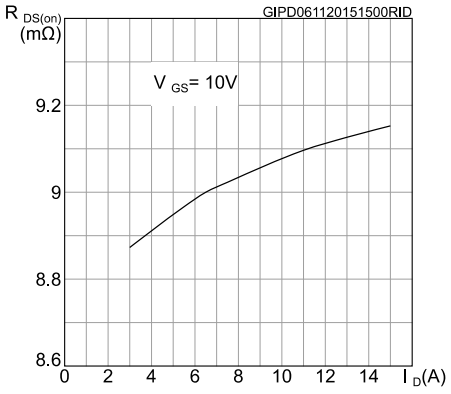


Figure 8: Capacitance variations

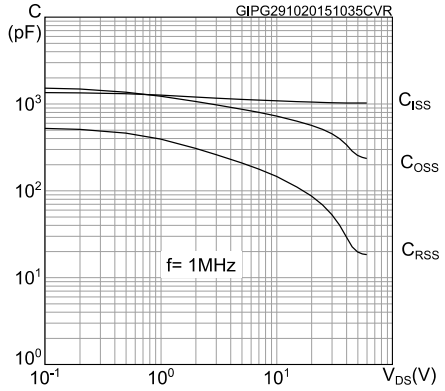


Figure 9: Normalized gate threshold voltage vs temperature

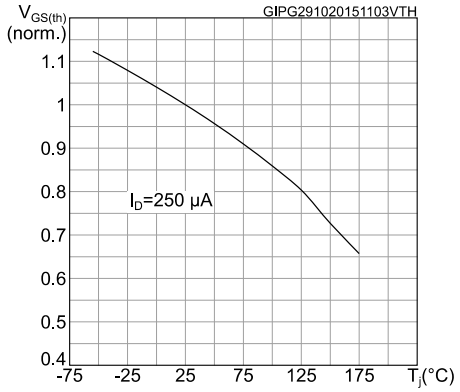


Figure 10: Normalized on-resistance vs temperature

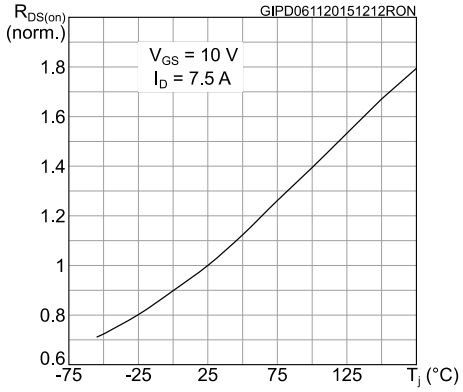


Figure 11: Normalized V(BR)DSS vs temperature

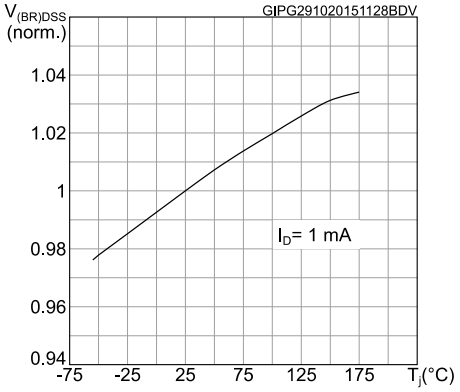
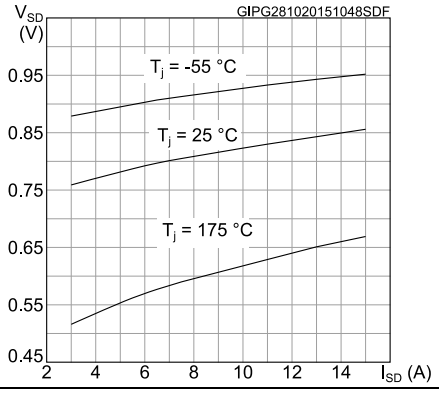


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

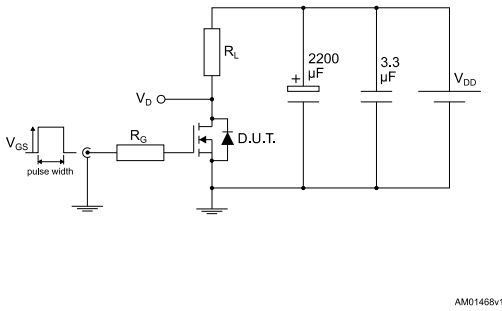


Figure 14: Test circuit for gate charge behavior

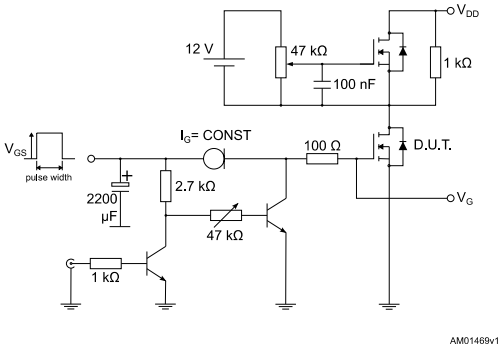


Figure 15: Test circuit for inductive load switching and diode recovery times

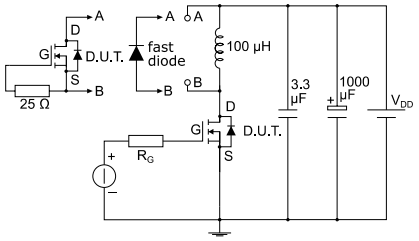


Figure 16: Unclamped inductive load test circuit

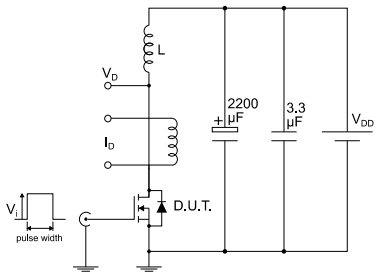


Figure 17: Unclamped inductive waveform

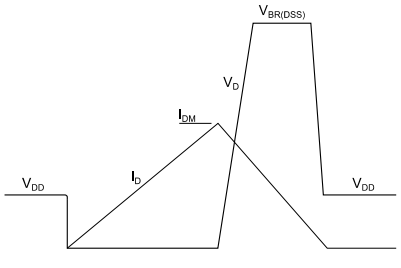
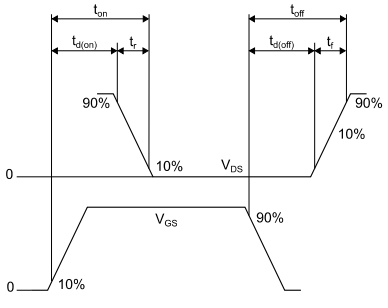


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT 5x6 double island type R package information

Figure 19: PowerFLAT™ 5x6 double island type R package outline

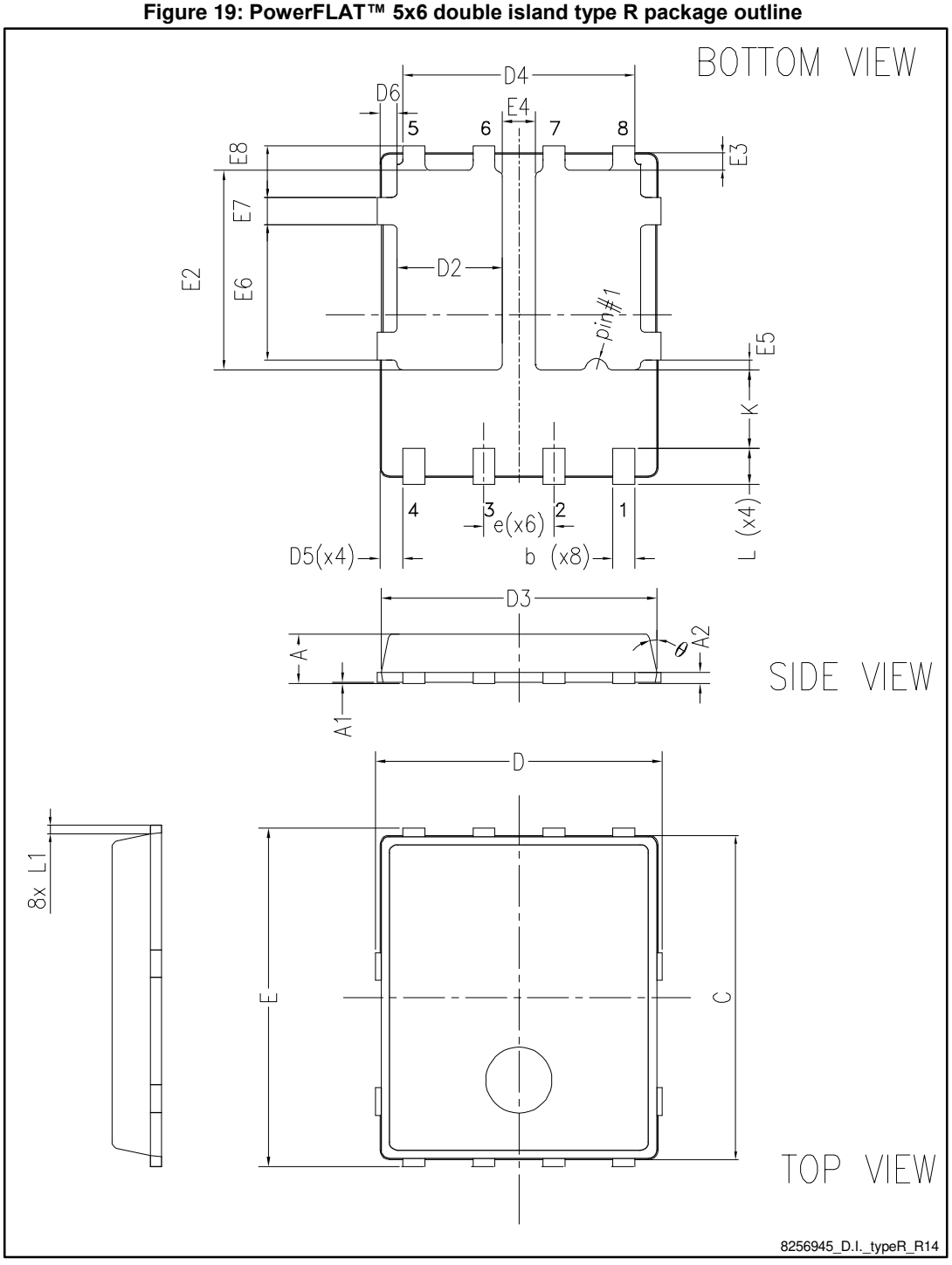
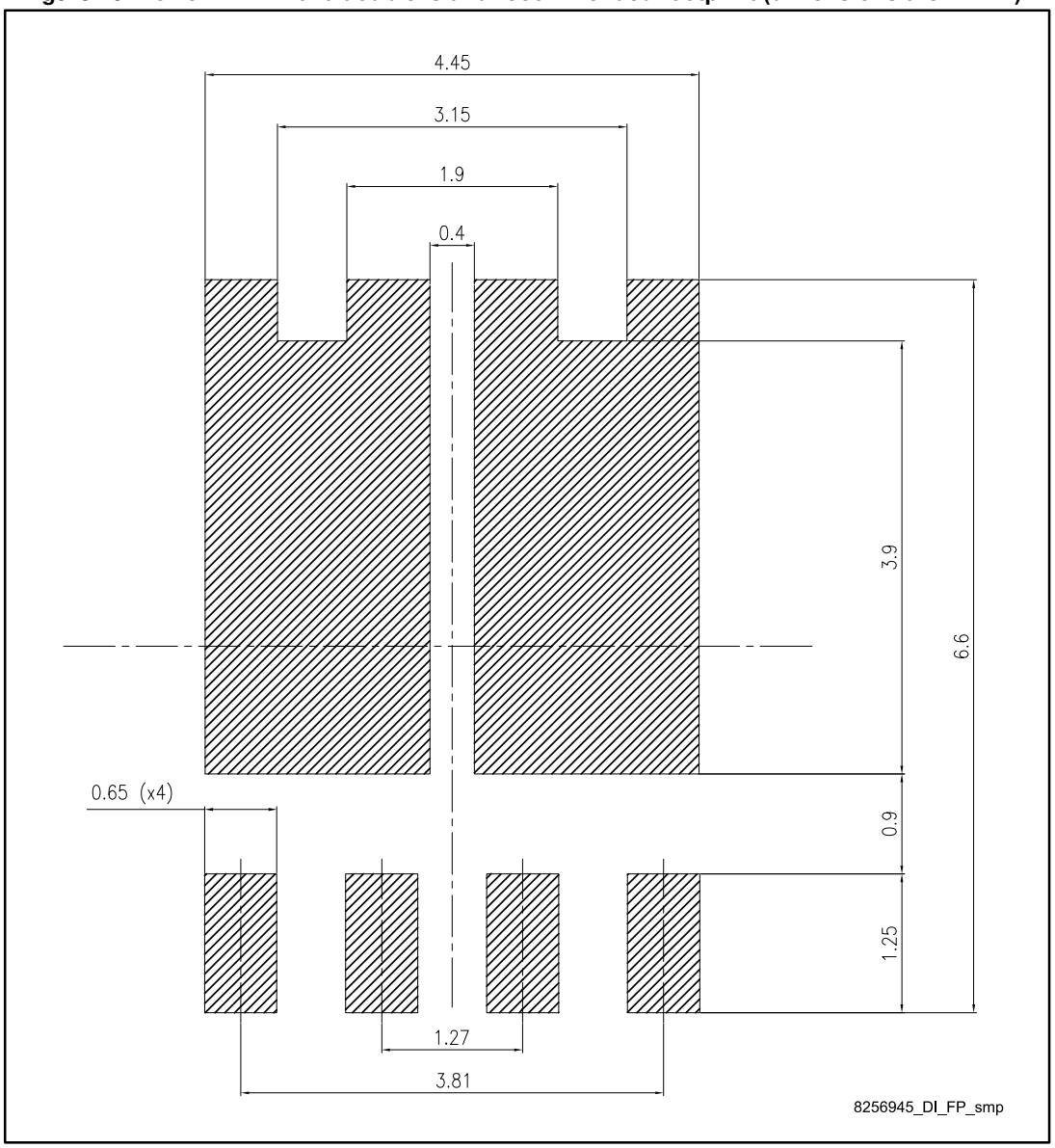


Table 8: PowerFLAT™ 5x6 double island type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	1.68		1.88
D3	4.80	5.00	5.20
D4	4.05	4.20	4.35
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	0.20	0.325	0.45
E4	0.55		0.75
E5	0.08		0.28
E6	2.35		2.55
E7	0.40		0.60
E8	0.75	0.90	1.05
L	0.60		0.80
L1	0.05	0.15	0.25
K	1.275		1.575
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 double island recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 packing information

Figure 21: PowerFLAT™ 5x6 tape (dimensions are in mm)

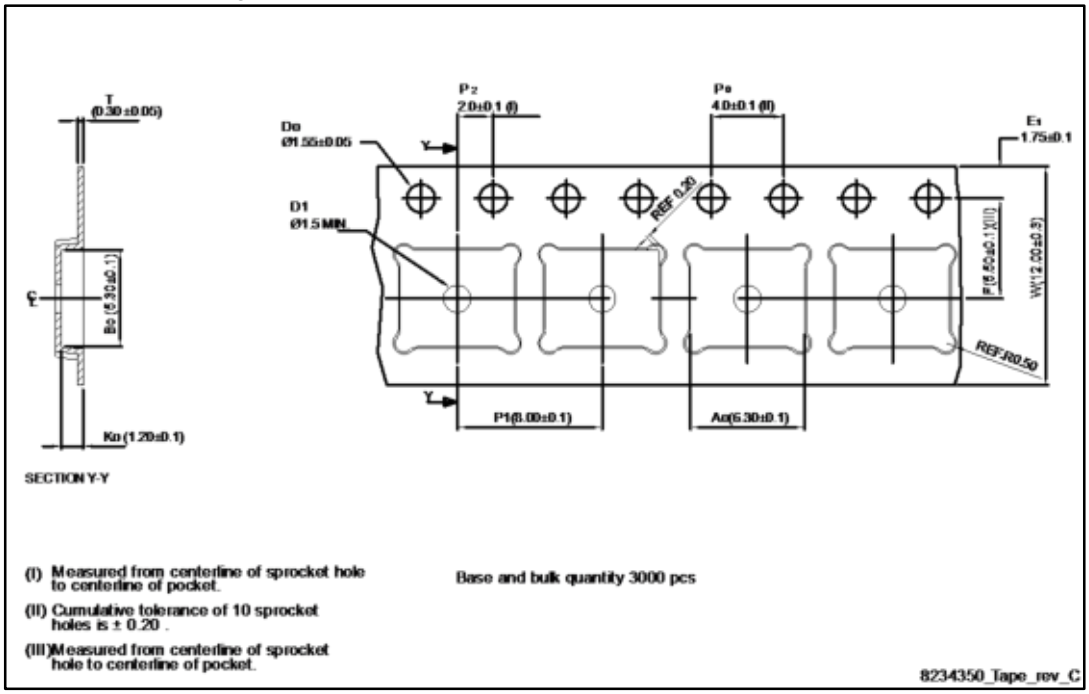


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

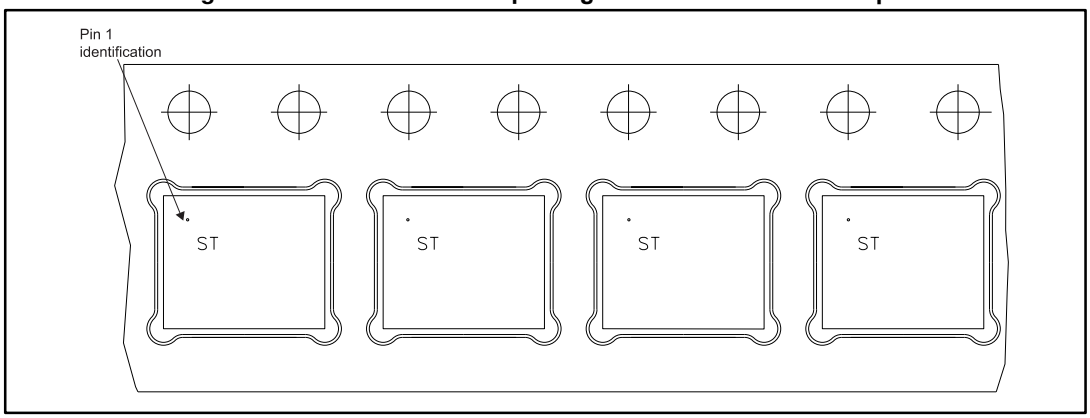
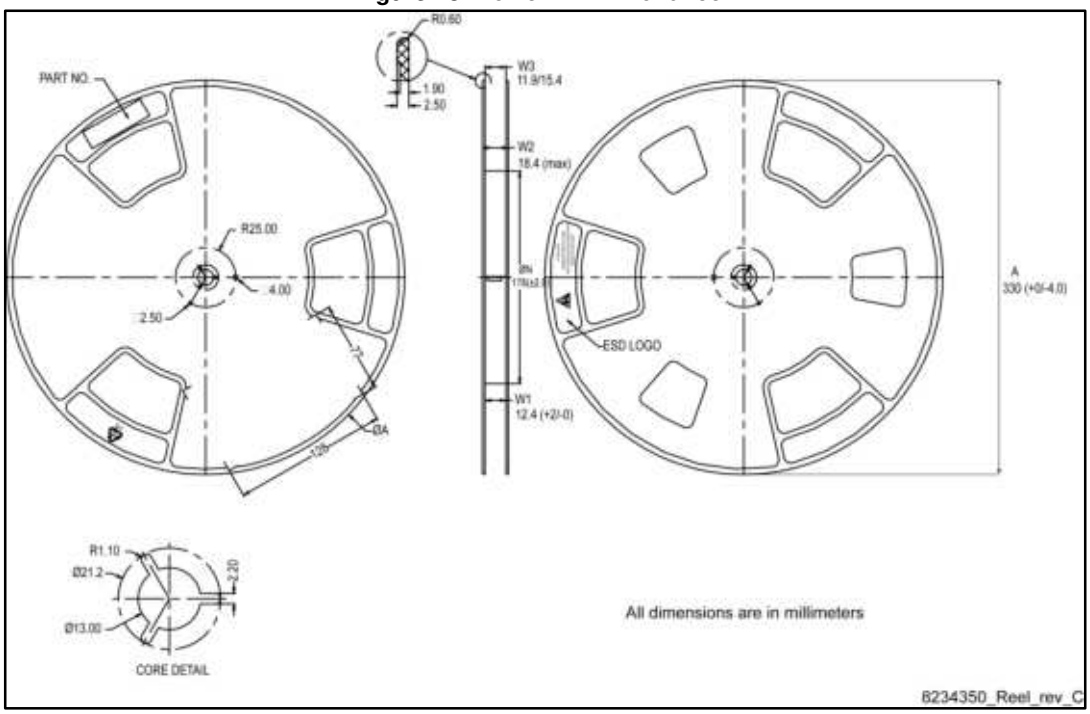


Figure 23: PowerFLAT™ 5x6 reel



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
17-Jul-2015	1	First release.
13-Nov-2015	2	Document status promoted from preliminary to production data. Updated title and features in cover page. Updated *Table 2: "Absolute maximum ratings"* and *Section 4: "Electrical characteristics"*. Added *Section 4.1: "Electrical characteristics(curve)"* Minor text changes.

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