M24C32M-FCU

32-Kbit serial I²C bus EEPROM 4 balls CSP

Datasheet - preliminary data



WLCSP (CU)

Features

- Compatible with all I²C bus modes::
  - 1 MHz
  - 400 kHz
  - 100 kHz
- Memory array:
  - 32 Kbit (4 Kbyte) of EEPROM
  - Page size: 32 byte
- Specific device code
- Supply voltage range:
  - 1.7 V to 5.5V over -40°C / +85°C
- Write
  - Byte Write within 5 ms
  - Page Write within 5 ms
- Random and sequential Read modes
- Enhanced ESD/Latch-Up protection
- More than 4 million Write cycles
- More than 200-years data retention
- Package
  - WLCSP (ECOPACK2®)

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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Contents

1 **Description** 6

2 **Signal description** 8

2.1 Serial Clock (SCL) 8

2.2 Serial Data (SDA) 8

2.3 V_{SS} (ground) 8

2.4 Supply voltage (V_{CC}) 8

2.4.1 Operating supply voltage (V_{CC}) 8

2.4.2 Power-up conditions 8

2.4.3 Device reset 8

2.4.4 Power-down conditions 9

3 **Memory organization** 10

4 **Device operation** 11

4.1 Start condition 12

4.2 Stop condition 12

4.3 Data input 12

4.4 Acknowledge bit (ACK) 12

4.5 Device addressing 13

5 **Instructions** 14

5.1 Write operations 14

5.1.1 Byte Write 15

5.1.2 Page Write 16

5.1.3 Minimizing Write delays by polling on ACK 17

5.2 Read operations 18

5.2.1 Random Address Read 18

5.2.2 Current Address Read 19

5.2.3 Sequential Read 19

6 **Initial delivery state** 20

7 **Maximum rating** 21

8 DC and AC parameters 22

9 Package information 30

9.1 Ultra Thin WLCSP package information 30

10 Part numbering 32

11 Revision history 34

List of tables

Table 1. Signal names . . . 6
Table 2. Signals vs. bump position . . . 7
Table 3. Device select code . . . 13
Table 4. Most significant address byte . . . 14
Table 5. Least significant address byte . . . 14
Table 6. Absolute maximum ratings . . . 21
Table 7. Operating conditions (voltage range F) . . . 22
Table 8. AC measurement conditions . . . 22
Table 9. Input parameters . . . 22
Table 10. Cycling performance . . . 23
Table 11. Memory cell data retention . . . 23
Table 12. DC characteristics (1.7 V to 2.5 V) . . . 24
Table 13. DC characteristics (2.5 V to 5.5 V) . . . 25
Table 14. 400 kHz AC characteristics . . . 26
Table 15. 1 MHz AC characteristics . . . 27
Table 16. Ultra Thin WLCSP- 4-bump, 0.795 x 0.674 mm, wafer level chip scale package mechanical data . . . 31
Table 17. Ordering information scheme . . . 32
Table 18. Document revision history . . . 34

List of figures

Figure 1. Logic diagram . . . 6
Figure 2. 4-bump WLCSP connections (top view, marking side, with balls on the underside) . . . 7
Figure 3. Block diagram . . . 10
Figure 4. I^2C bus protocol . . . 11
Figure 5. Write mode sequence . . . 15
Figure 6. Write mode sequence . . . 16
Figure 7. Write cycle polling flowchart using ACK . . . 17
Figure 8. Read mode sequences . . . 18
Figure 9. AC measurement I/O waveform . . . 22
Figure 10. Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus at maximum frequency f_C = 400 kHz . . . 28
Figure 11. Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus at fC = 1MHz . . . 28
Figure 12. AC waveforms . . . 29
Figure 13. Ultra Thin WLCSP- 4-bump, 0.795 x 0.674 mm, wafer level chip scale package outline . . . 30
Figure 14. Thin WLCSP- 4-bump, 0.795 x 0.674 mm, wafer level chip scale package recommended footprint . . . 31

1 Description

The M24C32M-FCU is a 32-Kbit I2C-compatible EEPROM (Electrically Erasable PROgrammable Memory)organized as 4 K × 8 bits.The M24C32M can be hooked on the same bus as the standard M24C32 in WLCSP 4 bump, thanks to specific device select code. See *Section 4.5: Device addressing*.

The M24C32M-FCU can operate with a supply voltage from 1.7 V to 5.5 V, over an ambient temperature range of -40 °C/+85 °C.

The M24C32M-FCU is delivered in a 4-ball WLCSP package.

Figure 1. Logic diagram

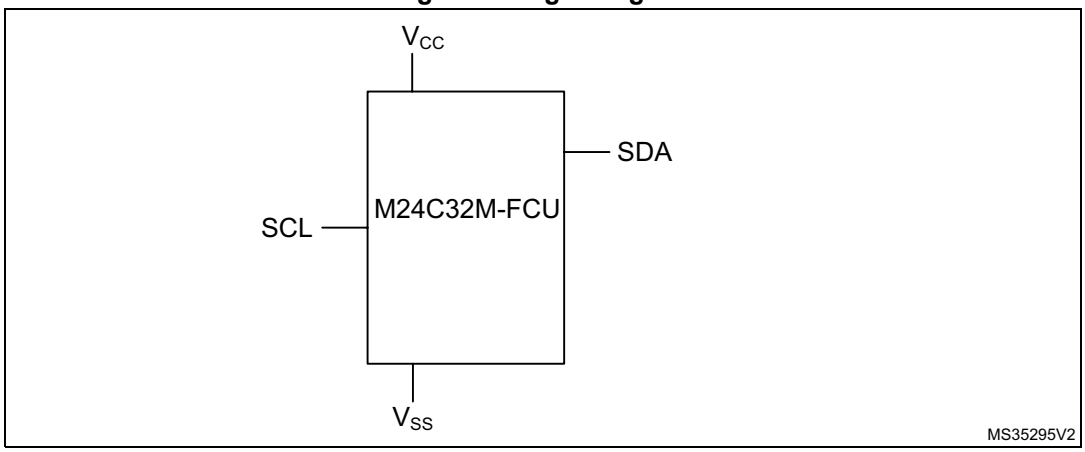


Table 1. Signal names

Signal name	Function	Direction
SDA	Serial Data	I/O
SCL	Serial Clock	Input
V_{CC}	Supply voltage	-
V_{SS}	Ground	-

Figure 2. 4-bump WLCSP connections
(top view, marking side, with balls on the underside)

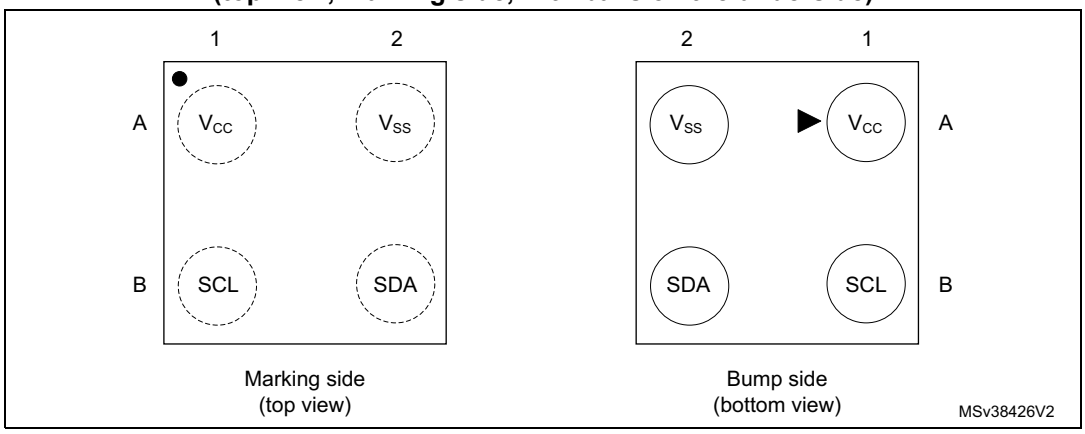


Table 2. Signals vs. bump position

Position	A	B
1	V_{CC}	SCL
2	V_{SS}	SDA

2 Signal description

2.1 Serial Clock (SCL)

SCL is an input. The signal applied on the SCL input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

2.2 Serial Data (SDA)

SDA is an input/output used to transfer data in or data out of the device. SDA(out) is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from Serial Data (SDA) to V_{CC} (*Figure 10* indicates how to calculate the value of the pull-up resistor).

2.3 V_{SS} (ground)

V_{SS} is the reference for the V_{CC} supply voltage.

2.4 Supply voltage (V_{CC})

2.4.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Operating conditions in *Section 8: DC and AC parameters)*. In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually from10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W).

2.4.2 Power-up conditions

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage (see Operating conditions in *Section 8: DC and AC parameters)*.

2.4.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} has reached the internal reset threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see Operating conditions in *Section 8: DC and AC parameters*). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode; however, the device must not be accessed until V_{CC} reaches a valid and stable DC voltage within the specified [V_{CC}(min), V_{CC}(max)] range (see Operating conditions in *Section 8: DC and AC parameters*).

In a similar way, during power-down (continuous decrease in V_{CC}), the device must not be accessed when V_{CC} drops below V_{CC}(min). When V_{CC} drops below the power-on-reset threshold voltage, the device stops responding to any instruction sent to it.

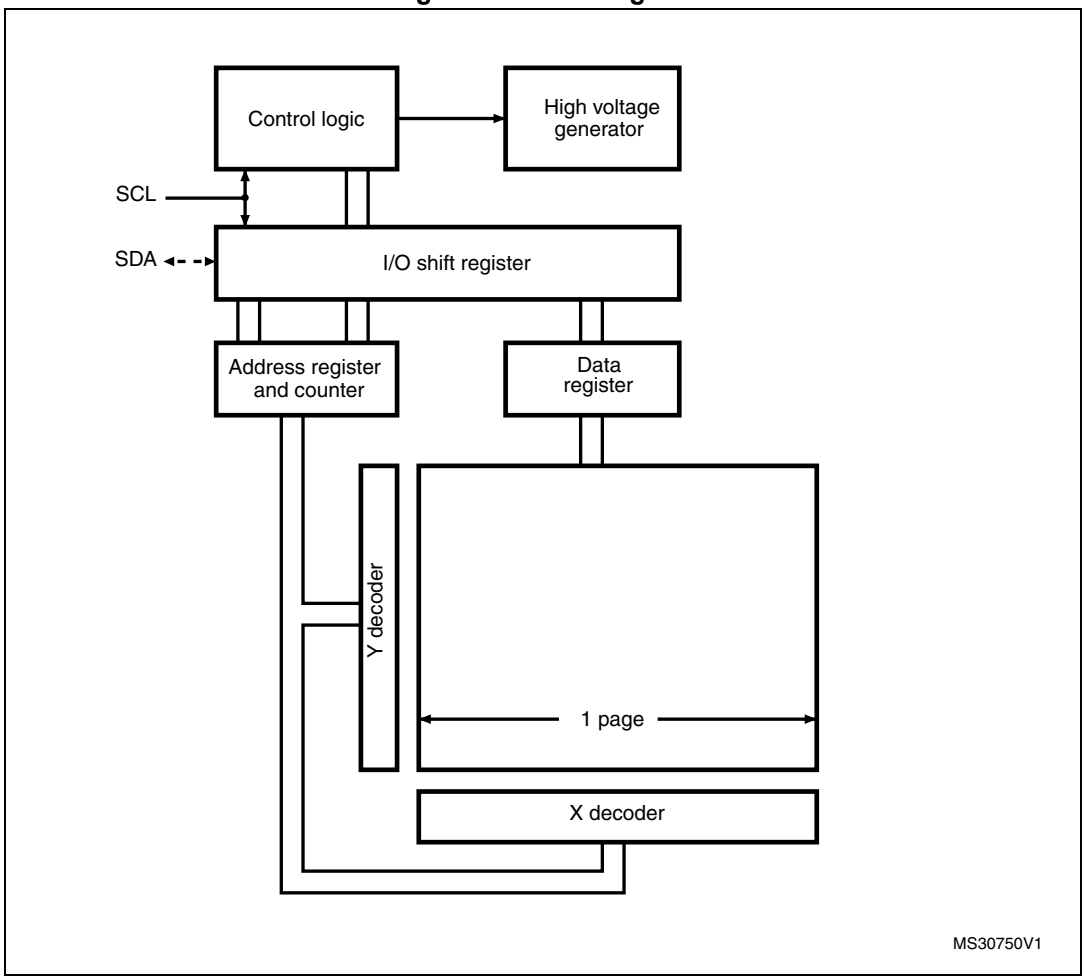
2.4.4 Power-down conditions

During power-down (continuous decrease in V_{CC}), the device must be in the Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

3 Memory organization

The memory is organized as shown below.

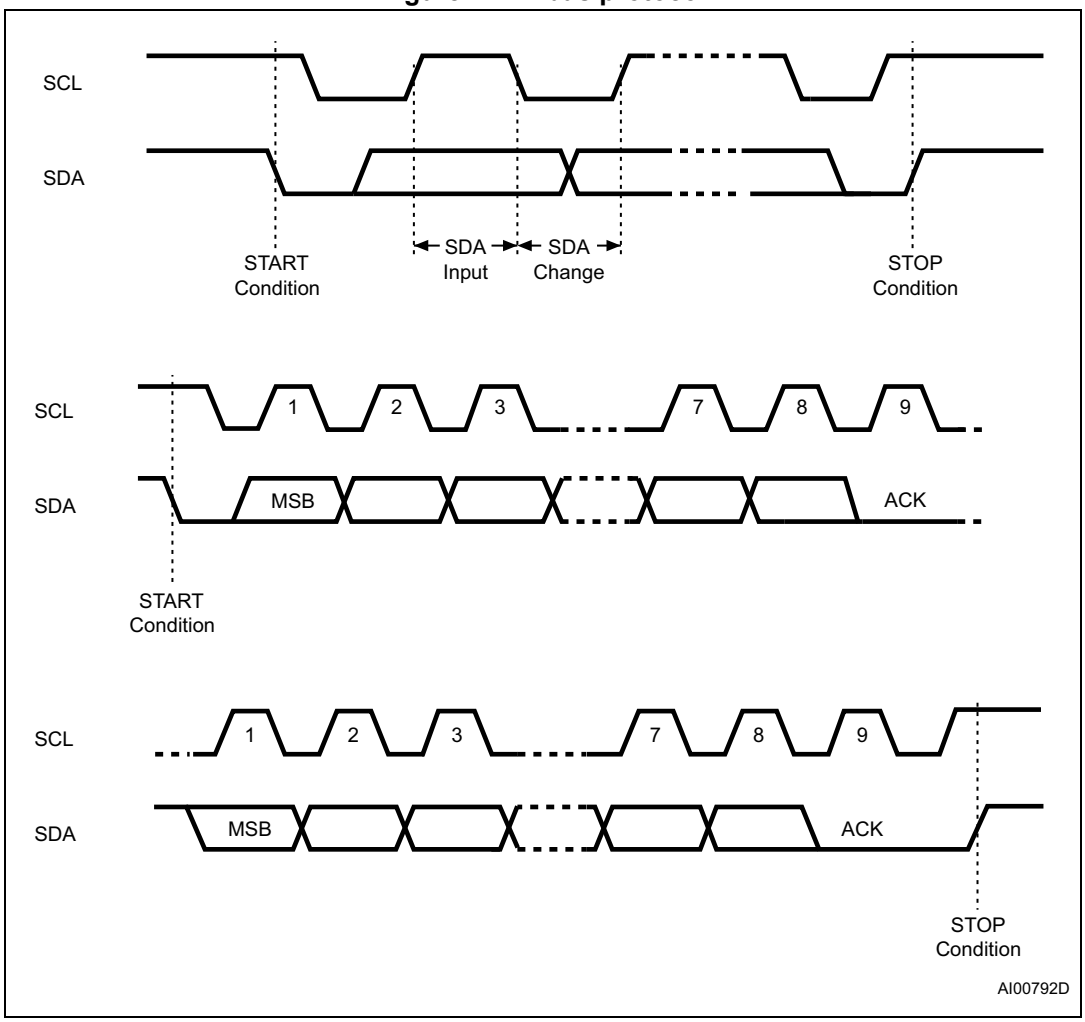
Figure 3. Block diagram



4 Device operation

The device supports the I^2C protocol. This is summarized in *Figure 4*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

Figure 4. I^2C bus protocol



4.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer instruction. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

4.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read instruction that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode.

A Stop condition at the end of a Write instruction triggers the internal Write cycle.

4.3 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

4.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

4.5 Device addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 3* (on Serial Data (SDA), most significant bit first).

Table 3. Device select code

	Device type identifier(1)				Chip Enable address			$\overline{RW}$
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code when addressing the memory array	1	0	1	0	1	0	0	$\overline{RW}$

1. The most significant bit, b7, is sent first.

The 8th bit is the Read/$\overline{Write}$ bit ($\overline{RW}$). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time.

If the device does not match the device select code, the device deselects itself from the bus, and goes into Standby mode (therefore will not acknowledge the device select code).

5 Instructions

5.1 Write operations

Following a Start condition the bus master sends a device select code with the R/$\overline{W}$ bit (R$\overline{W}$) reset to 0. The device acknowledges this, as shown in *Figure 5*, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

Table 4. Most significant address byte

A15	A14	A13	A12	A11	A10	A9	A8

Table 5. Least significant address byte

A7	A6	A5	A4	A3	A2	A1	A0

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the “10th bit” time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle t_W is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

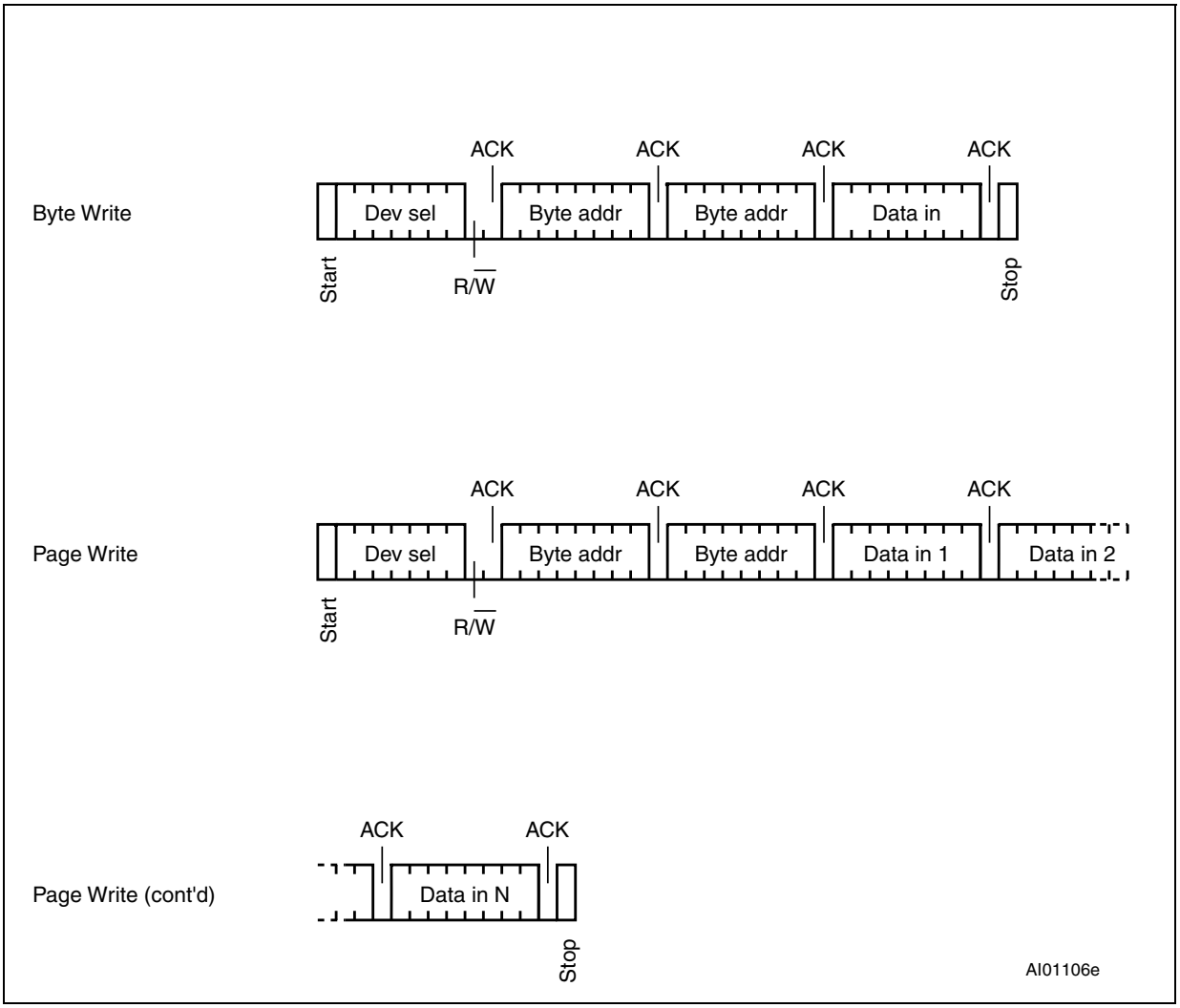
After the Stop condition and the successful completion of an internal Write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

5.1.1 Byte Write

After the device select code and the address bytes, the bus master sends one data byte. The device replies with Ack, as shown in *Figure 5*. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 5*.

Figure 5. Write mode sequence



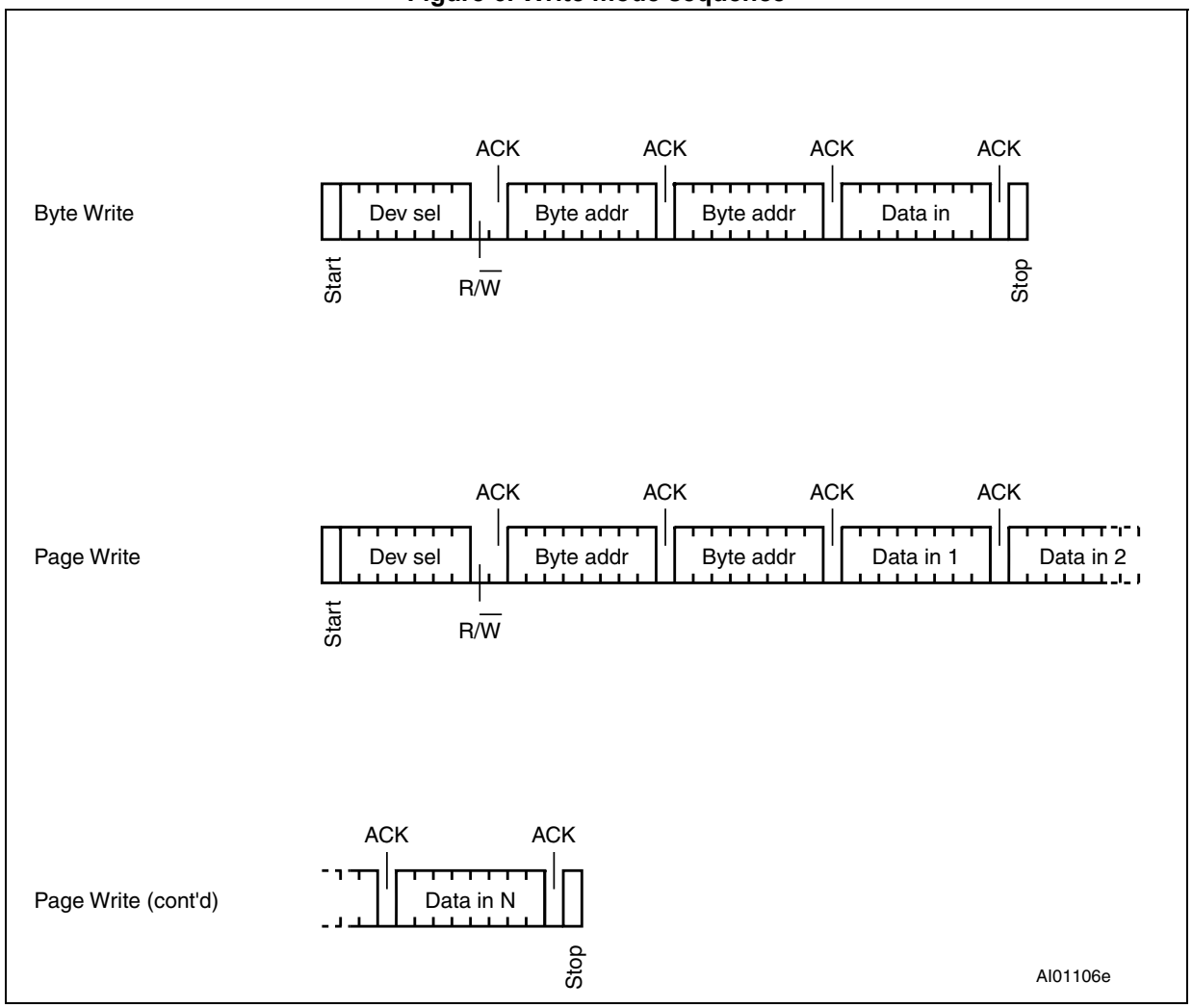
5.1.2 Page Write

The Page Write mode allows up to 32 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits, A15/A5, are the same. If more bytes are sent than will fit up to the end of the page, a “roll-over” occurs, i.e. the bytes exceeding the page end are written on the same page, from location 0.

The bus master sends from 1 to 32 bytes of data, each of which is acknowledged by the device. After each transferred byte, the internal page address counter is incremented.

The transfer is terminated by the bus master generating a Stop condition.

Figure 6. Write mode sequence



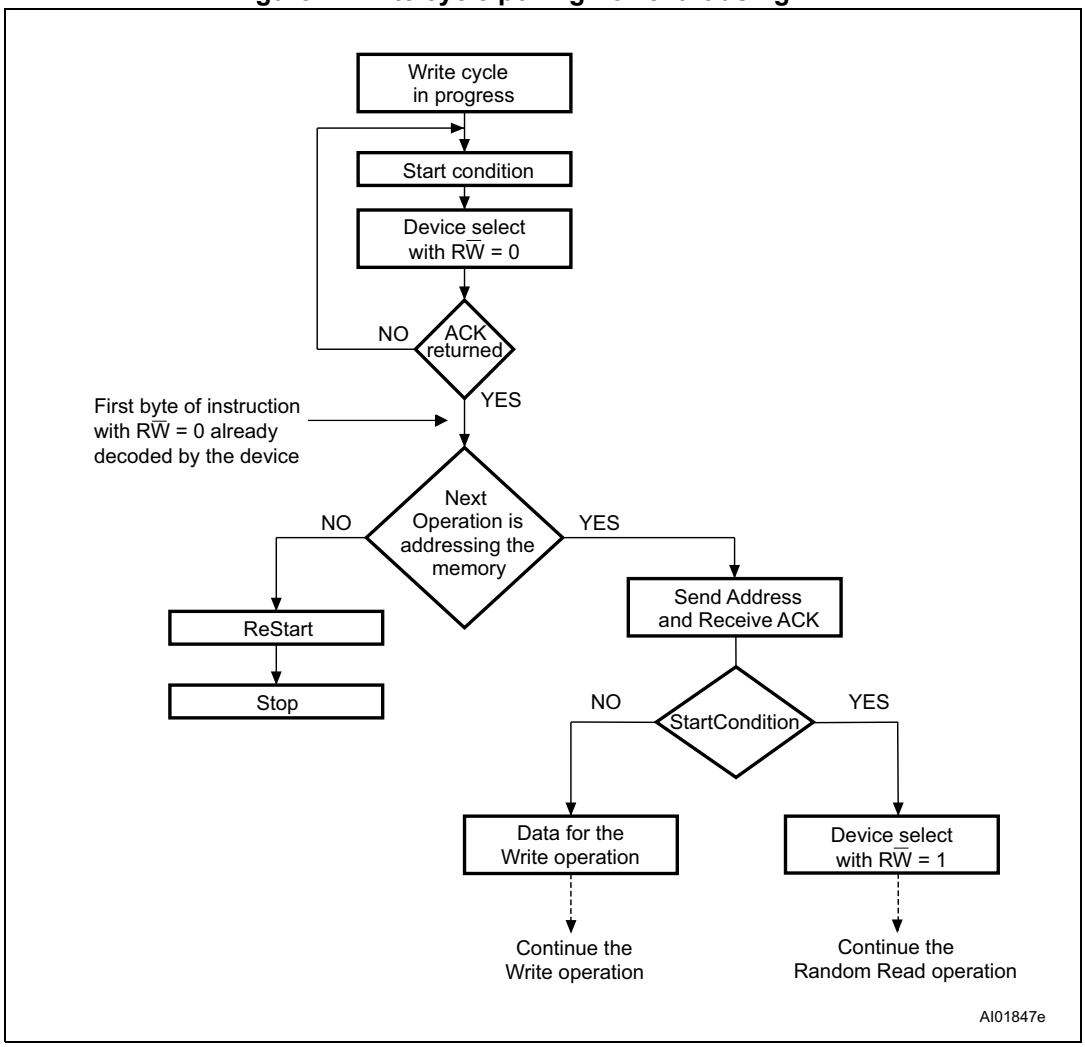
5.1.3 Minimizing Write delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_w) is shown in AC characteristics tables in *Section 8: DC and AC parameters*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 7*, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 7. Write cycle polling flowchart using ACK



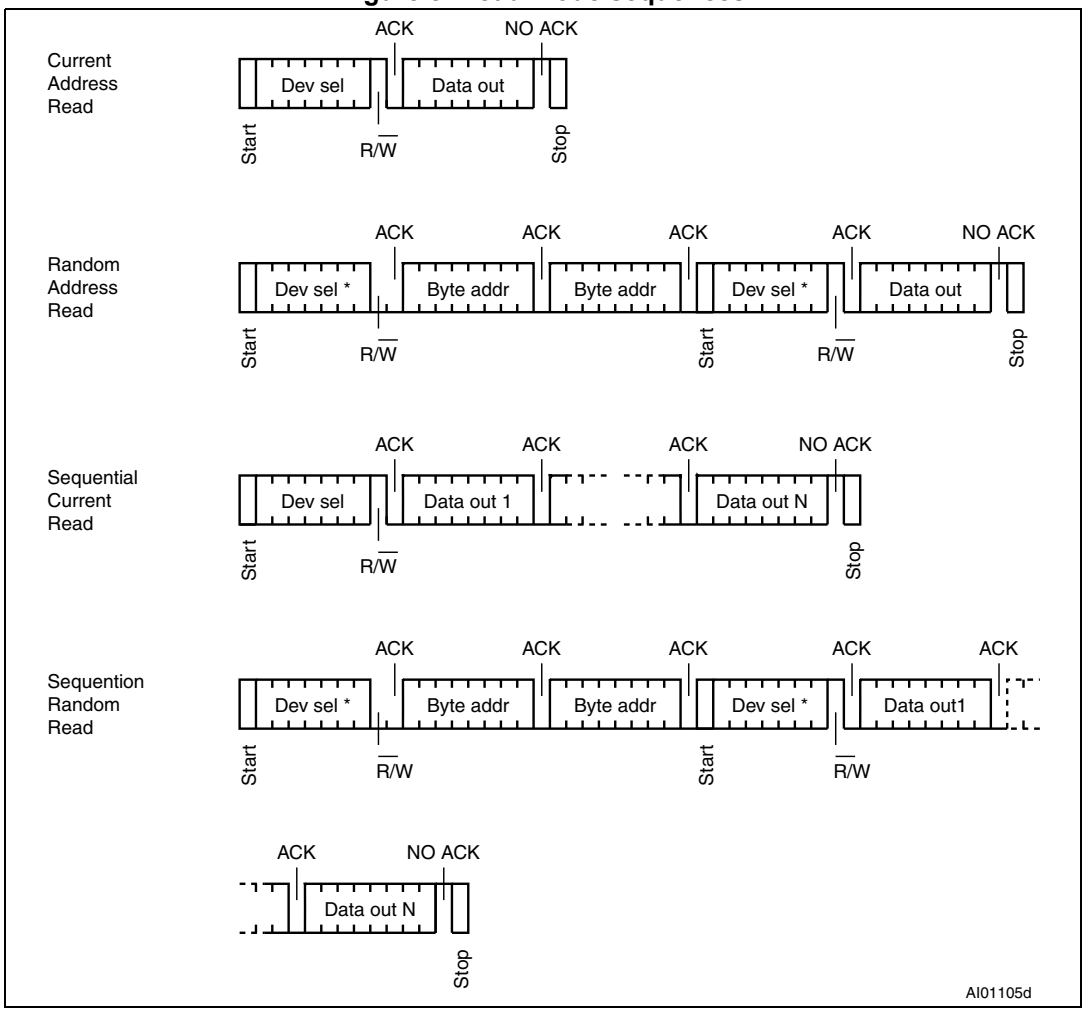
1. The seven most significant bits of the Device Select code of a Random Read (bottom right box in the figure) must be identical to the seven most significant bits of the Device Select code of the Write (polling instruction in the figure).

5.2 Read operations

After the successful completion of a Read operation, the device internal address counter is incremented by one, to point to the next byte address.

For the Read instructions, after each byte read (data out), the device waits for an acknowledgment (data in) during the 9th bit time. If the bus master does not acknowledge during this 9th time, the device terminates the data transfer and switches to its Standby mode.

Figure 8. Read mode sequences



5.2.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 8*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the RW bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

5.2.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the R/$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 8*, *without* acknowledging the byte.

Note that the address counter value is defined by instruction accessing the memory. When accessing the memory, it is safer to always use the Random Address Read instruction (this instruction loads the address counter with the byte location to read in the memory, see *Section 5.2.1*) instead of the Current Address Read instruction.

5.2.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 8*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter “rolls-over”, and the device continues to output data from memory address 00h.

6 Initial delivery state

The device is delivered with all the memory array bits set to 1 (each byte contains FFh) .

7 Maximum rating

Stressing the device outside the ratings listed in *Table 6* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
-	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note(1)		°C
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{IO}	Input or output range	–0.50	6.5	V
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic pulse (Human Body model)(2)	-	3000	V

1. Compliant with JEDEC standard J-STD-020D (for small-body, Sn-Pb or Pb free assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS directive 2011/65/EU of July 2011).
2. Positive and negative pulses applied on different combinations of pin connections, according to AEC-Q100-002 (compliant with AANSI/ESDA/JEDEC JS-001-2012, C1=100 pF, R1=1500 Ω).

8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 7. Operating conditions (voltage range F)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	5.5	V
T_A	Ambient operating temperature	-40	85	°C
f_C	Operating clock frequency	-	1	MHz

Table 8. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	100		pF
-	SCL input rise/fall time, SDA input fall time	-	50	ns
-	Input levels	0.2 V_{CC} to 0.8 V_{CC}		V
-	Input and output timing reference levels	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 9. AC measurement I/O waveform

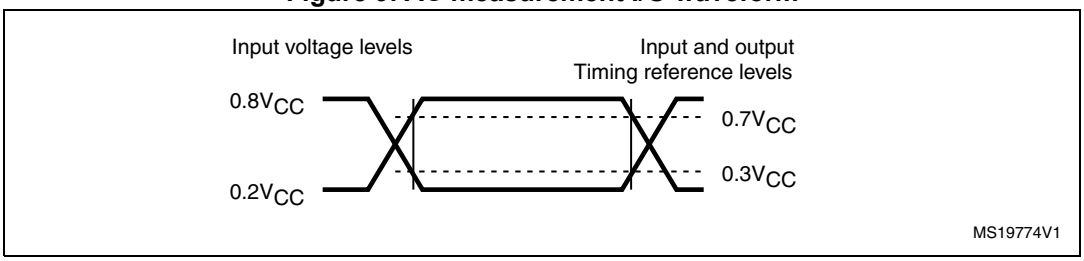


Table 9. Input parameters

Symbol	Parameter (1)	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)	-	-	8	pF
C_{IN}	Input capacitance (other pins)	-	-	6	pF

1. Characterized only, not tested in production.

Table 10. Cycling performance

Symbol	Parameter	Test condition	Max.	Unit
Ncycle	Write cycle endurance(1)	$T_A \leq 25$ °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	4,000,000	Write cycles(2)
		$T_A = 85$°C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	1.200.000	

1. The Write cycle endurance is defined by characterization and qualification.
2. A Write cycle is executed when either a Page Write or a Byte write instruction is decoded

Table 11. Memory cell data retention

Parameter	Test condition	Min.	Unit
Data retention(1)	T_A = 55 °C	200	Years

1. The data retention behavior is checked in production, while the data retention limit defined in this table is extracted from characterization and qualification results.

Table 12. DC characteristics (1.7 V to 2.5 V)

Symbol	Parameter	Test conditions(1) (in addition to those in *Table 7*)	Min	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC}, device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.7 V, f_C = 400 kHz	-	0.8	mA
		f_C = 1 MHz	-	2.5	
I_{CC0}	Supply current (Write)	During t_W, V_{CC} < 2.5 V	-	3(2)	mA
I_{CC1}	Standby supply current	Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.7 V	-	1	µA
V_{IL}	Input low voltage (SCL, SDA)	V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	V_{CC} < 2.5 V	0.7 V_{CC}	6.5	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.7 V	-	0.2	V

1. If the application operates with 2.5 V < VCC < 5.5 V and -40 °C < TA < +85 °C, please refer to *Table 13* instead of this *Table 12*.
2. Characterized only, not 100% tested.
3. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).

Table 13. DC characteristics (2.5 V to 5.5 V)

Symbol	Parameter	Test conditions (in addition to *Table 7*)	Min	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC}, device in Standby mode	-	± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 2	µA
I_{CC}	Supply current (Read)	2.5 V < V_{CC} < 5.5 V, f_C = 400 kHz (rise/fall time < 50 ns)	-	2	mA
		2.5 V < V_{CC} < 5.5 V, f_C = 1 MHz (rise/fall time < 50 ns)	-	2.5	
I_{CC0}	Supply current (Write)	During t_W	-	5(1)	mA
I_{CC1}	Standby supply current	Device not selected(2), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V	-	2	µA
		Device not selected(2), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5.5 V	-	3	
V_{IL}	Input low voltage (SCL, SDA)	-	–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	-	0.7 V_{CC}	6.5	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V or I_{OL} = 3 mA, V_{CC} = 5.5 V	-	0.4	V

1. Characterized only, not 100% tested.
2. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).

Table 14. 400 kHz AC characteristics

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	ns
t_{QL1QL2}(1)	t_F	SDA (out) fall time	20(2)	300	ns
t_{XH1XH2}	t_R	Input signal rise time	(3)	(3)	ns
t_{XL1XL2}	t_F	Input signal fall time	(3)	(3)	ns
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	100	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX} (4)	t_{DH}	Data out hold time	100	-	ns
t_{CLQV} (5)	t_{AA}	Clock low to next data valid (access time)	-	900	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	ns
t_W	t_{WR}	Write time	-	5	ms
t_{NS}(1)	-	Pulse width ignored (input filter on SCL and SDA) - single glitch	-	80	ns

1. Characterized only, not tested in production.
2. With C_L = 10 pF.
3. There is no min. or max. value for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when f_C < 400 kHz.
4. The min value for t_{CLQX} (Data out hold time) offers a safe timing to bridge the undefined region of the falling edge SCL.
5. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either $0.3V_{CC}$ or $0.7V_{CC}$, assuming that $R_{bus} \times C_{bus}$ time constant is less than 400 ns.

Table 15. 1 MHz AC characteristics

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	0	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	260	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	500	-	ns
t_{XH1XH2}	t_R	Input signal rise time	(1)	(1)	ns
t_{XL1XL2}	t_F	Input signal fall time	(1)	(1)	ns
t_{QL1QL2} (2)	t_F	SDA (out) fall time	20(3)	120	ns
t_{DXCH}	$t_{SU:DAT}$	Data in setup time	50	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX} (4)	t_{DH}	Data out hold time	100	-	ns
t_{CLQV} (5)	t_{AA}	Clock low to next data valid (access time)	-	450	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	250	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	250	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	ns
t_W	t_{WR}	Write time	-	5	ms
t_{NS} (2)	-	Pulse width ignored (input filter on SCL and SDA)	-	80	ns

1. There is no min. or max. values for the input signal rise and fall times. However, it is recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 120 ns when f_C < 1 MHz.
2. Characterized only, not tested in production.
3. With CL = 10 pF.
4. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
5. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that the Rbus × Cbus time constant is within the values specified in *Figure 10*.

Figure 10. Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus at maximum frequency f_C = 400 kHz

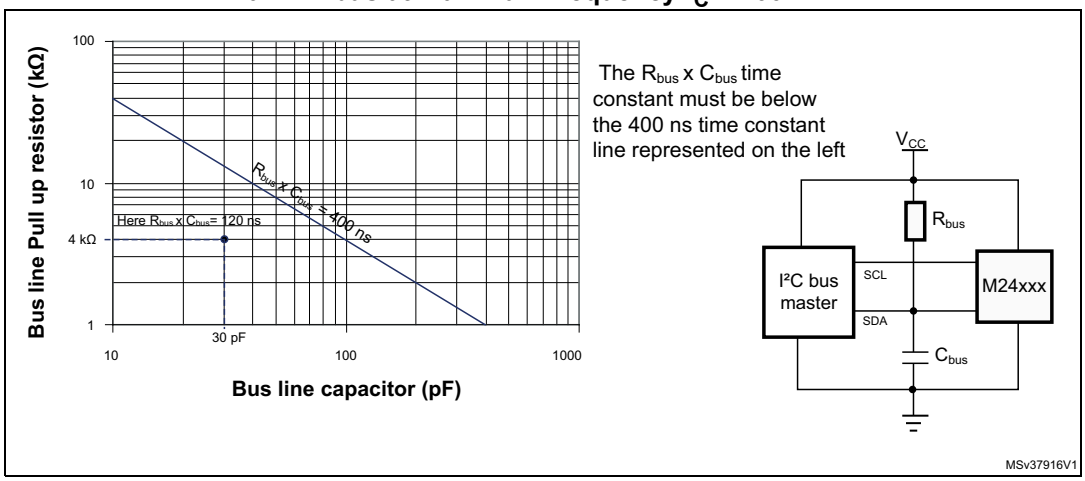


Figure 11. Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus at f_C = 1MHz

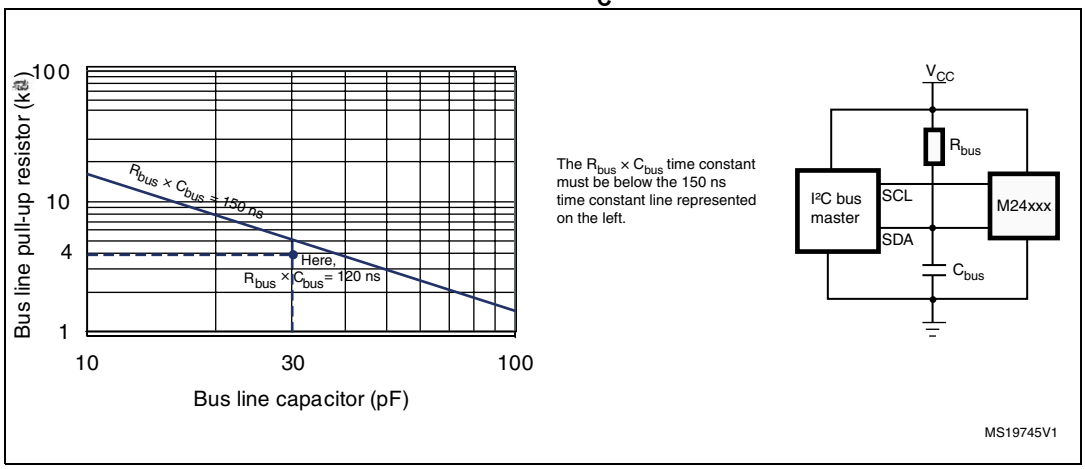
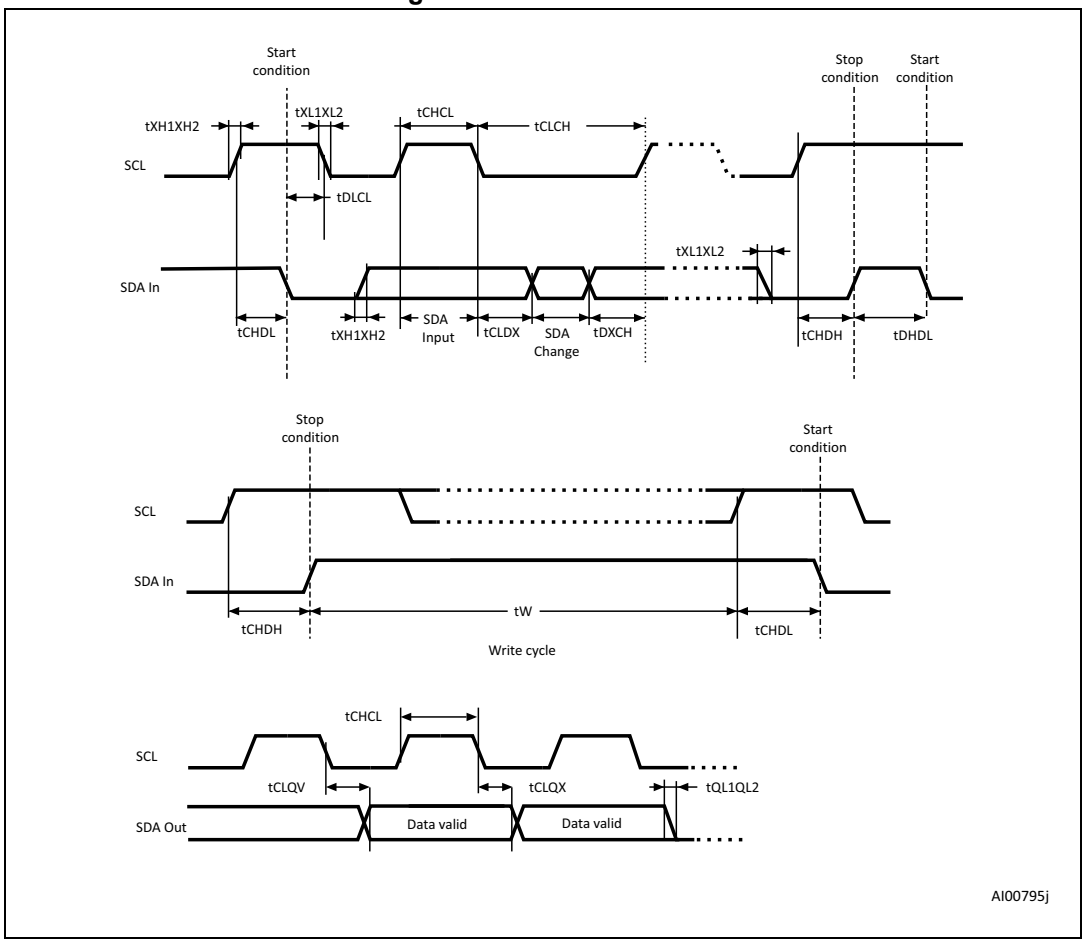


Figure 12. AC waveforms

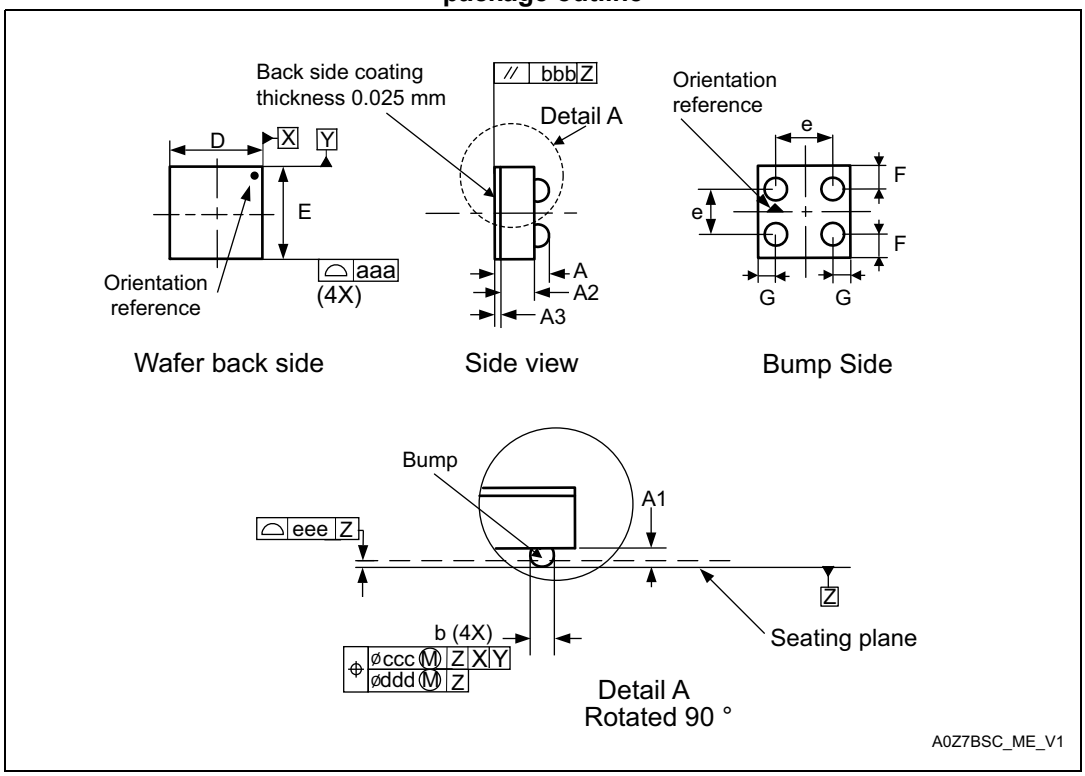


9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

9.1 Ultra Thin WLCSP package information

Figure 13. Ultra Thin WLCSP- 4-bump, 0.795 x 0.674 mm, wafer level chip scale package outline



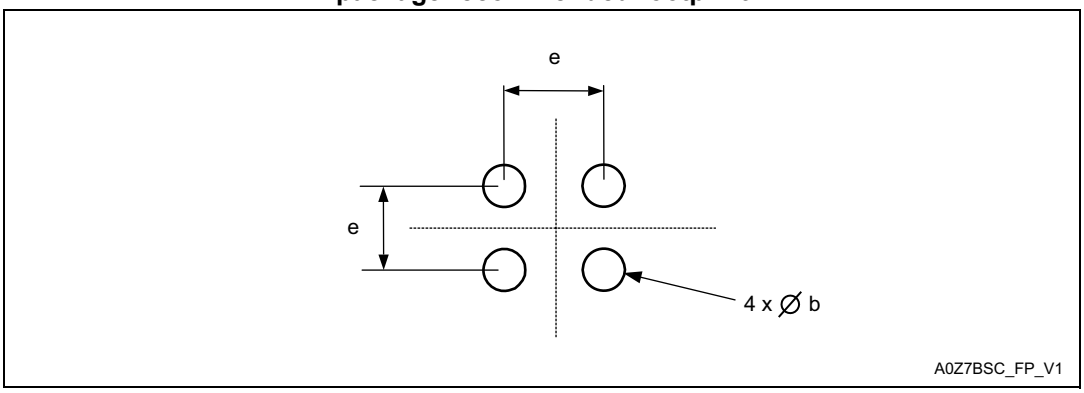
1. Drawing is not to scale.
2. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
3. Preliminary data

Table 16. Ultra Thin WLCSP- 4-bump, 0.795 x 0.674 mm, wafer level chip scale package mechanical data(1)

Symbol	millimeters			inches(2)		
	Min	Typ	Max	Min	Typ	Max
A	0.285	0.315	0.345	0.0112	0.0124	0.0136
A1	-	0.115	-	-	0.0045	-
A2	-	0.175	-	-	0.0069	-
A3 (BSC)	-	0.025	-	-	0.0010	-
b(3) (4)	-	0.160	-	-	0.0063	-
D	-	0.795	0.815	-	0.0313	0.0321
E	-	0.674	0.694	-	0.0265	0.0273
e	-	0.400	-	-	0.0157	-
F	-	0.137	-	-	0.0054	-
G	-	0.198	-	-	0.0078	-
aaa	-	-	0.110	-	-	0.0043
bbb	-	-	0.110	-	-	0.0043
ccc	-	-	0.110	-	-	0.0043
ddd	-	-	0.060	-	-	0.0024
eee	-	-	0.060	-	-	0.0024

1. Preliminary data
2. Values in inches are converted from mm and rounded to 4 decimal digits.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.
4. Primary datum Z and seating plane are defined by the spherical crowns of the bump.

Figure 14. Thin WLCSP- 4-bump, 0.795 x 0.674 mm, wafer level chip scale package recommended footprint



1. Dimensions are expressed in millimeters.

10 Part numbering

Table 17. Ordering information scheme

Example: M24 C32M - F CU 6 T /T F

Device type

M24 = I^2C serial access EEPROM

Device function

C32M = 32 Kbits (4096 x 8 bit)

Operating voltage

F = V_{CC} = 1.7 V to 5.5 V

Package(1)

CU = Ultra thin 4-bump WLCSP

Device grade

6 = device tested with standard test flow over –40 to 85 °C

Option

T = Tape and reel packing

blank = tube packing

Process technology(2)

T = Manufacturing technology code

Option

Blank = No Back Side Coating

F = Back Side Coating (WLCSP height = 0.345mm)

1. ECOPACK2® (RoHS compliant and free of brominated, chlorinated and antimony oxide flame retardants).
2. The process letter appears on the device package (marking) and on the shipment box. Please contact your nearest ST Sales Office for further information.

Engineering samples

Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

11 Revision history

Table 18. Document revision history

Date	Revision	Changes
07-Sep-2015	1	Initial release
01-Nov-2015	2	Updated *Table 6*, *Table 10* and *Section 9*
10-Feb-2016	3	Updated *Figure 2* and added *Table 2*

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