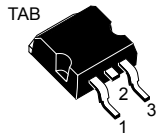
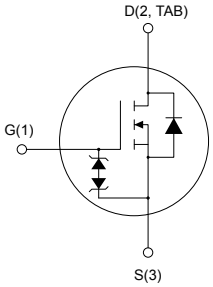
STB45N40DM2AG

Datasheet

Automotive-grade N-channel 400 V, 63 mΩ typ., 38 A, MDmesh DM2 Power MOSFET in a D²PAK package



D²PAK



AM01476v1_tab

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STB45N40DM2AG	400 V	72 m Ω	38 A	250 W

- AEC-Q101 qualified
- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM2 fast-recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Product status
STB45N40DM2AG

Product summary	
Order code	STB45N40DM2AG
Marking	45N40DM2
Package	D²PAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	38	A
	Drain current (continuous) at T_C = 100 °C	24	
I_{DM}(1)	Drain current (pulsed)	110	A
P_{TOT}	Total power dissipation at T_C = 25 °C	250	W
dv/dt(2)	Peak diode recovery voltage slope	50	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 38 A, di/dt = 800 A/µs, V_{DS} peak < $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$*
3. *V_{DS} ≤ 320 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.5	°C/W
R_{thJA}(1)	Thermal resistance, junction-to-ambient	30	

1. *When mounted on a standard 1-inch² area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}(1)	Avalanche current, repetitive or not repetitive	7	A
E_{AS}(2)	Single pulse avalanche energy	1100	mJ

1. *Pulse width is limited by $T_{J\ max.}$*
2. *starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V*

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	400			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 400 V			10	µA
		V_{GS} = 0 V, V_{DS} = 400 V, T_{case} = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 19 A		63	72	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	2600	-	pF
C_{oss}	Output capacitance		-	180	-	
C_{rss}	Reverse transfer capacitance		-	3.5	-	
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 to 320 V, V_{GS} = 0 V	-	300	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	4	-	Ω
Q_g	Total gate charge	V_{DD} = 320 V, I_D = 38 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	56	-	nC
Q_{gs}	Gate-source charge		-	13	-	
Q_{gd}	Gate-drain charge		-	28	-	

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 200 V, I_D = 19 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	20	-	ns
t_r	Rise time		-	6.7	-	
$t_{d(off)}$	Turn-off delay time		-	68	-	
t_f	Fall time		-	9.8	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		38	A
I_{SDM} (1)	Source-drain current (pulsed)		-		110	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 38 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} =38 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	95		ns
Q_{rr}	Reverse recovery charge		-	0.4		µC
I_{RRM}	Reverse recovery current		-	8.5		A
t_{rr}	Reverse recovery time	I_{SD} = 38 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	185		ns
Q_{rr}	Reverse recovery charge		-	1.62		µC
I_{RRM}	Reverse recovery current		-	17.5		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

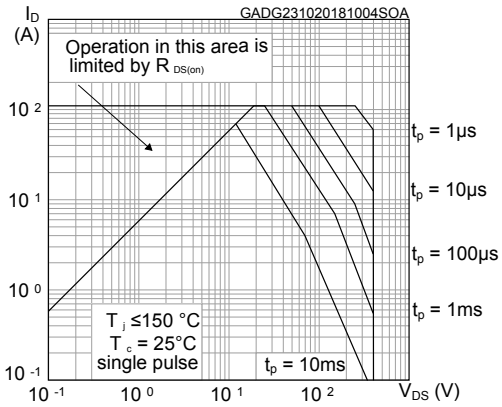


Figure 2. Thermal impedance

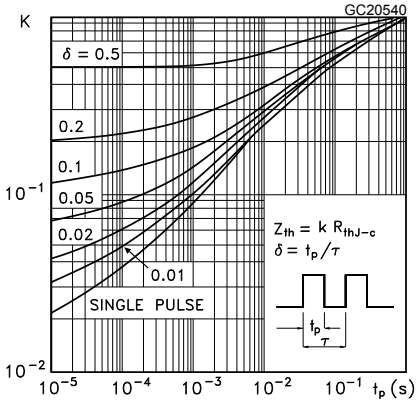


Figure 3. Output characteristics

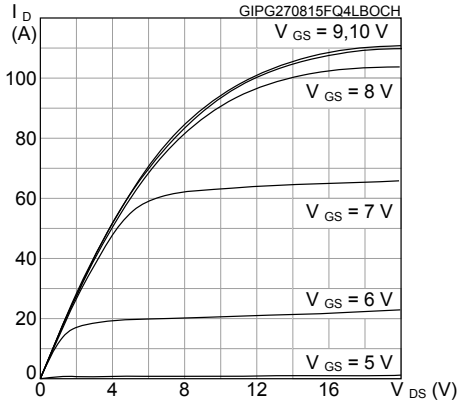


Figure 4. Transfer characteristics

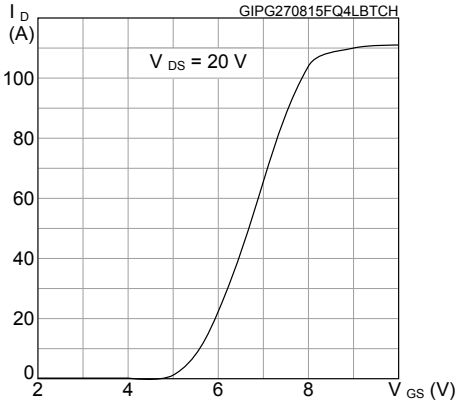


Figure 5. Gate charge vs gate-source voltage

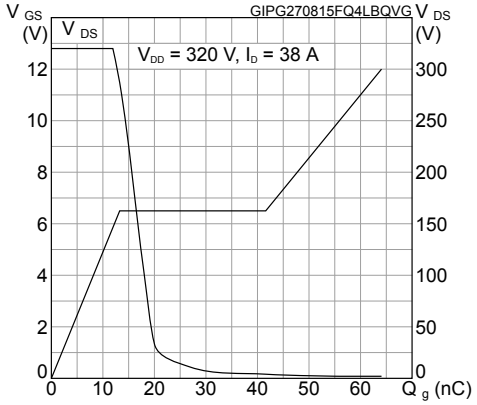


Figure 6. Static drain-source on-resistance

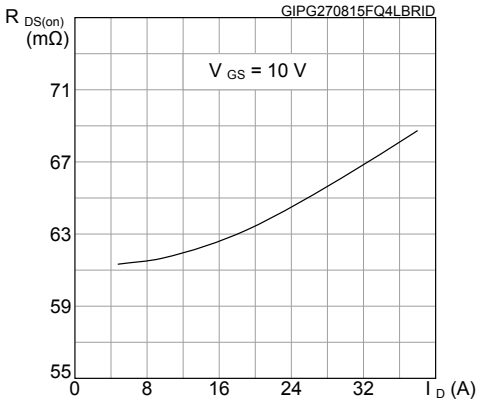


Figure 7. Capacitance variations

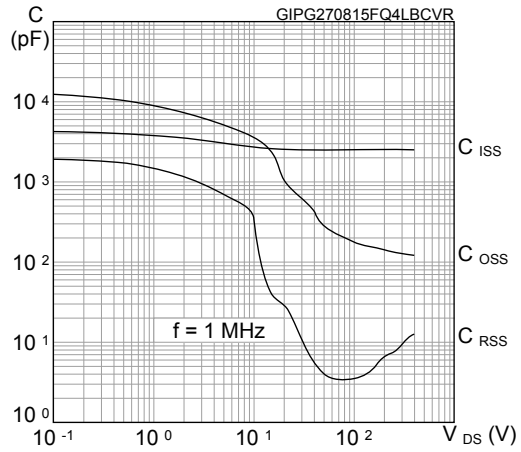


Figure 8. Normalized gate threshold voltage vs temperature

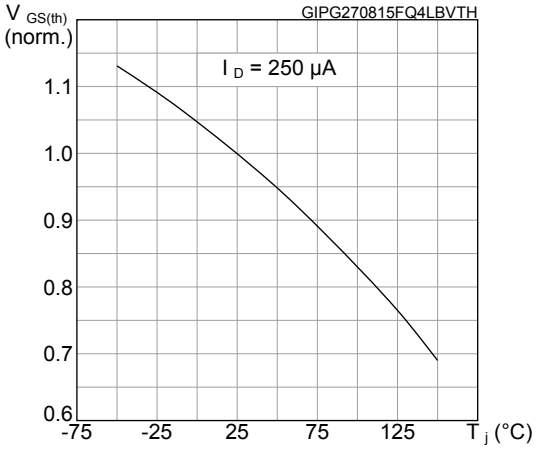


Figure 9. Normalized on-resistance vs temperature

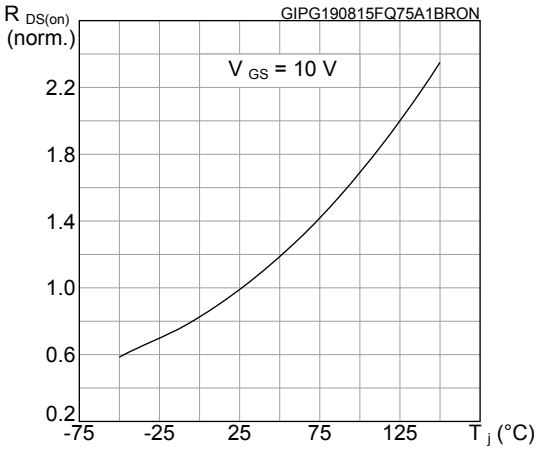


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

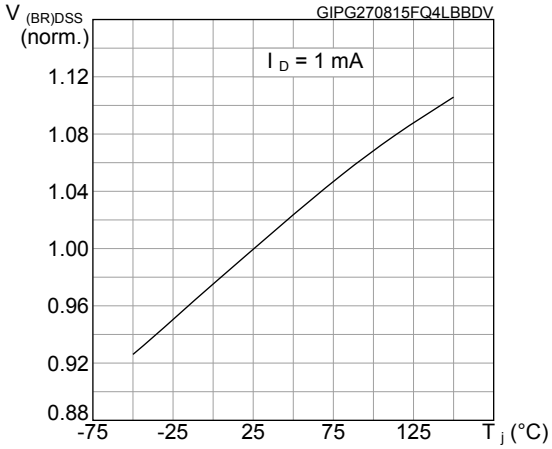


Figure 11. Output capacitance stored energy

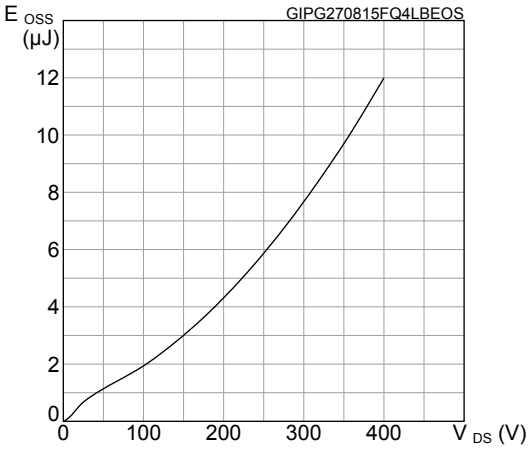
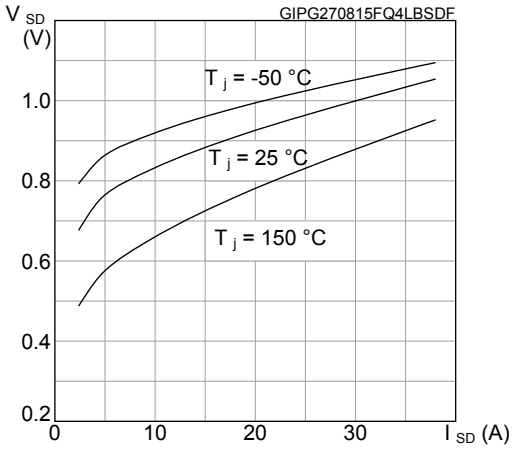
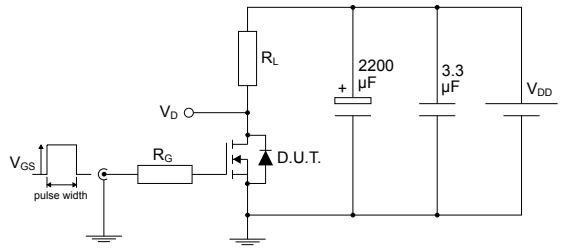


Figure 12. Source- drain diode forward characteristics



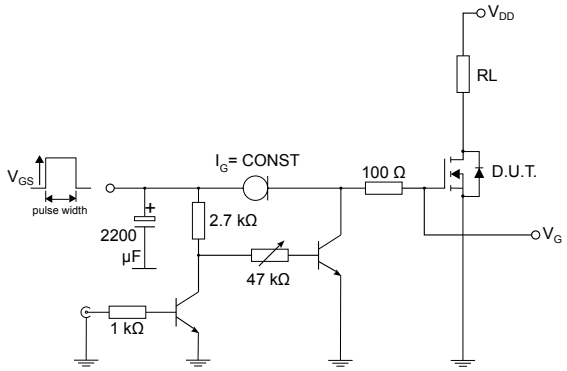
3 Test circuits

Figure 13. Test circuit for resistive load switching times



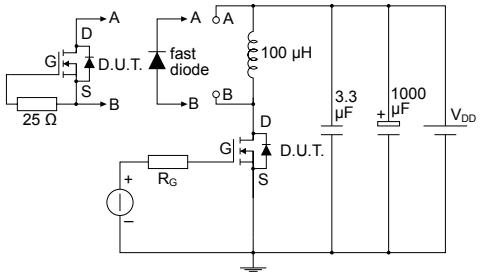
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Figure 14. Test circuit for gate charge behavior



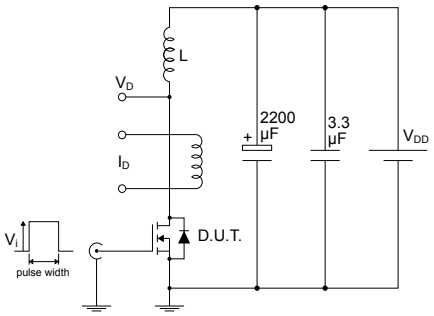
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Figure 15. Test circuit for inductive load switching and diode recovery times



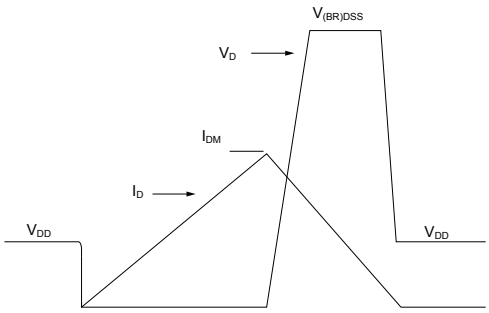
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Figure 16. Unclamped inductive load test circuit



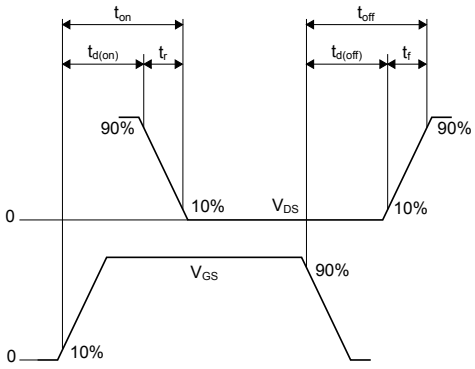
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Figure 17. Unclamped inductive waveform



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Figure 18. Switching time waveform



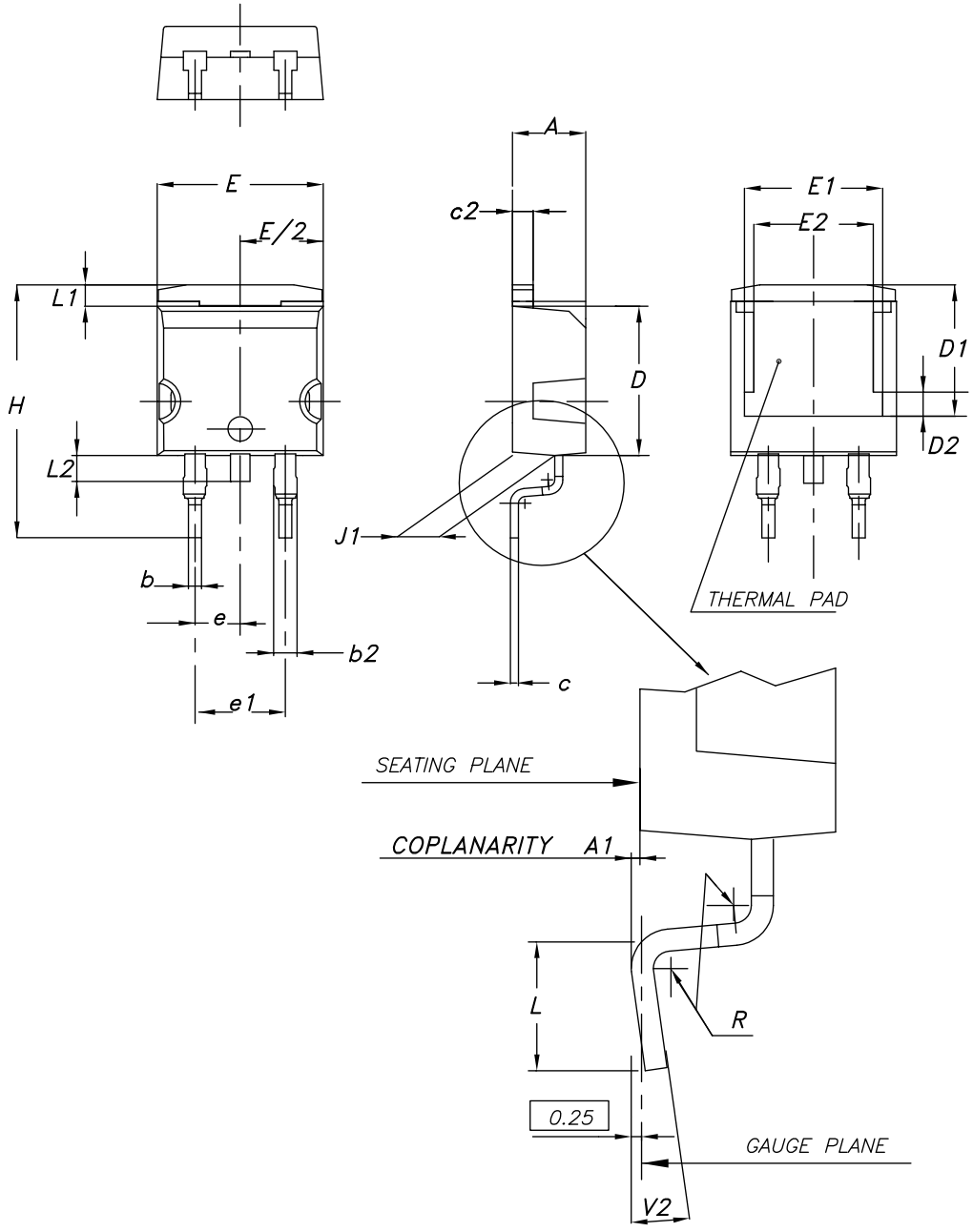
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A2 package information

Figure 19. **D²PAK (TO-263) type A2 package outline**



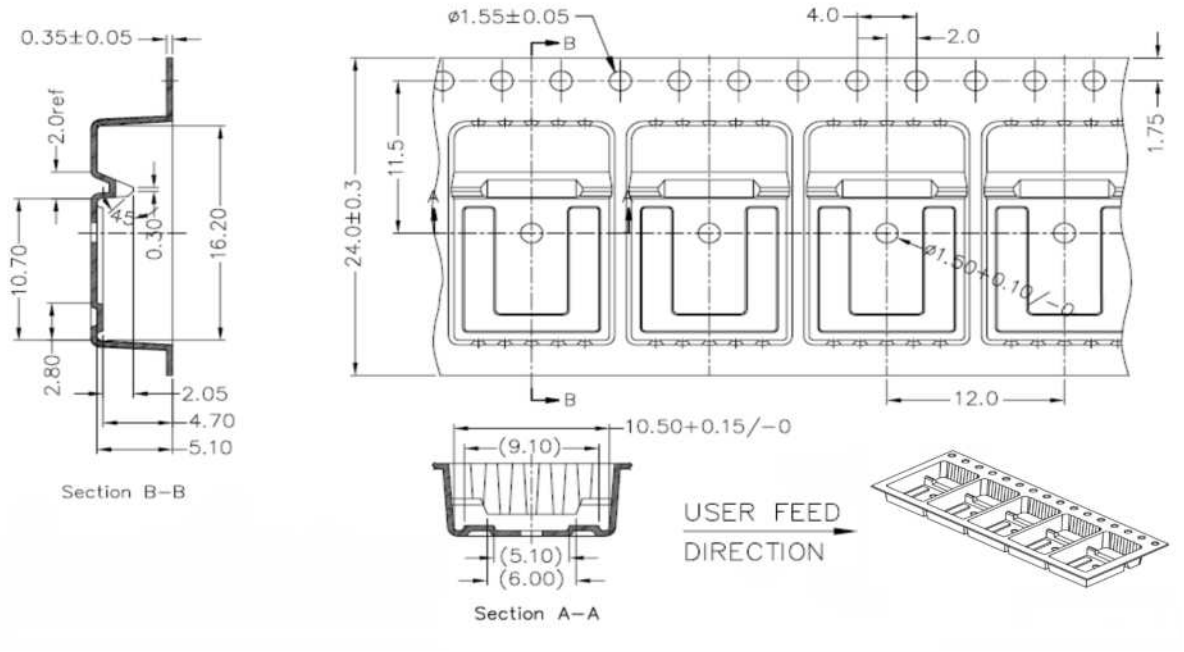
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Table 8. **D²PAK (TO-263) type A2 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

4.2 D²PAK packing information

Figure 20. **D²PAK tape drawing (dimensions are in mm)**



DM01095771_2

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
27-Aug-2015	1	Initial version
04-Aug-2016	2	Updated *Figure 2: "Safe operating area"*. Minor text changes.
14-Feb-2018	3	Removed maturity status indication from cover page. Updated *Section 4.1 D²PAK (TO-263) type A2 package information.* Minor text changes
23-Oct-2018	4	Updated *Table 1. Absolute maximum ratings* and *Table 7. Source-drain diode* Updated *Figure 1. Safe operating area* and *Figure 14. Test circuit for gate charge behavior.* Minor text changes.
27-Oct-2025	5	Updated Section 4: Package information. Minor text changes.

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