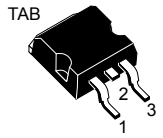
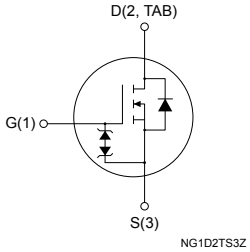
STB23N80K5

Datasheet

N-channel 800 V, 230 mΩ typ., 16 A MDmesh K5 Power MOSFET in a D²PAK package



D²PAK



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STB23N80K5	800 V	280 mΩ	16 A	190 W

- Very low FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Product status link
STB23N80K5

Product summary	
Order code	STB23N80K5
Marking	23N80K5
Package	D²PAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	16	A
	Drain current (continuous) at T_C = 100 °C	10	
I_{DM} (1)	Drain current (pulsed)	64	A
P_{TOT}	Total power dissipation at T_C = 25 °C	190	W
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 16 A, di/dt=100 A/µs; $V_{DS(peak)}$ < $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.*
3. *V_{DS} ≤ 640 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-ambient	0.66	°C/W
R_{thJA} (1)	Thermal resistance, junction-to-ambient	30	

1. *When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR} (1)	Avalanche current, repetitive or not repetitive	5	A
E_{AS} (2)	Single pulse avalanche energy	400	mJ

1. *Pulse width limited by T_J max.*
2. *Starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.*

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	800			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 800 V			1	µA
		V_{GS} = 0 V, V_{DS} = 800 V, T_C = 125 °C (1)			50	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 8 A		230	280	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1000	-	pF
C_{oss}	Output capacitance		-	65	-	
C_{rss}	Reverse transfer capacitance		-	1.5	-	
$C_{O(tr)}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 640 V, V_{GS} = 0 V	-	165	-	pF
$C_{O(er)}$ (2)	Equivalent output capacitance	V_{DS} = 0 to 640 V, V_{GS} = 0 V	-	59	-	
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	4.7	-	Ω
Q_g	Total gate charge	V_{DD} = 640 V, I_D = 16 A, V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	33	-	nC
Q_{gs}	Gate-source charge		-	6	-	
Q_{gd}	Gate-drain charge		-	25	-	

1. *Time related is defined as a constant equivalent capacitance giving the same charging time as C_{OSS} when V_{DS} increases from 0 to 80% V_{DSS}.*
2. *Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{OSS} when V_{DS} increases from 0 to 80% V_{DSS}*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 8 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	14	-	ns
t_r	Rise time		-	9	-	
$t_{d(off)}$	Turn-off delay time		-	48	-	
t_f	Fall time		-	9	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		16	A
I_{SDM} (1)	Source-drain current (pulsed)		-		64	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 16 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 16 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	410		ns
Q_{rr}	Reverse recovery charge		-	7		µC
I_{RRM}	Reverse recovery current		-	34		A
t_{rr}	Reverse recovery time	I_{SD} = 16 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	650		ns
Q_{rr}	Reverse recovery charge		-	10		µC
I_{RRM}	Reverse recovery current		-	32		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

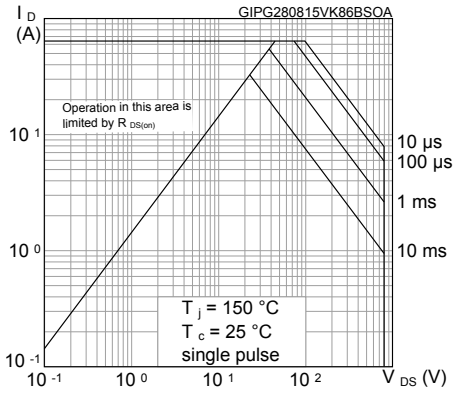


Figure 2. Normalized transient thermal impedance

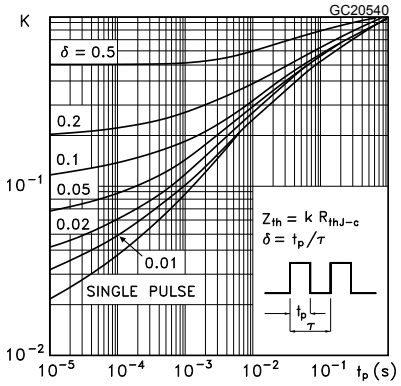


Figure 3. Typical output characteristics

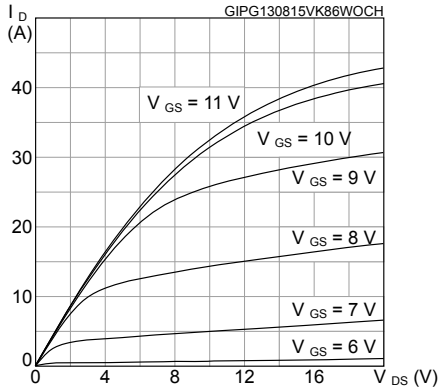


Figure 4. Typical transfer characteristics

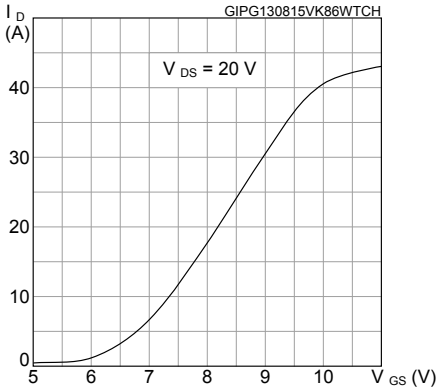


Figure 5. Typical gate charge characteristics

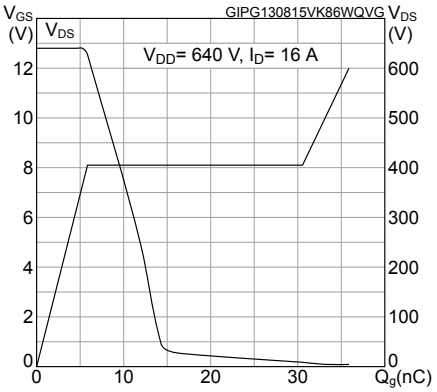


Figure 6. Typical drain-source on-resistance

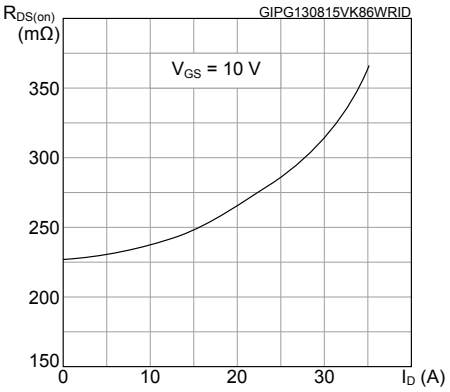


Figure 7. Typical capacitance characteristics

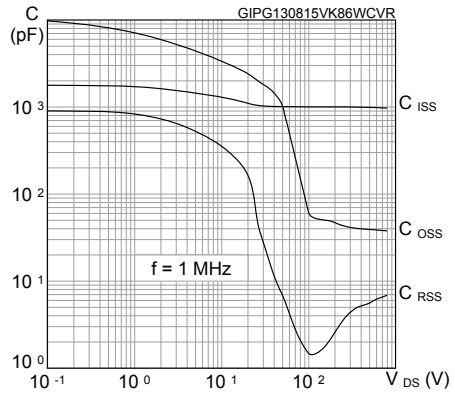


Figure 8. Normalized gate threshold vs temperature

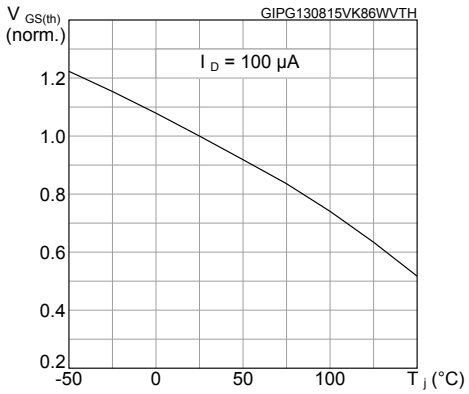


Figure 9. Normalized on-resistance vs temperature

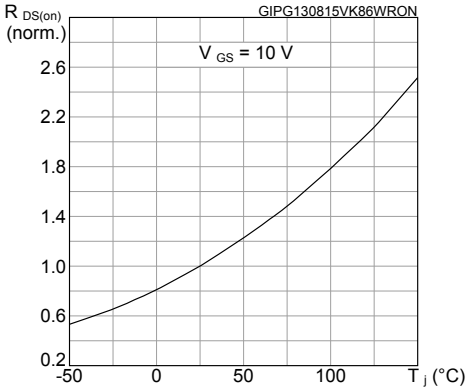


Figure 10. Normalized breakdown voltage vs temperature

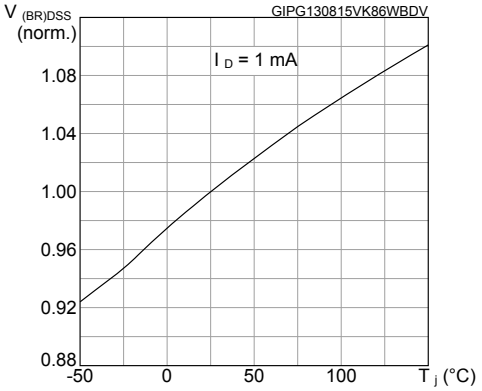
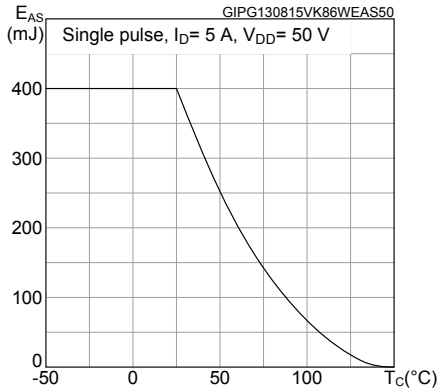
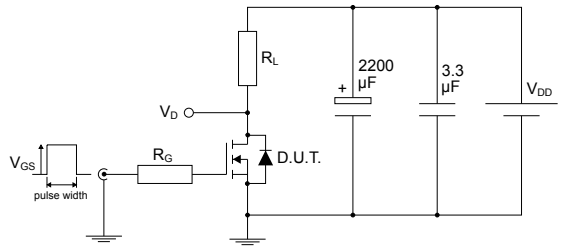


Figure 11. Maximum avalanche energy vs temperature



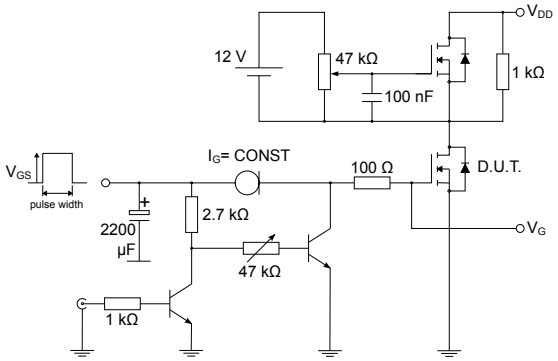
3 Test circuits

Figure 12. Test circuit for resistive load switching times



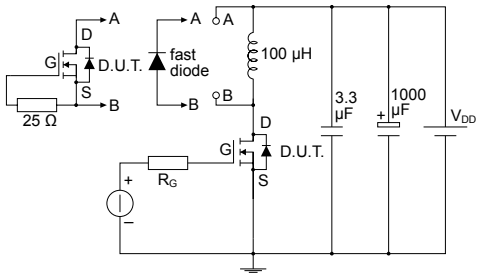
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Figure 13. Test circuit for gate charge behavior



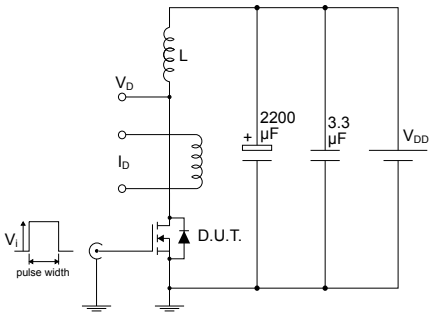
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Figure 14. Test circuit for inductive load switching and diode recovery times



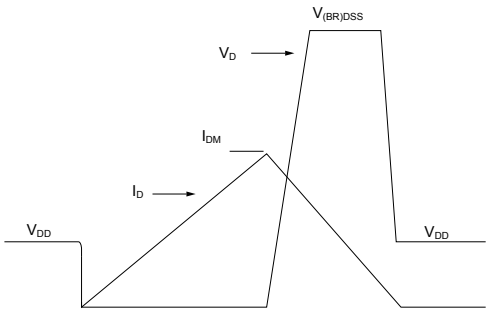
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Figure 15. Unclamped inductive load test circuit



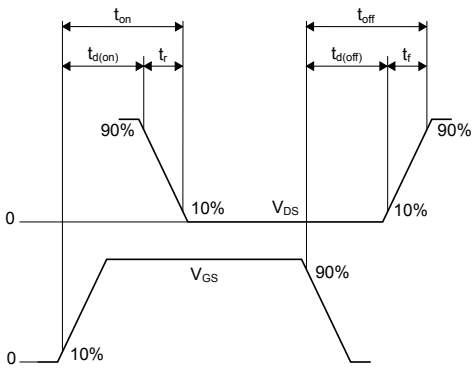
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Figure 16. Unclamped inductive waveform



AM01472v1

Figure 17. Switching time waveform



AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 18. **D²PAK (TO-263) type A package outline**

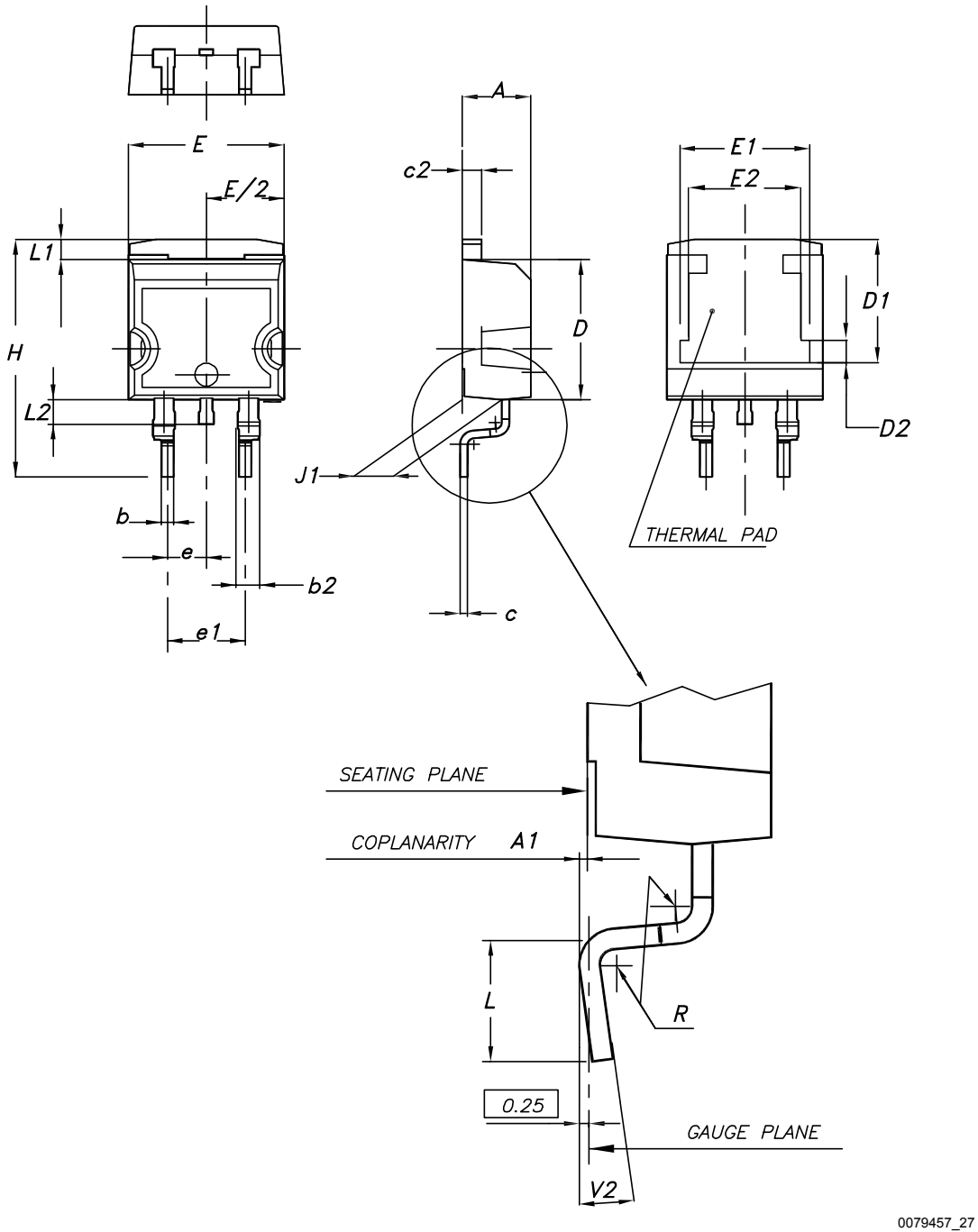
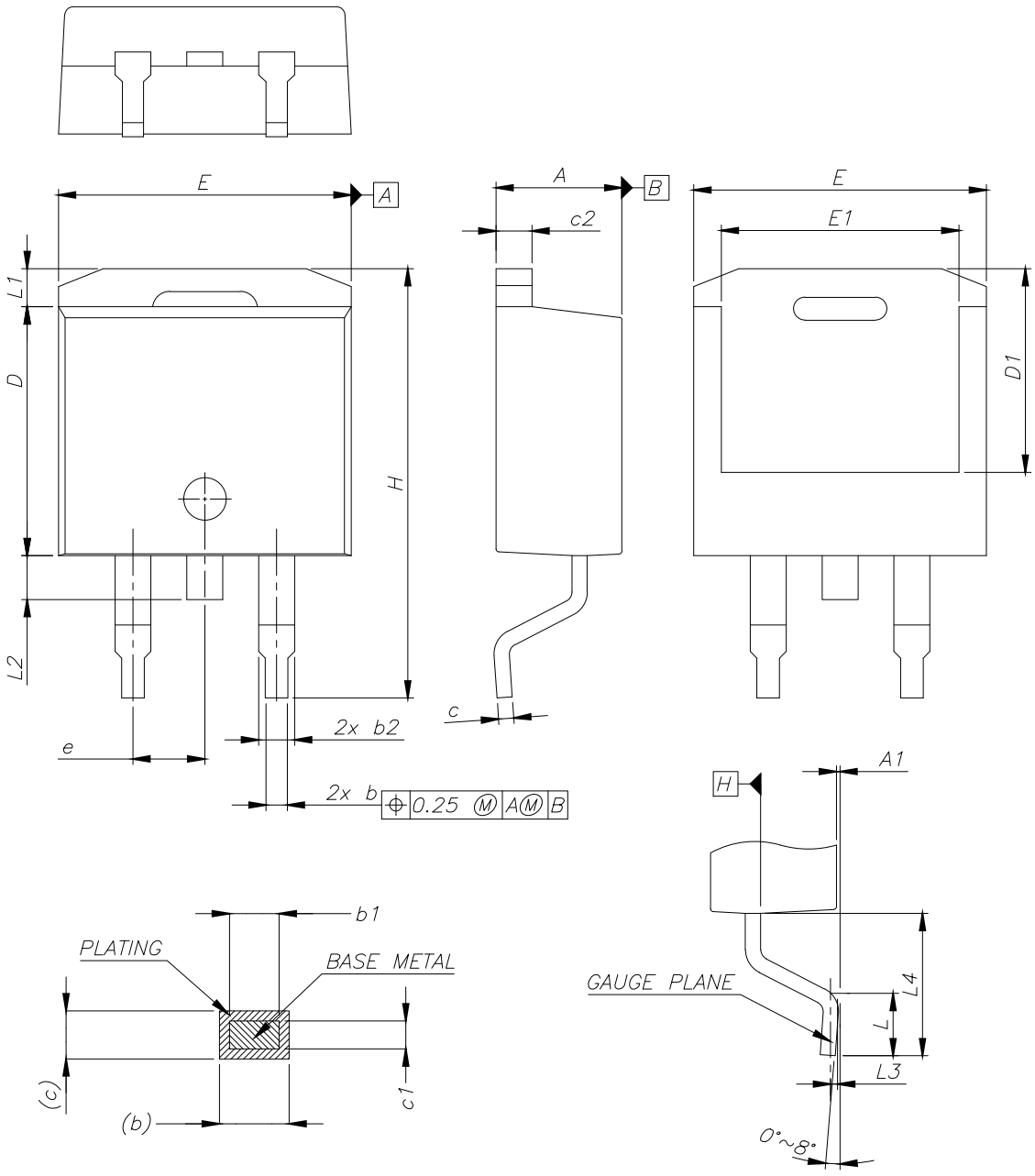


Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

4.2 D²PAK (TO-263) type B package information

Figure 19. D²PAK (TO-263) type B package outline

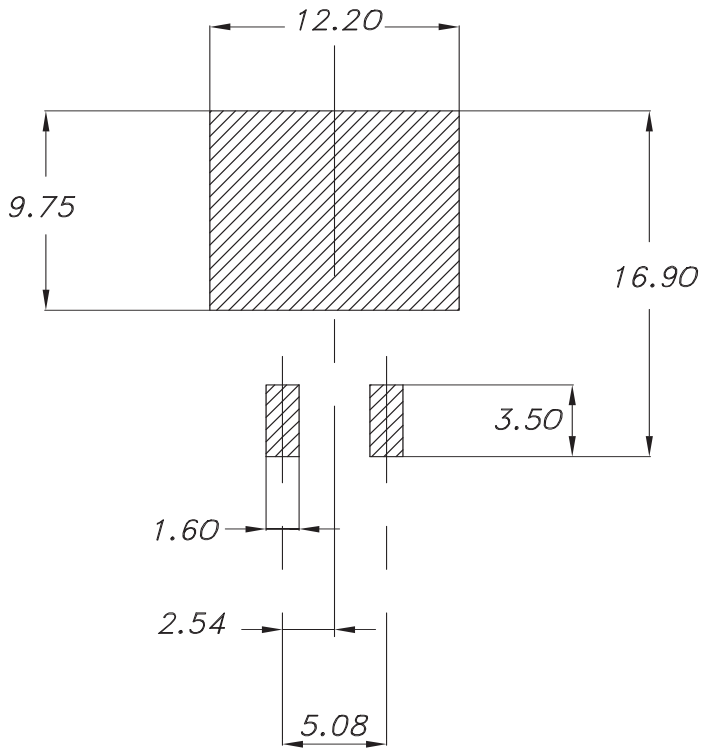


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Table 9. D²PAK (TO-263) type B mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.36		4.56
A1	0.00		0.25
b	0.70		0.90
b1	0.51		0.89
b2	1.17		1.37
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.34
D	8.60		9.00
D1	6.90		7.50
E	10.15		10.55
E1	8.10		8.70
e	2.54 BSC		
H	15.00		15.60
L	1.90		2.50
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

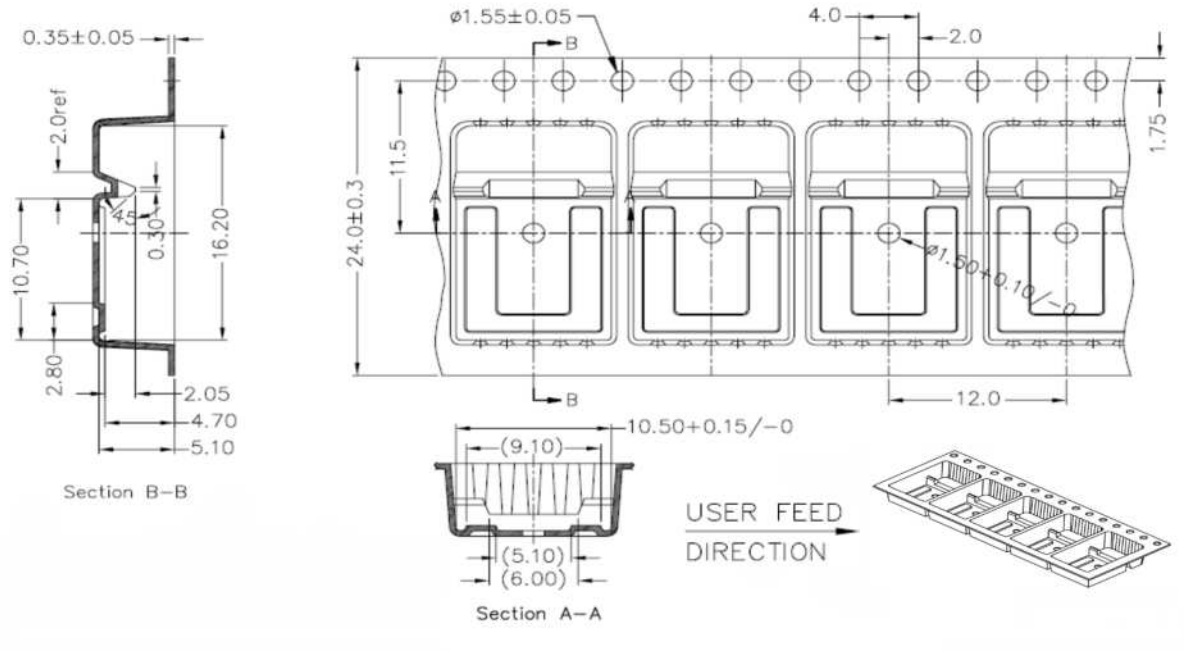
Figure 20. D²PAK (TO-263) recommended footprint (dimensions are in mm)



0079457_Rev27_footprint

4.3 D²PAK packing information

Figure 21. **D²PAK tape drawing (dimensions are in mm)**



DM01095771_2

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
28-Aug-2015	1	First release.
21-May-2021	2	Updated *Section 4.1 D²PAK (TO-263) type A package information*. Added *Section 4.3 D²PAK (TO-263) type B package information*. Minor text changes.
21-Aug-2025	3	Updated Section 4: Package information. Minor text changes.

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