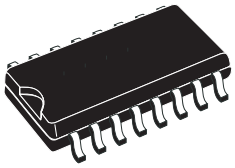
VIPer0P

Datasheet

Zero-power off-line high voltage converter



SO16 narrow

Product status link
VIPer0P

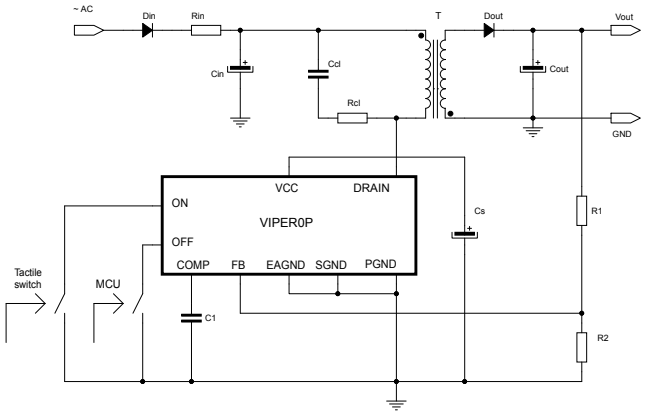
Features

- Smart stand-by architecture using the zero-power mode (ZPM)
- ZPM management by MCU easily realizable
- 800 V avalanche-rugged power MOSFET allowing ultra wide VAC input range to be covered
- Embedded HV startup and sense-FET
- Current mode PWM controller
- Drain current limit protection (OCP)
- Wide supply voltage range: 4.5 V to 30 V
- Self-supply option allows to remove the auxiliary winding or bias components
- Minimized system input power consumption:
  - Less than 4 mW @ 230 V_{AC} in ZPM
  - Less than 10 mW @ 230 V_{AC} in no-load condition
  - Less than 400 mW @ 230 V_{AC} with 250 mW load
- Jittered switching frequency reduces the EMI filter cost
  - 60 kHz ± 7% (type L)
  - 120 kHz ± 7% (type H)
- Embedded E/A with 1.2 V reference and separate ground for easy negative voltage setting
- Protections with automatic restart: overload/short circuit (OLP), max. duty cycle counter, V_{CC} clamp
- Pulse-skip protection to prevent flux-runaway
- Embedded thermal shutdown
- Built in soft start for improved system reliability

Applications

- SMPS for home appliances, home automation, industrial, lighting and consumers

Figure 1. Basic application schematic

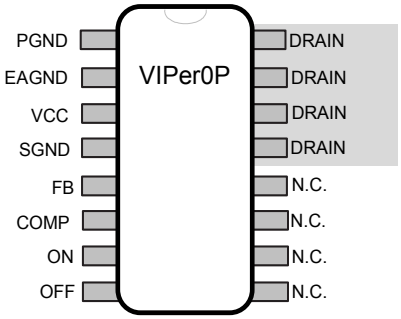


1 Description

The device is a high-voltage converter that smartly integrates an 800 V avalanche rugged power MOSFET with PWM current-mode control. The power MOSFET with 800 V breakdown voltage allows extended input voltage range to be applied, as well as to reduce the size of the DRAIN snubber circuit. This IC is capable of meeting the most stringent energy-saving standards as it has very low consumption and operates in pulse frequency modulation under light load. The zero-power mode (ZPM) feature enables the IC to work in an idle state, where the system is totally shutdown. An MCU can be easily connected to the IC for smart ZPM management and it can be supplied by the IC itself during the idle state. The design of flyback, buck and buck boost converters is supported. The integrated HV startup, sense FET, error amplifier and oscillator with jitter allow a complete application to be designed with a minimum component count. In flyback non isolated topology, a negative output voltage is easily set thanks to the integrated error amplifier with separate ground.

2 Pin setting

Figure 2. Connection diagram



GIPD210420151108MT

Note: The PCB copper area for heat dissipation has to be provided under the DRAIN pins.

Table 1. Pin description

SO16N	Name	Function
1	PGND	**Power ground and MOSFET source.** The pulsed current flowing through the Power MOSFET must be closed on this pin. The pin must be connected to the same ground plan of SGND with the shortest track.
2	EAGND	**Error amplifier ground reference.** In case of non-isolated flyback converter with negative output voltage, this pin can be connected directly to the negative rail. Otherwise, in case of positive output voltage, the pin must be shorted to SGND.
3	VCC	**Controller supply.** An external storage capacitor has to be connected across this pin and SGND. The pin, internally connected to the high-voltage current source, provides the VCC capacitor charging current at startup and, if self-supply mode is selected, also during steady-state operation. A small bypass capacitor (0.1 µF typ.) in parallel, placed as close as possible to the IC, is also recommended, for noise filtering purpose.
4	SGND	**Signal ground.** All of the groundings of bias components must be tied to a trace going to this pin and kept separate from the pulsed current return.
5	FB	**Direct feedback.** It is the inverting input of the internal transconductance E/A, which is internally referenced to 1.2 V with respect to EAGND. In case of non-isolated converter, the output voltage information is directly fed into the pin through a voltage divider. In case of primary regulation, the FB voltage divider is connected to the VCC. The E/A is disabled soldering FB to EAGND.
6	COMP	**Compensation.** It is the output of the internal E/A. A compensation network is placed between this pin and SGND to achieve stability and good dynamic performance of the control loop. In case of secondary feedback, the internal E/A must be disabled and the COMP directly driven by the optocoupler to control the DRAIN peak current setpoint.
7	ON	**ZPM exit.** When the device is in ZPM, the IC is reactivated by forcing this pin to SGND for a debounce time, t_{DEB_ON}. Due to the extremely low level of energy available while in ZPM, the pin can be noise sensitive. A film-type bypass capacitor from the pin to SGND is therefore recommended in a noisy environment to prevent improper startup of the device. An internal pull-up resistor keeps the pin voltage at V_{ON} level during normal operation.
8	OFF	**ZPM enter.** To enter ZPM this pin has to be forced to SGND, for a debounce time t_{DEB_OFF}. An internal pull-up resistor keeps the pin voltage at V_{OFF} level during normal operation.
9 to12	N.C.	These pins are not internally connected and must be left floating in order to get a safe clearance distance.
13 to 16	DRAIN	**MOSFET drain**. The internal high-voltage current source sinks current from this pin to charge the VCC capacitor at startup and during steady-state operation. These pins are mechanically connected to the internal metal PAD of the MOSFET in order to facilitate heat dissipation. On the PCB, some copper area must be placed under these pins in order to decrease the total junction-to-ambient thermal resistance thus facilitating the power dissipation.

3 Electrical and thermal ratings

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter (1)	Min.	Max.	Unit
V_{DS}	13 to 16	Drain-to-source (ground) voltage	-0.3	800	V
I_{DRAIN}	13 to 16	Pulsed drain current (pulse-width limited by SOA)		2	A
V_{EAGND}	2	EAGND voltage (referred to VCC)	-35 (2)	0.3	V
		EAGND voltage (referred to SGND)		0.3	V
V_{CC}	3	VCC voltage (referred to EAGND)	-0.3	35 (2)	V
		VCC voltage (referred to SGND)	-0.3	35	V
I_{CC}	3	VCC internal Zener current		30	mA
V_{FB}	5	FB voltage (referred to EAGND)	-0.3	5 (2)	V
		FB voltage (referred to VCC)	-35	0.3	V
V_{COMP}	6	COMP voltage (referred to SGND)	-0.3	5 (2)	V
		COMP voltage (referred to VCC)	-35	0.3	V
V_{ON}	7	ON voltage (referred to SGND)	-0.3	5.5	V
		ON voltage (referred to VCC)	-35	0.3	V
V_{OFF}	8	OFF voltage (referred to SGND)	-0.3	5.5	V
		OFF voltage (referred to VCC)	-35	0.3	V
P_{TOT}		Power dissipation @ T_{amb} < 50 °C		1	W
T_j		Junction temperature operating range	-40	150	°C
T_{STG}		Storage temperature	-55	150	°C

1. *Stresses beyond those listed absolute maximum ratings may cause permanent damage to the device.*
2. *Voltage is internally limited.*

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
		SO16N	
R_{thJP}	Thermal resistance junction-pin (dissipated power 1 W)	35	°C/W
R_{thJA} (1)	Thermal resistance junction-ambient (dissipated power 1 W)	110	
	Thermal resistance junction-ambient (dissipated power 1 W) (2)	80	

1. *Derived by characterization.*
2. *When mounted on a standard single side FR4 board with 100 mm² (0.155² inch) of Cu (35 µm thick).*

Table 4. Avalanche characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{AR}	Avalanche current	Pulse-width limited by T_{Jmax} Repetitive and non-repetitive			0.8	A
E_{AS}	Single pulse avalanche energy(1)	Starting T_J = 25 °C I_{AS} = I_{AR}; V_{DS} = 100 V			0.5	mJ

1. *Parameter derived by characterization.*

3.1 Electrical characteristics

T_j = -40 to 125 °C, V_{CC} = 9 V (unless otherwise specified).

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BVDSS}	Breakdown voltage	I_{DRAIN} = 1 mA, V_{COMP} = SGND, T_J = 25 °C	800			V
I_{DSS}	Drain-source leakage current	V_{DS} = 400 V, V_{COMP} = SGND, T_J = 25 °C			1	µA
$R_{DS(on)}$	Static drain-source on-resistance	I_{DRAIN} = 200 mA, T_J = 25 °C			20	Ω
		I_{DRAIN} = 200 mA, T_J = 125 °C			40	
$C_{OSS\ EQ}$	Equivalent output capacitance	V_{GS} = 0; V_{DS} = 0 to 640 V, T_J = 25 °C		10		pF

Table 6. Supply section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
High voltage startup current source						
V_{BVDSS_SU}	Breakdown voltage of startup MOSFET		800			V
V_{HV_START}	Drain-source start up voltage		40		80	V
R_G	Startup resistor	V_{DRAIN} = 400 V, V_{DRAIN} = 600 V $V_{FB} > V_{FB_REF}$,	28	34	40	MΩ
I_{CH1}	VCC charging current at startup	V_{CC} = 0 V, T_J = 25 °C $V_{FB} > V_{FB_REF}$, V_{DRAIN} = 100 V	0.7	1	1.3	mA
I_{CH2}	VCC charging current at startup	V_{CC} = 1 V, T_J = 25 °C $V_{FB} > V_{FB_REF}$, V_{DRAIN} = 100 V	2.3	3.2	4.1	
I_{CH3} (1)	Max. VCC charging current in self-supply	V_{CC} = 6 V, T_J = 25 °C $V_{FB} > V_{FB_REF}$, V_{DRAIN} = 100 V	6.4	7.8	9.2	
IC supply and consumptions						
V_{CC}	Operating voltage range	referred to SGND, V_{EAGND} = 0 referred to EAGND, V_{EAGND} < 0	4.5		30	V
$V_{CCclamp}$	Clamp voltage	$I_{CC} = I_{clamp_max}$	30	32.5	35	V
$I_{clamp\ max}$	Clamp shutdown current	$V_{CC} > V_{CCclamp}$	29	35	41	mA
$t_{clamp\ max}$	Clamp time before shutdown			5		ms
V_{CCon}	V_{CC} startup threshold	V_{FB} = 1.2 V,V_{DRAIN} = 400 V	7.5	8	8.5	V
V_{CSon}	HV current source turn-on threshold	V_{CC} falling	4	4.25	4.5	V
V_{CCoff}	UVLO	V_{FB} = 1.2 V,V_{DRAIN} = 400 V	3.75	4	4.25	V
I_q	Quiescent current	Not switching, $V_{FB} > V_{FB_REF}$		0.25	0.35	mA
I_{q_ZPM}	Quiescent current in ZPM	Not switching, $V_{FB} > V_{FB_REF}$, V_{DRAIN} = 325 V			20	µA
I_{CC}	Operating supply current, switching	F_{OSC} = 60 kHz, V_{DS} = 150 V, V_{COMP} =1.2 V	0.6	0.9	1.2	mA
		F_{OSC} = 120 kHz, V_{DS} = 150 V, V_{COMP} =1.2 V	0.9	1.2	1.5	

1. *Current supplied only during the main MOSFET OFF time.*

Table 7. Controller section

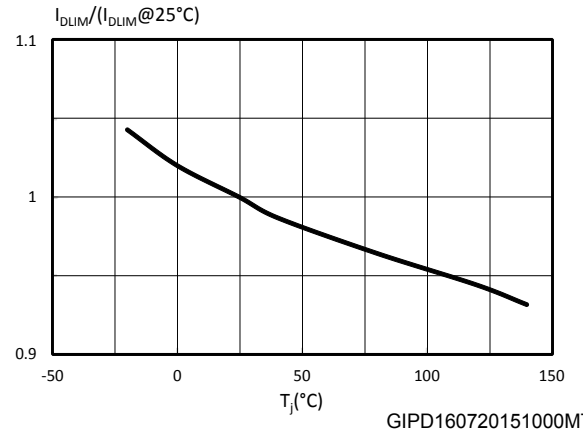
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E/A						
V_{EAGND}	E/A ground reference voltage	Referred to SGND	-20		0	V
V_{FB_REF}	E/A reference voltage	Referred to EAGND	1.175	1.2	1.225	V
V_{FB_DIS}	E/A disable voltage	Referred to EAGND	150	250	350	mV
$I_{FB\ PULL\ UP}$	Pull-up current		0.5	1	1.5	µA
G_M	Trans conductance	V_{COMP} = 1.5 V, $V_{FB} > V_{FB_REF}$	300	550	700	µA/V
I_{COMP1}	Max. source current	V_{FB} = 0.5 V, V_{COMP} = 1.5 V	75	100	125	µA
I_{COMP2}	Max. sink current	V_{FB} = 2 V, V_{COMP} = 1.5 V	75	100	125	µA
$R_{COMP(DYN)}$	Dynamic resistance	V_{COMP} = 2.7 V, V_{FB} = EAGND	55	65	75	kΩ

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{COMPH}	Current limitation threshold	Referred to SGND	2.65	3.2	3.75	V
V_{COMPL}	PFM threshold	Referred to SGND	0.7	0.9	1.1	V
OLP and timing						
I_{DLIM}	Drain current limitation	T_J = 25 °C	380	400	420	mA
I^2f	Power coefficient	VIPER0PL	-10%	9.6	+10%	A^2·kHz
		VIPER0PH		19.2		
I_{DLIM_PFM}	Drain current limitation at light load	T_J = 25 °C $V_{COMP} = V_{COMPL}$ (1)	60	95	130	mA
t_{OVL}	Overload delay time	F_{OSC} = 60 kHz (VIPER0PL) F_{OSC} = 120 kHz (VIPER0PH)	45	50	55	ms
t_{OVL_MAX}	Max. overload delay time	$F_{OSC} = F_{OSC_MIN}$ (VIPER0PL)	180	200	220	ms
		$F_{OSC} = F_{OSC_MIN}$ (VIPER0PH)	360	400	440	
t_{SS}	Soft-start time			8		ms
t_{ON_MIN}	Minimum turn-on time	$V_{FB} = V_{FB_REF}$ V_{CC} = 9 V, V_{COMP} = 1 V,	230		350	ns
$t_{RESTART}$	Restart time after fault			1		s
ZPM						
V_{OFFth}	ZPM entering threshold	During normal operation V_{CC}= 7 V	0.75	1	1.25	V
V_{OFF}	Operating voltage level	Pin floating	3.75		4.75	V
R_{OFF}	Pull-up resistor on OFF pin		32	41	50	kΩ
t_{DEB_OFF}	OFF debounce time			10	16	ms
V_{ONth}	ZPM exiting threshold	During ZPM	0.75	1	1.25	V
V_{ON}	Operating voltage level	Pin floating	3.75		4.75	V
R_{ON}	Pull-up resistor on ON pin		32	41	50	kΩ
t_{DEB_ON} (2)	ON debounce time			20	35	µs
Oscillator						
F_{OSC}	Switching frequency	VIPER0PL	54	60	66	kHz
		VIPER0PH	108	120	132	
F_{OSC_MIN}	Minimum switching frequency	(3)	13.5	15	16.5	kHz
F_D	Modulation depht			±7% F_{OSC}		kHz
F_M	Modulation frequency			260		Hz
D_{MAX}	Max. duty cycle		70		80	%
Thermal shutdown						
T_{SD}	Thermal shutdown temperature	(2)	150	160		°C

1. *See Section 5.10 Pulse frequency modulation.*
2. *Parameter assured by design, characterization, and statistical correlation.*
3. *See Section 5.7 Pulse skipping.*

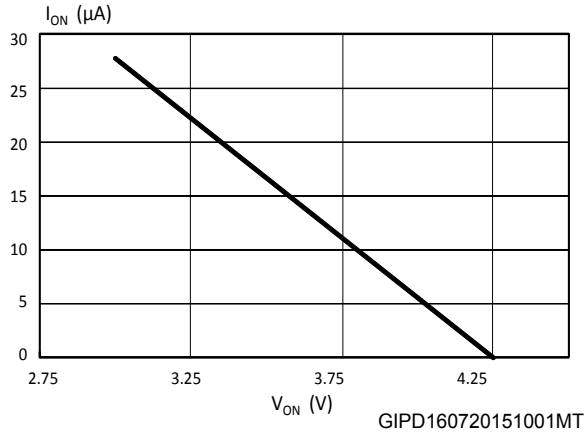
4 Typical electrical characteristics

Figure 3. I_{DLIM} vs T_J



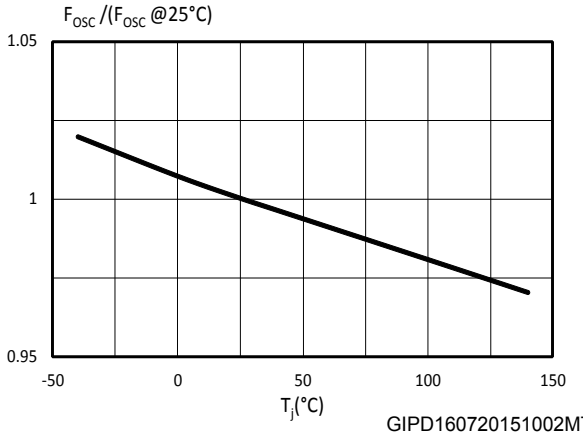
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Figure 4. I_{ON} vs V_{ON}



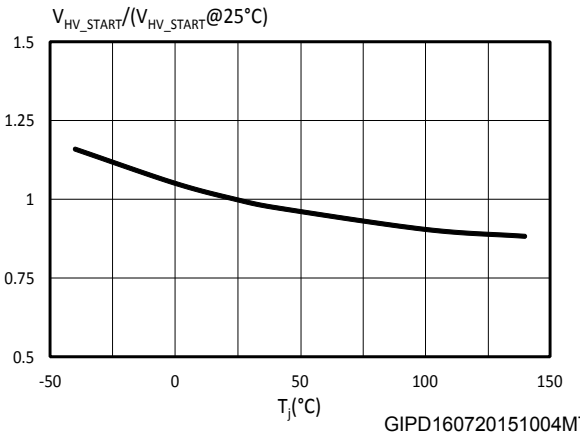
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Figure 5. F_{OSC} vs T_J



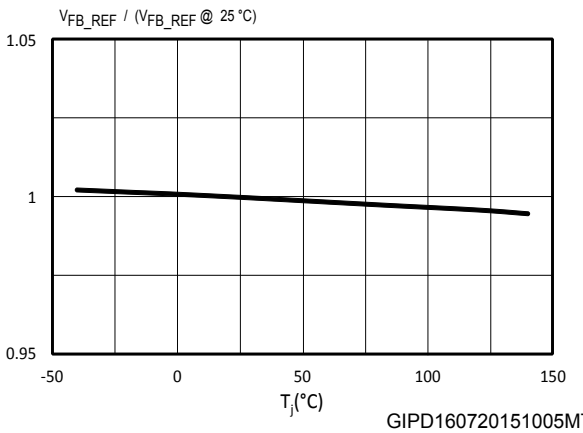
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Figure 6. V_{HV_START} vs T_J



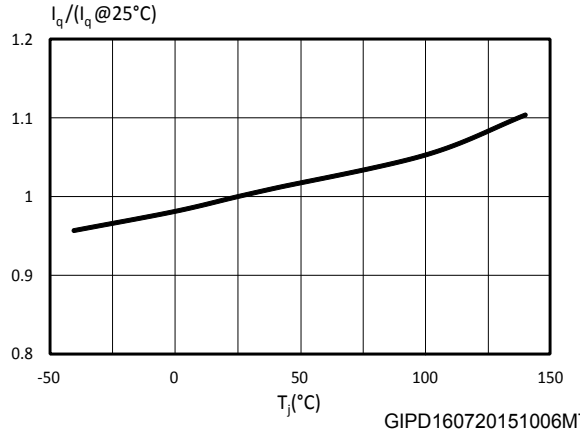
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Figure 7. V_{FB_REF} vs T_J



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Figure 8. Quiescent current I_q vs T_J



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Figure 9. Operating current I_{CC} vs T_J

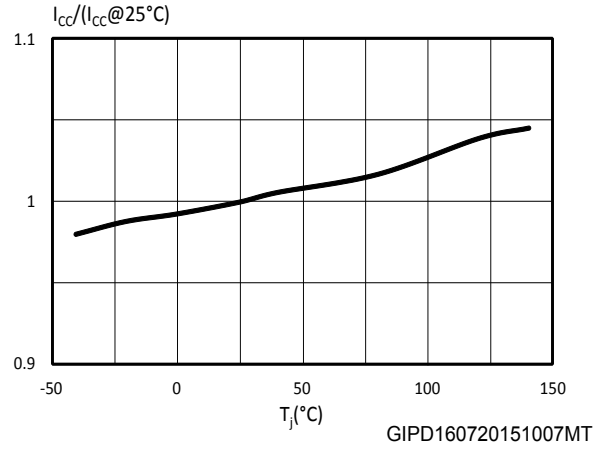


Figure 10. I_{COMP} vs T_J

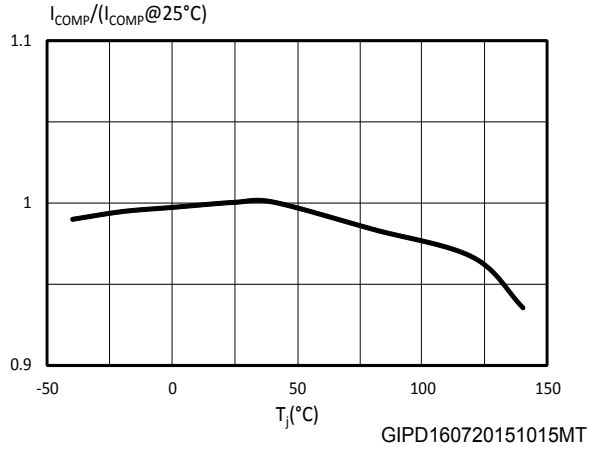


Figure 11. I_{CH1} vs T_J

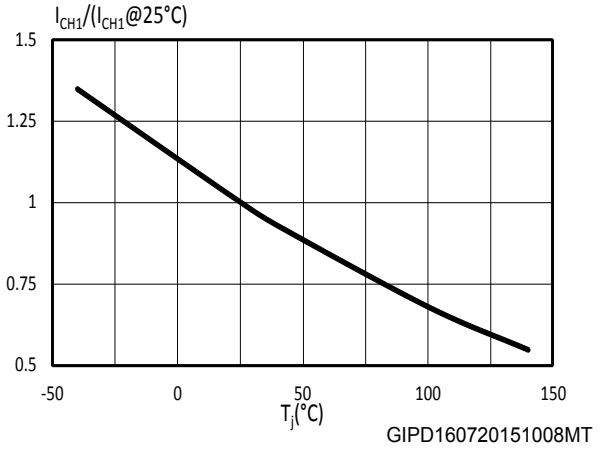


Figure 12. I_{CH1} vs V_{DRAIN}

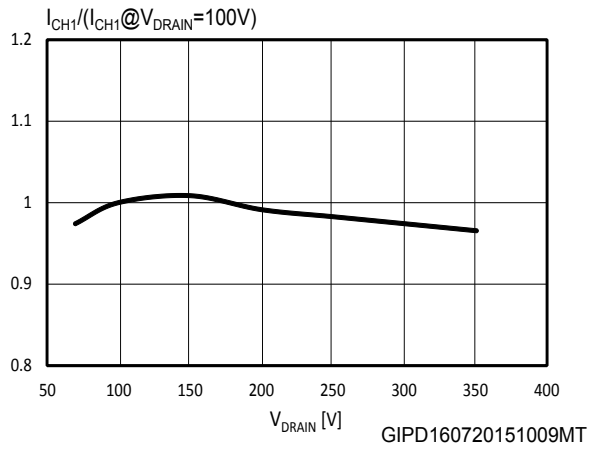


Figure 13. I_{CH2} vs T_J

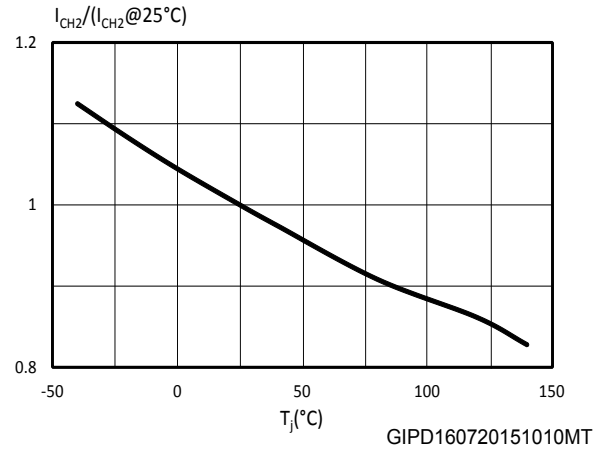


Figure 14. I_{CH2} vs V_{DRAIN}

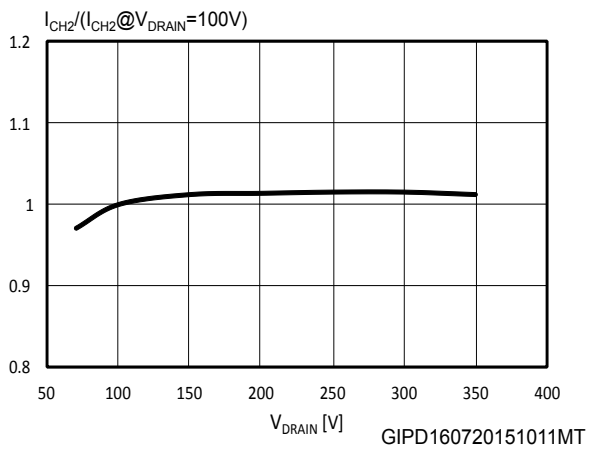


Figure 15. I_{CH3} vs T_J

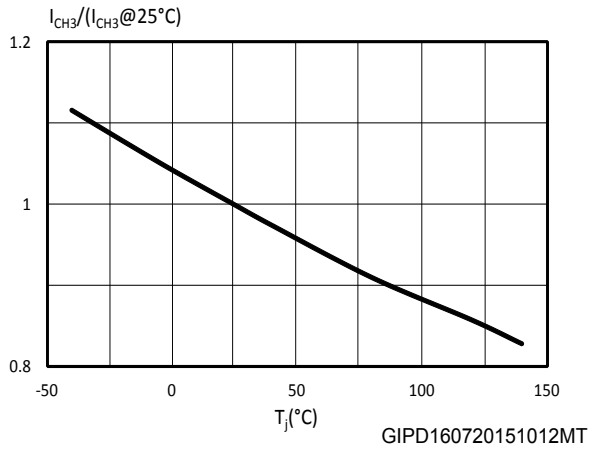


Figure 16. I_{CH3} vs V_{DRAIN}

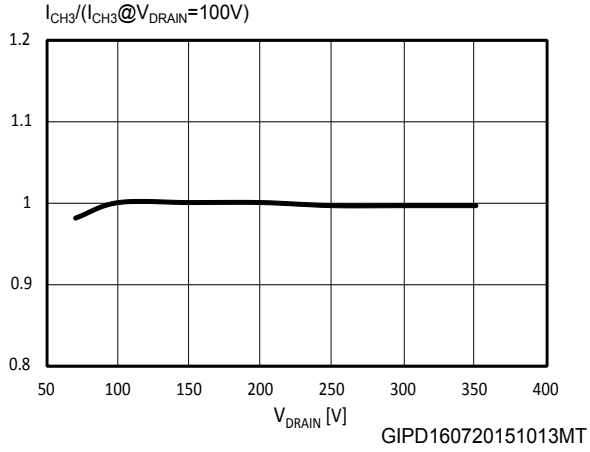


Figure 17. G_M vs T_J

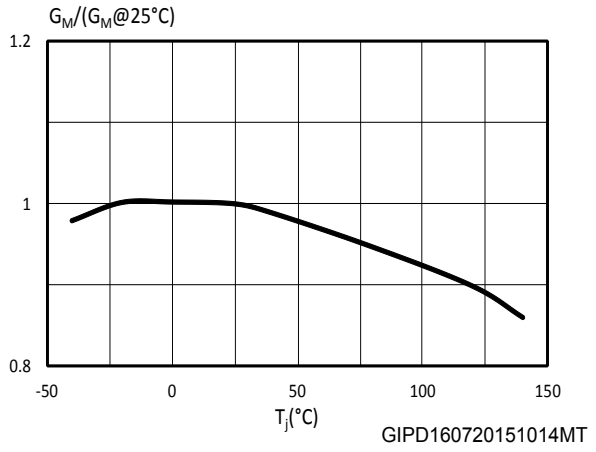


Figure 18. $R_{DS(on)}$ vs T_J

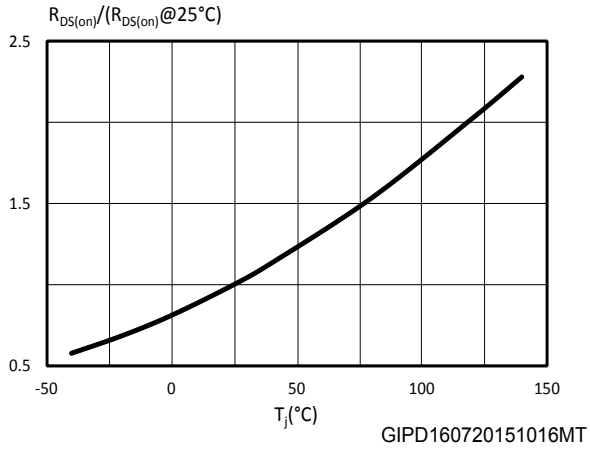


Figure 19. Static drain source on resistance

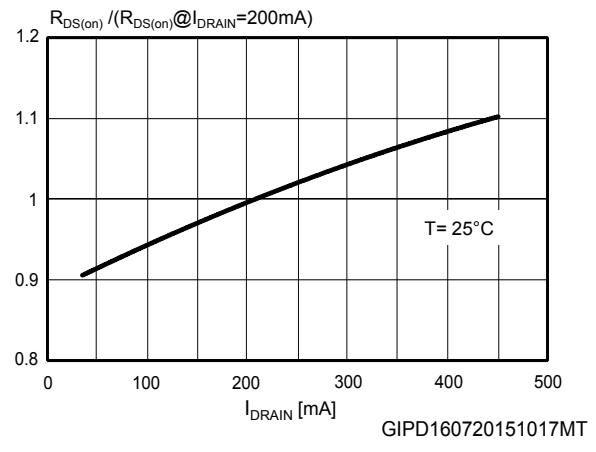


Figure 20. Output characteristic

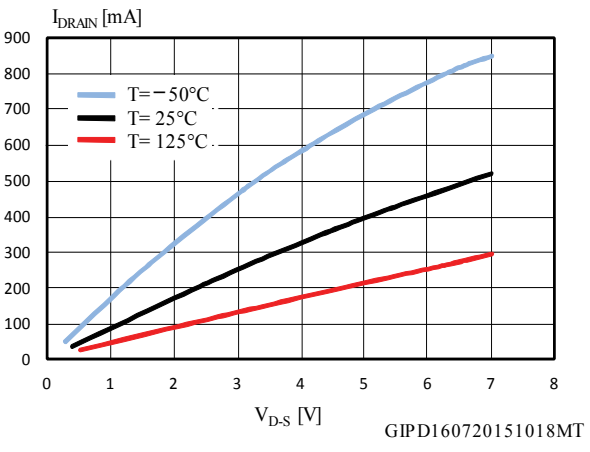


Figure 21. V_{BVDSS} vs T_J

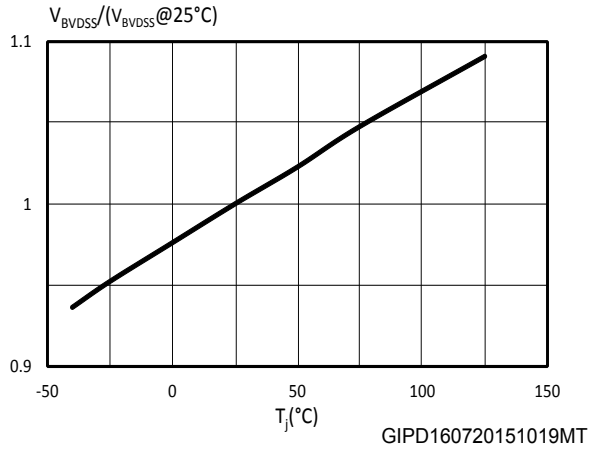


Figure 22. Max avalache energy vs T_J

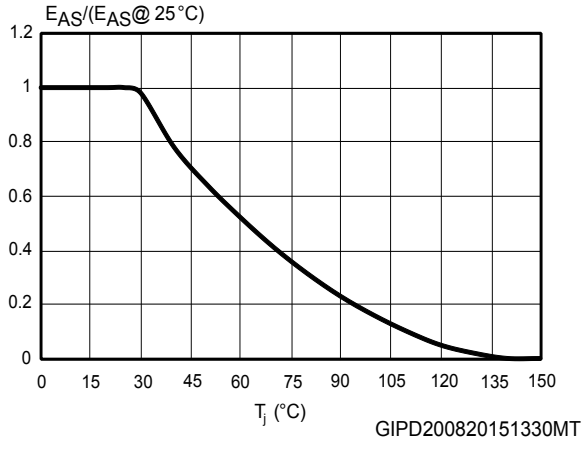
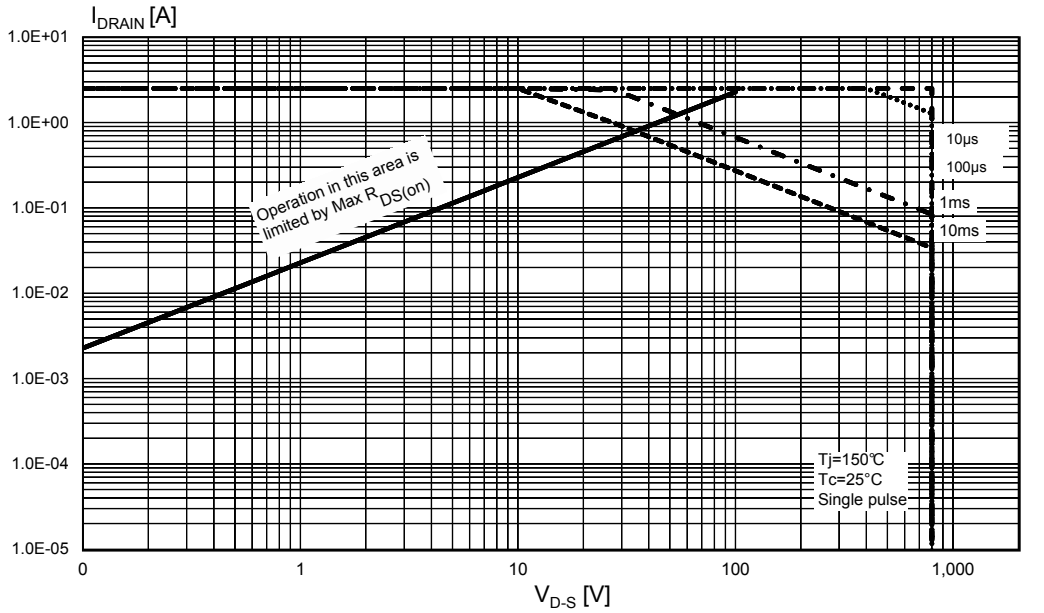


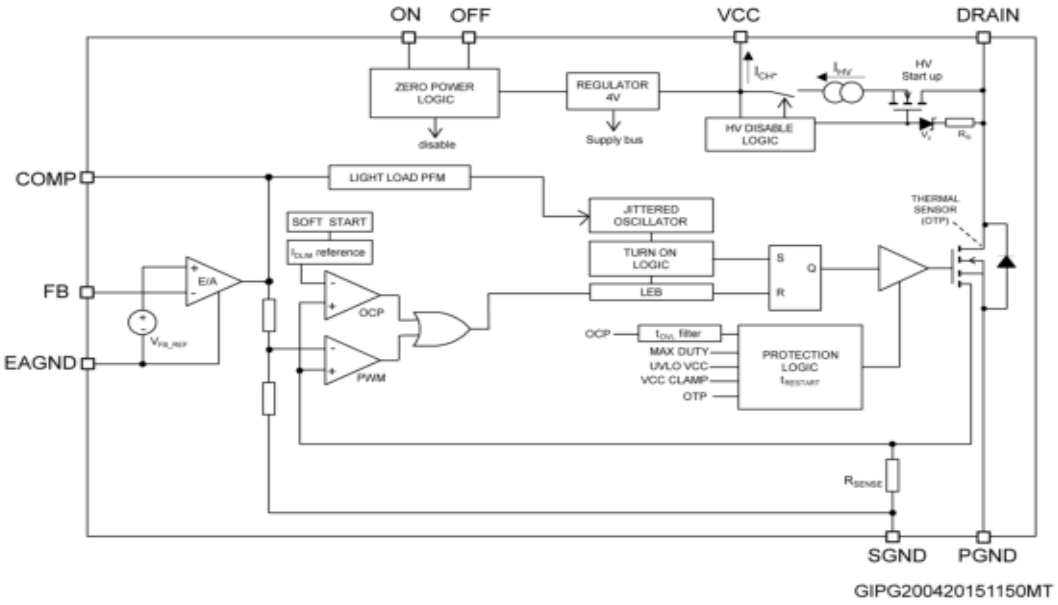
Figure 23. SOA SO16N package



5 General description

5.1 Block diagram

Figure 24. **Block diagram**



5.2 Typical power capability

Table 8. **Typical power**

Vin: 230 V_{AC}		Vin: 85-265 V_{AC}	
Adapter (1)	Open frame (2)	Adapter (1)	Open frame (2)
10 W	12 W	6 W	7 W

1. *Typical continuous power in non-ventilated enclosed adapter measured at 50 °C ambient.*
2. *Maximum practical continuous power in an open frame design at 50 °C ambient, with adequate heatsinking.*

5.3 Primary MOSFET

The primary switch is implemented with an avalanche rugged N-channel MOSFET with minimum breakdown voltage 800 V, V_{BVDSS}, and maximum on-resistance of 20 Ω, $R_{DS(on)}$. The sense-FET is embedded and it allows a virtually lossless current sensing. The startup-MOSFET is embedded and it allows the HV voltage startup operation.

The MOSFET gate driver controls the gate current during both turn-on and turn-off in order to minimize EMI.

5.4 High voltage startup

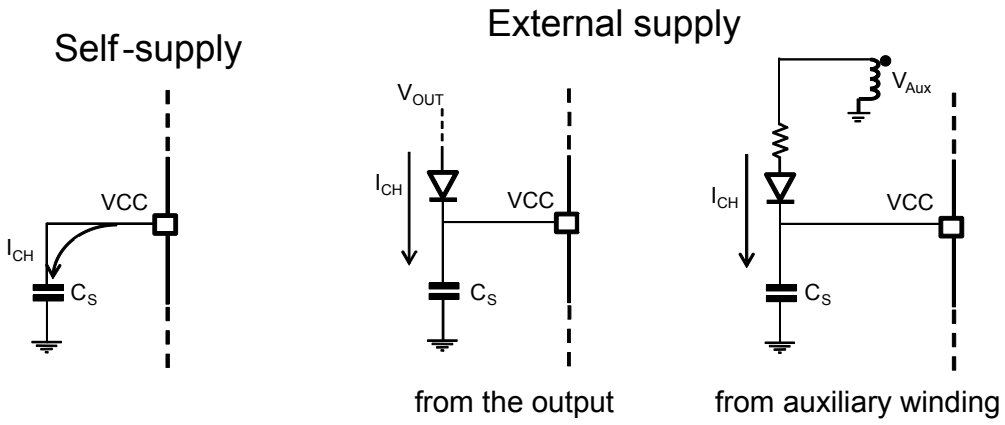
The embedded high voltage startup includes both the 800 V startup FET, whose gate is biased through the resistor R_G, and the switchable HV current source, delivering the current I_{HV}. The major portion of I_{HV}, (I_{CH}), charges the capacitor connected to VCC. A minor portion is sunk by the controller block.

At start up, as the voltage across the DRAIN pin exceeds the V_{HV_START} threshold, the HV current source is turned on, charging linearly the Cs capacitor. At the very beginning of the start-up, when Cs is fully discharged, the charging current is low (I_{CH1} = 1 mA typ.) in order to avoid IC damaging in case VCC is accidentally shorted to SGND. As V_{CC} exceeds 1 V, I_{CH} is increased to I_{CH2} (3.2 mA, typ.) in order to speed up the charging of C_S.

As V_{CC} reaches the startup threshold V_{CCon} (8 V typ.) the chip starts operating, the primary MOSFET is enabled to switch, the HV current source is disabled and the device is powered by the energy stored in the C_S capacitor.

In steady-state the IC supports two different kind of supplies: self-supply and external supply, as shown in Figure 25. IC supply modes: self-supply and external supply.

Figure 25. IC supply modes: self-supply and external supply



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In self-supply only a capacitor C_S is connected to the VCC and the device is supplied by the energy stored in C_S. After the IC startup, due to its internal consumption, the V_{CC} decays to V_{Cson} (4.25 V, typ.) and the HV current source is turned on delivering the current I_{CH3} (7.8 mA typ.) until V_{CC} is recharged to V_{CCon}. The HV current source is reactivated when V_{CC} decays to VCS_{on} again. The I_{CH3} is supplied during the switching OFF time only.

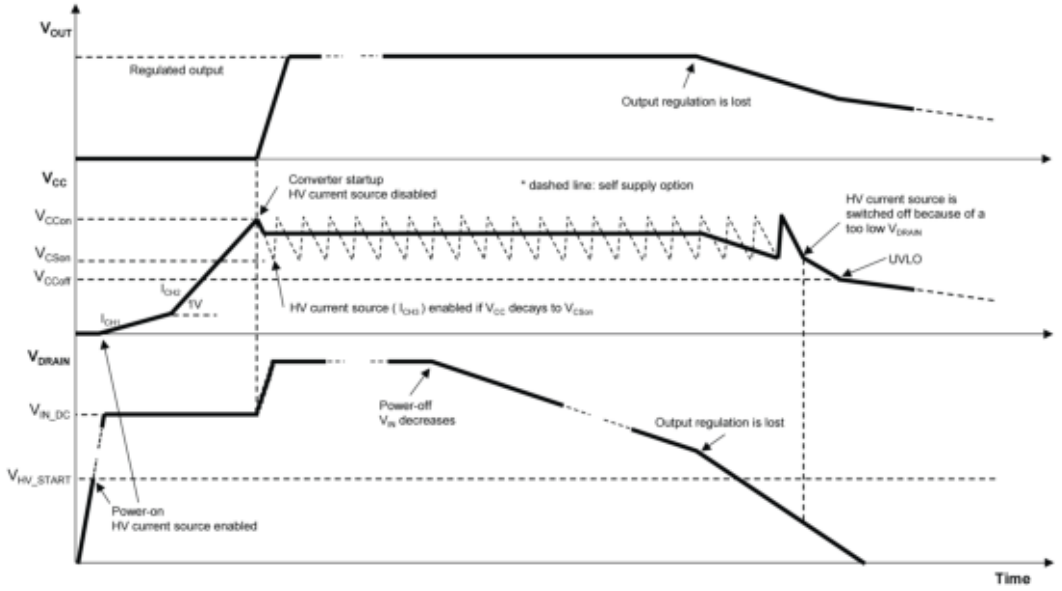
In external supply the HV current source is always kept off by maintaining the V_{CC} above VCS_{on}. This can be obtained through a transformer auxiliary winding or a connection from the output, the latter only in case of non-isolated topology. In this case the residual consumption is given by the power dissipated on R_G, calculated as follows:

$$P_d = \frac{V_{INDC}^2}{R_G}$$

At the nominal input voltage, 230 V_{AC}, the typical consumption (R_G = 34 MΩ) is 3.2 mW and the worst-case consumption (R_G = 28 MΩ) is 3.9 mW.

When the IC is disconnected from the mains, or there is a mains interruption, for some time the converter will keep on working, powered by the energy stored in the input bulk capacitor. When this is discharged below a critical value, the converter is no longer able to keep the output voltage regulated. During the power down, when the DRAIN voltage becomes too low, the HV current source (I_{HV}) remains off and the IC is stopped as soon as the V_{CC} drops below the UVLO threshold, V_{CCoff}.

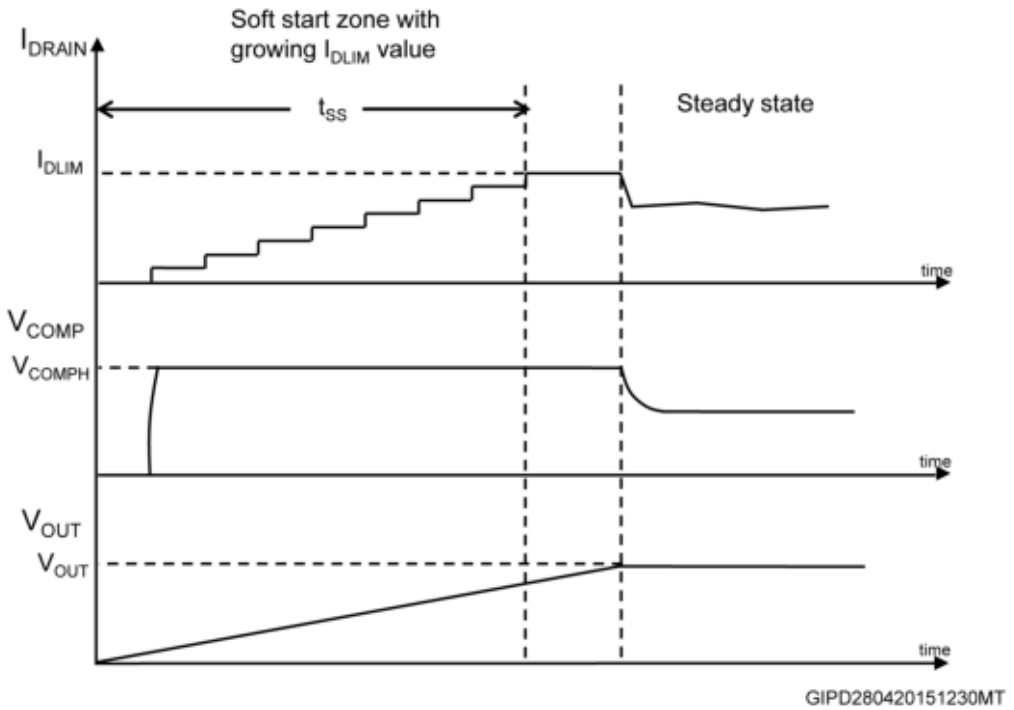
Figure 26. **Power-ON and power-OFF**



5.5 Soft start up

The internal soft-start function of VIPer0P progressively increases the cycle-by-cycle current limitation set point from zero up to I_{DLIM} in 8 steps of 50 mA each. The soft-start time, t_{SS}, is internally set at 8 ms. This function is activated at any attempt of converter start-up and at any restart after a fault event. The feature protects the system at the startup when the output load presents itself like a short-circuit and the converter would work at its maximum drain current limitation.

Figure 27. **Soft startup**



5.6 Oscillator

The IC embeds a fixed frequency oscillator with jittering feature. The switching frequency is modulated by approximately ±7% kHz F_{OSC} at 260 Hz rate. The purpose of the jittering is to get a spread-spectrum action that distributes the energy of each harmonic of the switching frequency over a number of frequency bands, having the same energy on the whole but smaller amplitudes. This helps to reduce the conducted emissions, especially when measured with the average detection method or, which is the same, to pass the EMI tests with an input filter of smaller size with respect to the one that should be needed in absence of jittering feature. Two options with different switching frequencies, F_{OSC}, are available: 60 kHz (L type) and 120 kHz (H type).

5.7 Pulse skipping

The IC embeds a pulse skip circuit that operates in the following way:

- each time the DRAIN peak current exceeds I_{DLIM} level within t_{ON_MIN}, the switching cycle is skipped. The cycles can be skipped until the minimum switching frequency is reached, F_{OSC_MIN} (15 kHz, typ.).
- each time the DRAIN peak current does not exceed I_{DLIM} within t_{ON_MIN}, a switching cycle is restored. The cycles can be restored until the nominal switching frequency is reached, F_{OSC} (60 or 120 kHz, typ.)

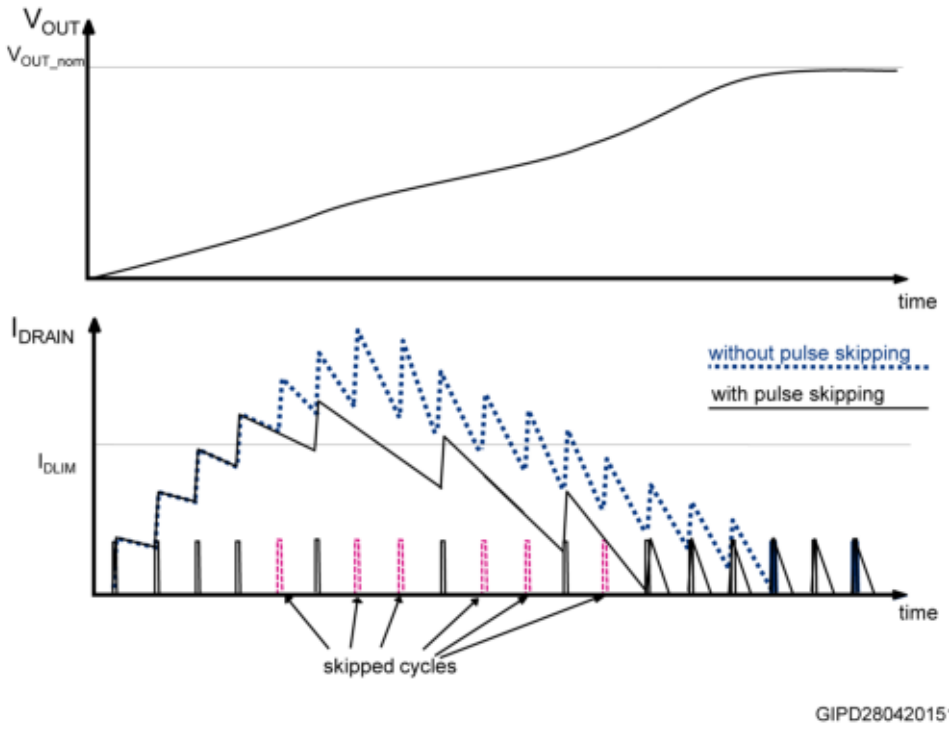
If the converter is indefinitely operated at F_{OSC_MIN}, the IC is turned off after the time t_{OVL_MAX} (200 ms or 400 ms typ., depending on F_{OSC}) and then automatically restarted with soft start phase, after the time $t_{RESTART}$ (1 sec, typ.).

The protection is intended in order to avoid the so called "flux runaway" condition often present at converter startup or in case of a dead-short at converter output and due to the fact that the primary MOSFET, which is turned on by the internal oscillator, cannot be turned off before the minimum on-time.

During the on-time, the inductor is charged through the input voltage and if it cannot be discharged by the same amount during the off-time, in every switching cycle there is a net increase of the average inductor current, that can reach dangerously high values until the output capacitor is not charged enough to ensure the inductor discharge rate needed for the volt-second balance. This condition is common at converter startup, because of the low output voltage.

In the following Figure 28. Pulse skipping during start-up for F_{OSC} = 60 kHz the effect of pulse skipping feature on the DRAIN peak current shape is shown (solid line), compared with the DRAIN peak current shape when pulse skipping feature is not implemented (dashed line). Providing more time for cycle-by-cycle inductor discharge when needed, this feature is effective in keeping low the maximum DRAIN peak current avoiding the flux runaway condition.

Figure 28. **Pulse skipping during start-up for F_{OSC} = 60 kHz**



5.8 Direct feedback

The IC embeds a transconductance type error amplifier (E/A) whose inverting input, ground reference and output are FB, EAGND and COMP, respectively. The internal reference voltage of the E/A is V_{FB_REF} (1.2 V typical value referred to EAGND). In non-isolated topologies this makes it possible to tightly regulate positive output voltages through a simple voltage divider applied among the output voltage terminal, FB and EAGND, and soldering SGND to EAGND. Since EAGND can float down to -12.5 V with respect to the ground of the IC (SGND), negative output voltages can be regulated as well, connecting EAGND to the negative rail, and the voltage divider among FB, EAGND and SGND, as shown in Figure 34. Negative output flyback converter (non-isolated).

The E/A output is scaled down and fed into the PWM comparator, where it is compared to the voltage across the sense resistor in series to the sense-FET, thus setting the cycle-by-cycle drain current limitation.

An R-C network connected on the output of the E/A (COMP) is usually used to stabilize the overall control loop.

The FB is provided with an internal pull-up to prevent a wrong IC behavior when the pin is accidentally left floating.

5.9 Secondary feedback

When a secondary feedback is required, the internal E/A has to be disabled shorting FB to EAGND (V_{FB} < V_{FB_DIS}). With this setting COMP is internally connected to a pre-regulated voltage through the pull-up resistor $R_{COMP(DYN)}$, (65 kΩ, typ.) and the voltage across COMP is set by the current sunk.

This allows the output voltage value to be set through an external error amplifier (TL431 or similar) placed on the secondary side, whose error signal is used to set the DRAIN peak current setpoint corresponding to the output power demand. If isolation is required, the error signal must be transferred through an optocoupler, with the phototransistor collector connected across COMP and SGND.

5.10 Pulse frequency modulation

If the output load is decreased, the feedback loop reacts lowering the V_{COMP} voltage, which reduces the DRAIN peak current setpoint, down to the minimum value of I_{DLIM_PFM} when the V_{COMPL} threshold is reached.

If the load is further decreased, the DRAIN peak current value is maintained at I_{DLIM_PFM} and some PWM cycles are skipped. This mode of operation is referred to as “pulse frequency modulation” (PFM), the number of the skipped cycles depends on the balance between the output power demand and the power transferred from the

input. The result is an equivalent switching frequency which can go down to some hundreds Hz, thus reducing all the frequency-related losses.

This kind of operation, together with the extremely low IC quiescent current, allows very low input power consumption in no load and light load, while the low DRAIN peak current value, I_{DLIM_PFM}, prevents any audible noise which could arise from low switching frequency values. When the load is increased, V_{COMP} increases and PFM is exited. V_{COMP} reaches its maximum at V_{COMPH} and corresponding to that value, the DRAIN current limitation (I_{DLIM}) is reached.

5.11 Zero power mode

The zero-power mode (ZPM) is a special idle state of VIPer0P, characterized by the following features:

- there is no switching activity, then neither voltage nor power, available at the output
- the HV current source charges V_{CC} at 13 V and does not perform its usual functions
- all IC circuits, except the ones needed to exit ZPM, are turned off, reducing the controller consumption to very low values

The IC enters ZPM if OFF is forced to SGND for more than t_{DEB_OFF} (10 ms, typ.), the IC exits ZPM if ON is forced to SGND for a more than t_{DEB_ON} (20 µs, typ.).

The ZPM can be managed manually or by a microcontroller (MCU) or in mixed mode. In case of mixed ZPM management (see Figure 29. ZPM managed in mixed mode) the MCU supervising the operation of the appliance shuts down the SMPS by pulling low OFF through one of its GPIOs, cutting also its own supply voltage. The restart is commanded by a pushbutton or a tactile switch pressed by the user that directly operates pin ON. For safety reasons, this switch should operate at low voltage (SELV level). The MCU wakes up after the SMPS is again up and running. This arrangement provides the minimum consumption from the power line.

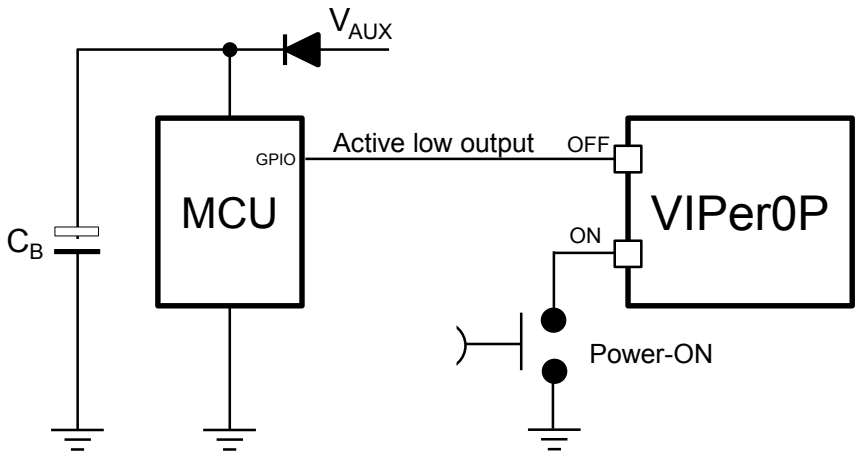
In case of ZPM management by MCU only (see Figure 30. ZPM fully managed by MCU) the MCU shuts down the SMPS by pulling low OFF and wakes it up as well by pulling low ON. Two of its GPIOs are used. The MCU is powered also during ZPM using the resistive pull-up available at ON (R_{ON}, 45 kΩ typical), provided that it is rated for 3.3 V supply voltage, and equipped with an ultra-low consumption Standby Mode.

Since in ZPM the device is supplied with extremely low current, it is naturally prone to pick up noise. If the device is required to work in a noisy environment, it is recommended to connect a film capacitor (tens to some hundreds pF) across ON and OFF versus SGND. If the device is disconnected from the mains or there is a mains interruption while in ZPM, the information in the logic is lost. When the input source is applied again, the IC will be restarted in normal mode.

The ultimate aim of ZPM function is to enable the realization of PSUs able to comply with the European regulation 1275/2008 as far as the standby and off-mode power consumption of appliances is concerned. To meet this target a careful system-level design is required.

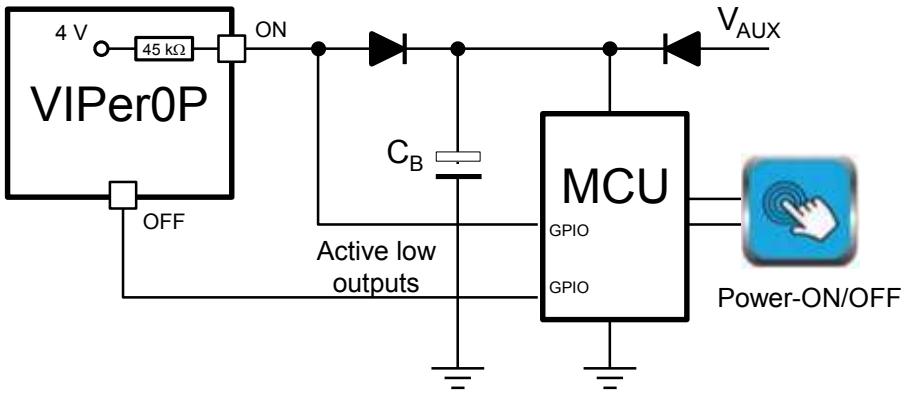
The total input consumption is therefore reduced to the residual consumption lower than 4 mW at 230 V_{AC} that can be rounded to zero based on the IEC62301 that sets to 10 mW the minimum accuracy of the standby power measurements.

Figure 29. **ZPM managed in mixed mode**



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Figure 30. **ZPM fully managed by MCU**



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5.12 Overload protection (OLP)

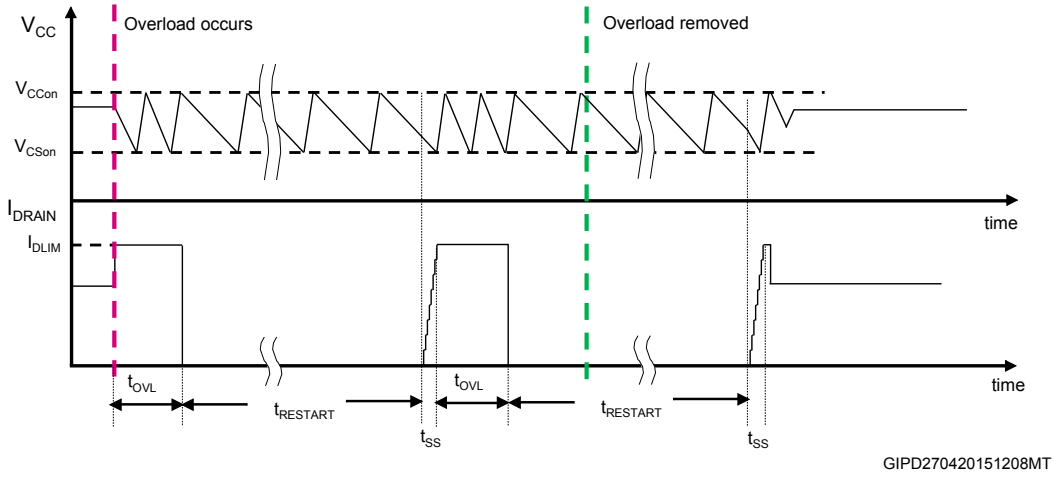
In order to manage the overload condition the IC embeds the following main blocks: the OCP comparator to turn off the power MOSFET when the drain current reaches its limit (I_{DLIM}), the up and down OCP counter to define the turn off delay time in case of continuous overload (t_{OVL} = 50 ms typ.) and the timer to define the restart time after protection tripping ($t_{RESTART}$ = 1 sec, typ.).

In case of short-circuit or overload, the control level on the inverting input of the PWM comparator is greater than the reference level fed into the inverting input of the OCP comparator. As a result, the cycle-by-cycle turn off of the power switch will be triggered by the OCP comparator instead of by the PWM comparator. Every cycle this condition is met, the OCP counter is incremented and if the fault condition persists for a time greater than t_{OVL} (corresponding to the counter end-of-count), the protection is tripped, the PWM is disabled for $t_{RESTART}$, then it resumes switching with soft-start and, if the fault is still present, it is disabled again after t_{OVL}. The OLP management prevents that the IC could be indefinitely operated at I_{DLIM} and the low repetition rate of the restart attempts of the converter avoids overheating the IC in case of repeated fault events.

After the fault removal, the IC resumes working normally. If the fault is removed before the protection tripping (before t_{OVL}), the t_{OVL}-counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped. If the fault is removed during $t_{RESTART}$, the IC waits for that the $t_{RESTART}$ period has elapsed before resuming switching.

In fault condition the V_{CC} ranges between V_{CSon} and V_{CCon} levels, due to the periodical activation of the HV current source recharging the V_{CC} capacitor.

Figure 31. **Overload condition**



5.13 Max. duty cycle counter protection

The IC embeds a max duty-cycle counter, which disables the PWM if the MOSFET is turned off by max duty cycle (70% min, 80% max) for ten consecutive switching cycles. After protection tripping, the PWM is stopped for $t_{RESTART}$ and then activated again with soft-start phase until the fault condition is removed.

In some cases (i.e. breaking of the loop) even if V_{COMP} is saturated high, the OLP cannot be triggered because at every switching cycle the PWM is turned off by maximum duty cycle before the DRAIN peak current can reach the I_{DLIM} setpoint. As a result, the output voltage V_{OUT} could increases out of control and be maintained indefinitely at much higher value than nominal one with risk for the output capacitor, the output diode and the IC itself. The max duty cycle counter protection prevents this kind of failures.

5.14 V_{CC} clamp protection

This protection can be invoked when the IC is supplied by auxiliary winding or diode from the output voltage, when an output over-voltage produces an increase of V_{CC}.

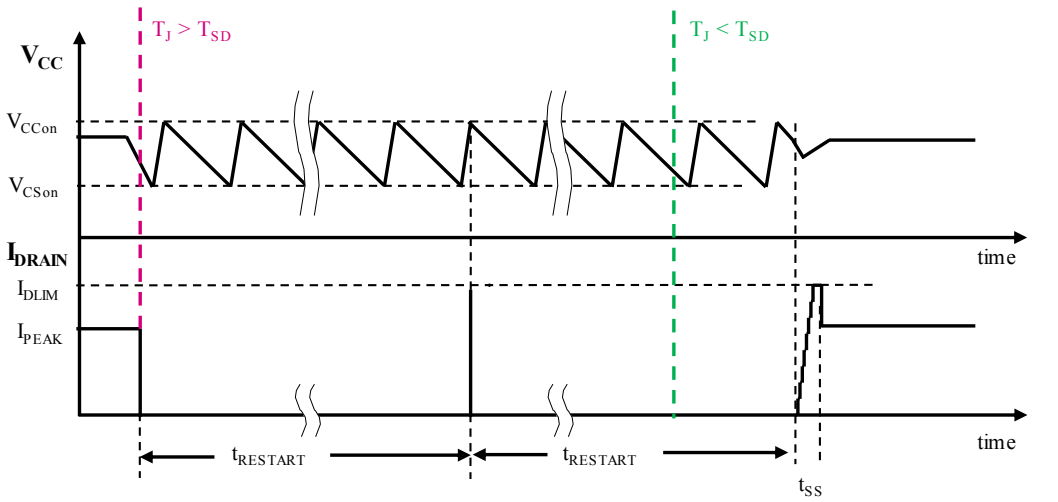
If V_{CC} reaches the clamp level $V_{CCclamp}$ (30 V, min. referred to EAGND) the current injected into the pin is monitored and if it exceeds the internal threshold I_{clamp_max} (30 mA, typ.) for more than t_{clamp_max} (5 ms, typ.), the PWM is disabled for $t_{RESTART}$ (1 sec, typ.) and then activated again with soft-start phase. The protection is disabled during the soft-start time.

5.15 Thermal shutdown

If the junction temperature becomes higher than the internal threshold T_{SD} (160 °C, typ.), the PWM is disabled. After $t_{RESTART}$ time, a single switching cycle is performed, during which the temperature sensor embedded in the Power MOSFET section is checked. If a junction temperature above T_{SD} is still measured, the PWM is maintained disabled for $t_{RESTART}$ time, otherwise it resumes switching with soft-start phase.

During $t_{RESTART}$ V_{CC} is maintained between V_{CSon} and V_{CCon} levels by the HV current source periodical activation. Such a behavior is summarized in Figure 32. Thermal shutdown timing diagram.

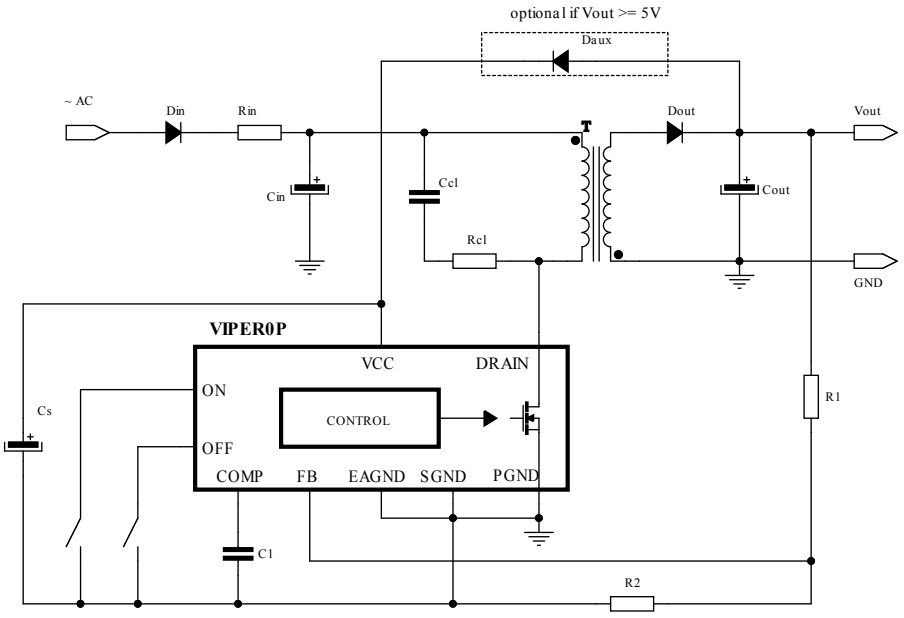
Figure 32. **Thermal shutdown timing diagram**



6 Application information

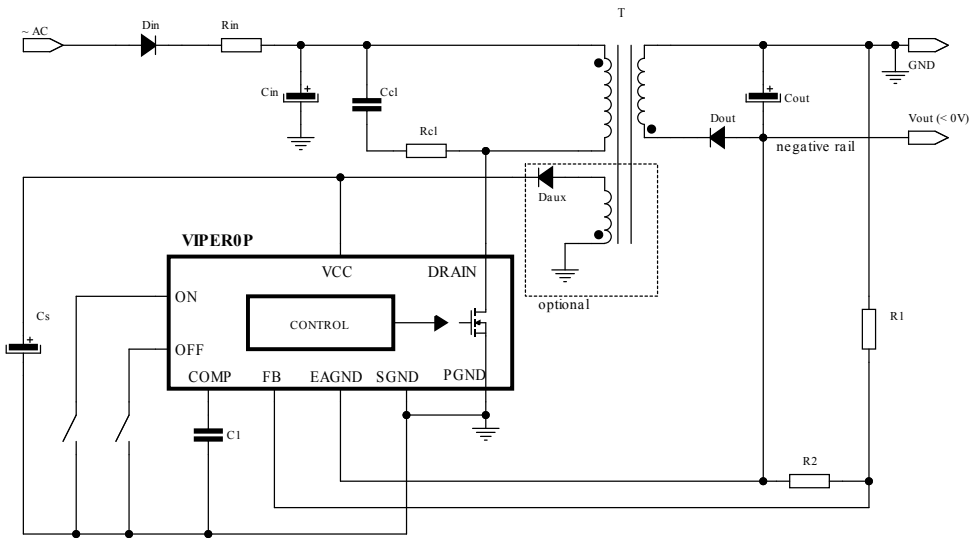
6.1 Typical schematics

Figure 33. **Flyback converter (non-isolated)**



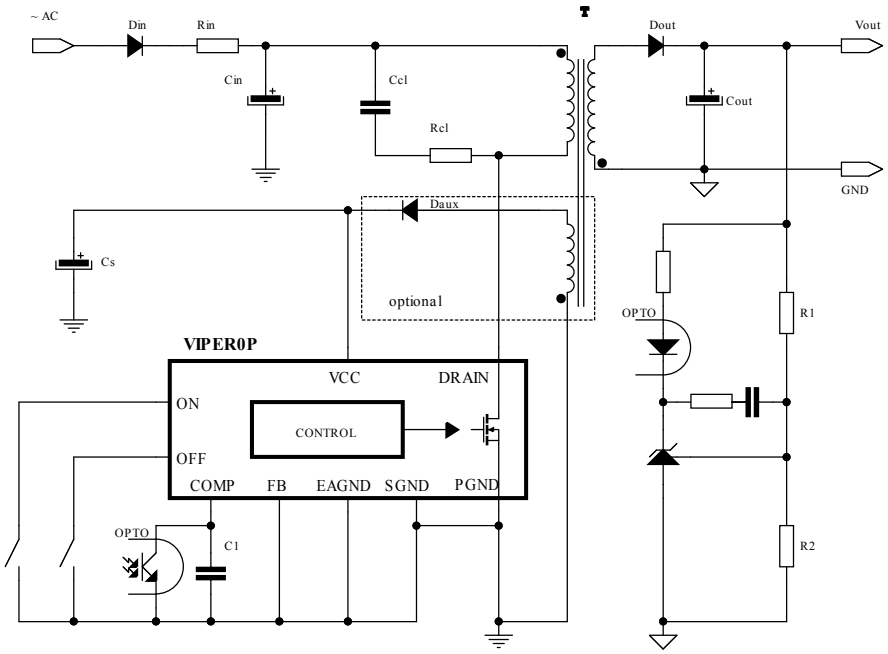
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Figure 34. **Negative output flyback converter (non-isolated)**



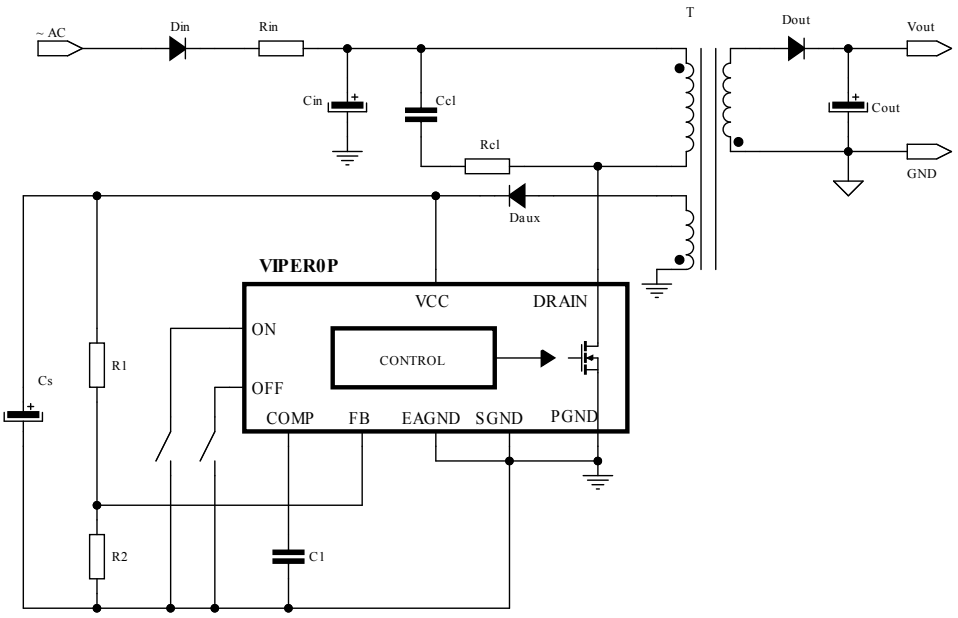
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Figure 35. **Isolated flyback converter with secondary feedback**



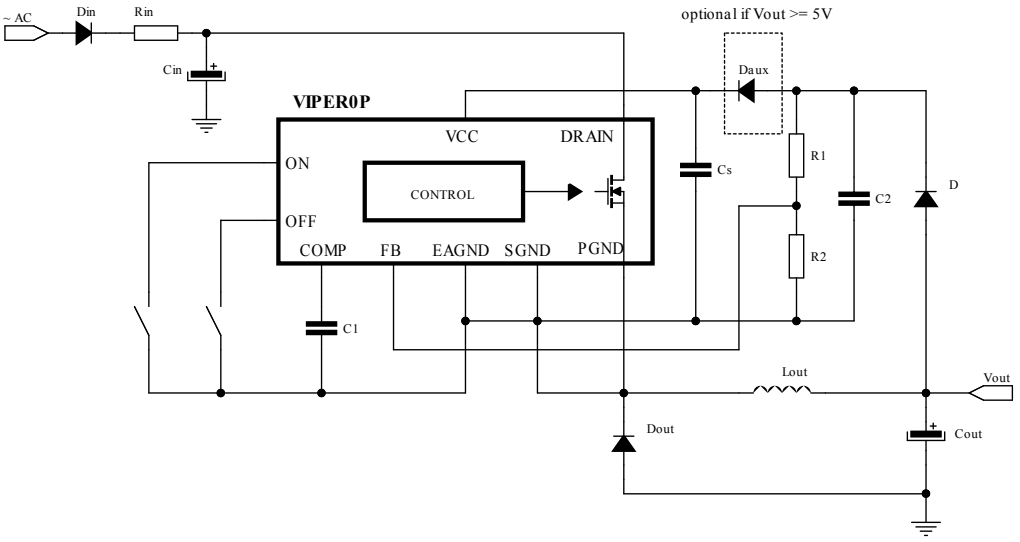
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Figure 36. **Primary side regulation isolated flyback converter**



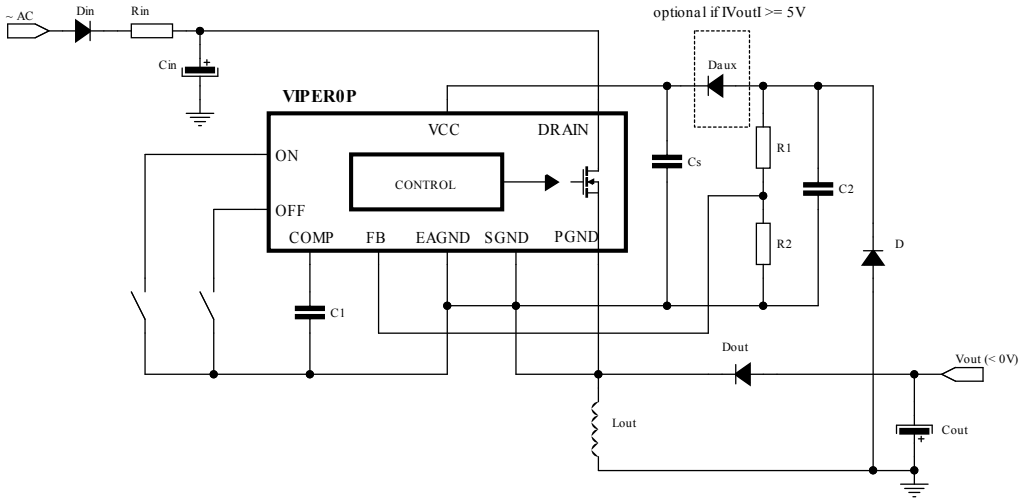
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Figure 37. **Buck converter (positive output)**



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Figure 38. **Buck-boost converter (negative output)**

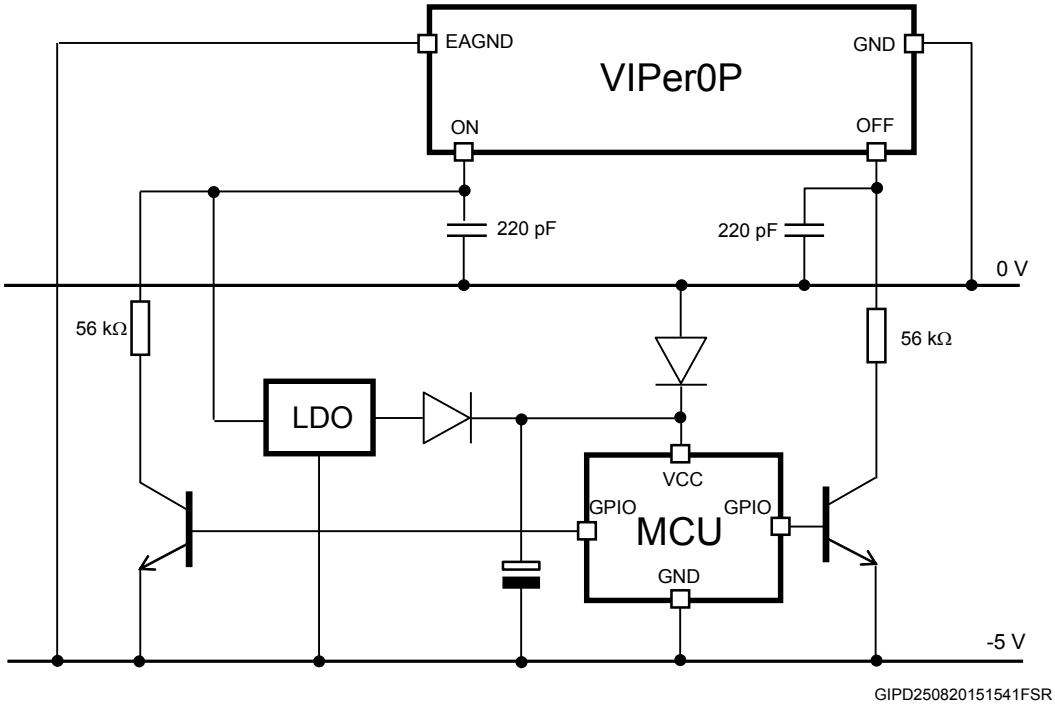


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6.2 Example of ZPM management using MCU

Sometimes the SMPS provides a -5 V bus for instance to enable triac driving to control the motor of a washing machine. In this case, not to generate an additional +5 V bus, the ground of the MCU can be connected to the -5 V bus and its positive supply voltage to the ground of SMPS and VIPer0P. This connection requires an interface circuit realizing a level shifting to properly drive ON and OFF, like the one shown in the Figure 39. Example of interfacing the VIPer0P to a MCU supplied from a negative rail . During ZPM the MCU is supplied through ON, but a linear regulator is needed in between, in order to avoid that during normal operation the AMR of the MCU is exceeded.

Figure 39. **Example of interfacing the VIPer0P to a MCU supplied from a negative rail**



6.3 Energy saving performances

VIPer0P allows designing applications compliant with the most stringent energy saving regulations. In order to show the typical performances achievable, the active mode average efficiency and the efficiency at 10% of the rated output power of a single output flyback converter using VIPer0P have been measured and are reported in Table 9. In addition, ZPM, no-load and light load consumptions are shown in the below tables and Figure 40. P_{IN} versus V_{IN} in ZPM and no load and Figure 41. P_{IN} versus V_{IN} in light load.

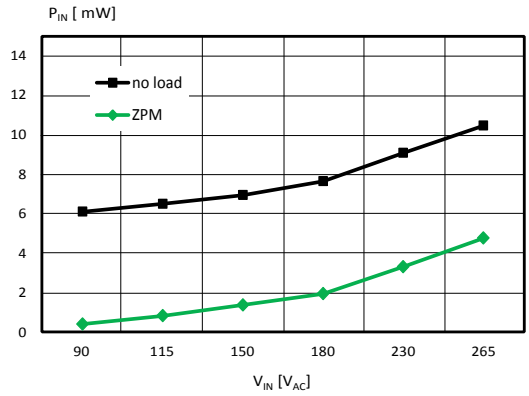
Table 9. **Power supply efficiency, V_{OUT} = 12 V**

V_{IN}	10% output load efficiency [%]	Active mode average efficiency [%]
115 V_{AC}	78.0	80.9
230 V_{AC}	71.1	81.0

Table 10. **Input power consumption**

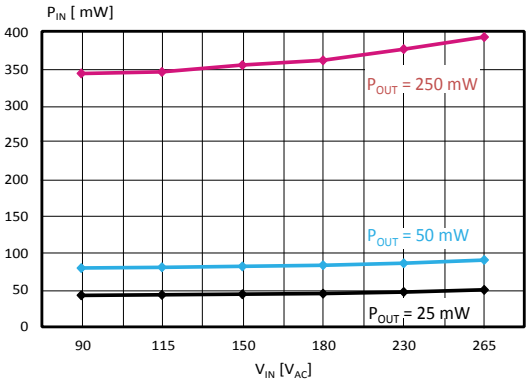
V_{IN}	P_{IN} in ZPM [mW]	P_{IN} @ no-load [mW]
115 V_{AC}	0.8	6.5
230 V_{AC}	3.3	9.0

Figure 40. P_{IN} versus V_{IN} in ZPM and no load



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Figure 41. P_{IN} versus V_{IN} in light load



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6.4 Layout guidelines and design recommendations

A proper printed circuit board layout is essential for correct operation of any switch-mode converter and this is true for the VIPer0P as well. The main reasons to have a proper PCB layout are:

- Provide clean signals to the IC, ensuring good immunity against external noises and switching noises
- Reduce the electromagnetic interferences, both radiated and conducted, to pass more easily the EMC

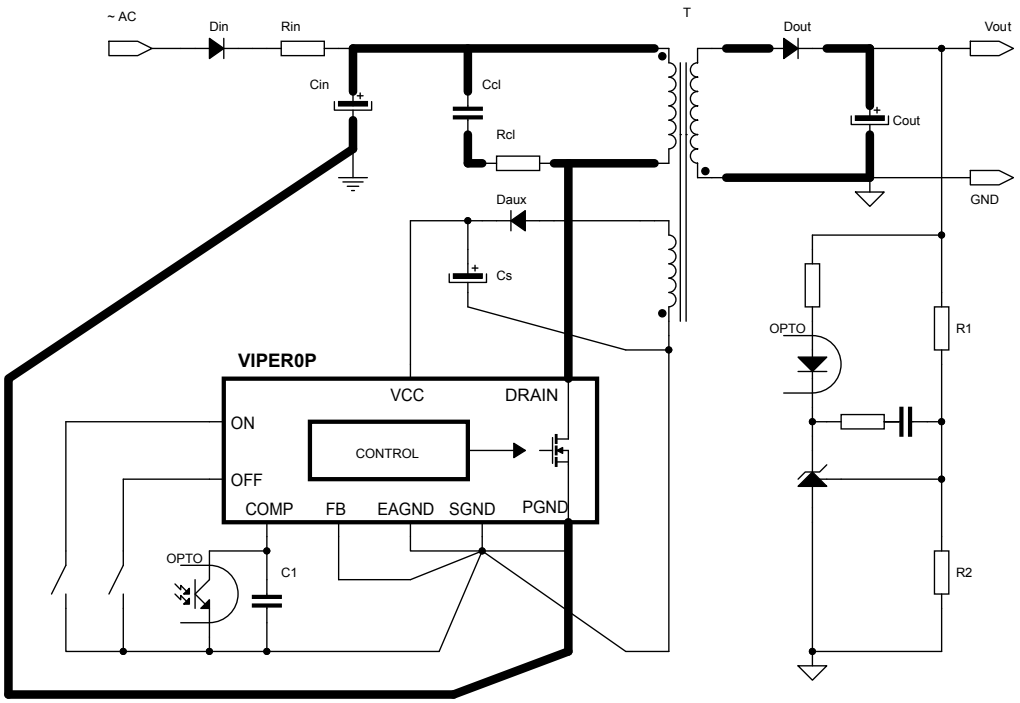
When designing a SMPS using VIPer0P, the following basic rules should be considered:

- **Separating signal from power tracks:** generally, traces carrying signal currents should run far from others carrying pulsed currents or with quickly swinging voltages. Signal ground traces should be connected to the IC signal ground, SGND, using a single "star point", placed close to the IC. Power ground traces should be connected to the IC power ground, PGND. SGND and PGND are then to be connected to each other with the shortest track as possible. The compensation network should be connected to the COMP, maintaining the trace to SGND as short as possible. In case of two layer PCB, it is a good practice to route signal traces on one PCB side and power traces on the other side.
- **Filtering sensitive pins:** some crucial points of the circuit need or may need filtering. A small high-frequency bypass capacitor to SGND might be useful to get a clean bias voltage for the signal part of the IC and protect the IC itself during EFT/ESD tests. A low ESL ceramic capacitor (a few hundreds pF up to 0.1 µF) should be connected across VCC and SGND, placed as close as possible to the IC. With flyback topologies, when the auxiliary winding is used, it is suggested to connect the VCC capacitor on the auxiliary return and then to the main GND using a single track. In case of nosy environment, it is strongly recommended to filter ON and OFF with small ceramic capacitors (tens to hundreds pF) connected to SGND, in order to improve the system noise immunity.
- **Keep power loops as confined as possible:** minimize the area circumscribed by current loops where high pulsed currents flow, in order to reduce its parasitic self-inductance and the radiated electromagnetic field: this will greatly reduce the electromagnetic interferences produced by the power supply during the switching. In a flyback converter the most critical loops are: the one including the input bulk capacitor, the power switch,

the power transformer, the one including the snubber, the one including the secondary winding, the output rectifier and the output capacitor. In a buck converter the most critical loop is the one including the input bulk capacitor, the power switch, the power inductor, the output capacitor and the free-wheeling diode.

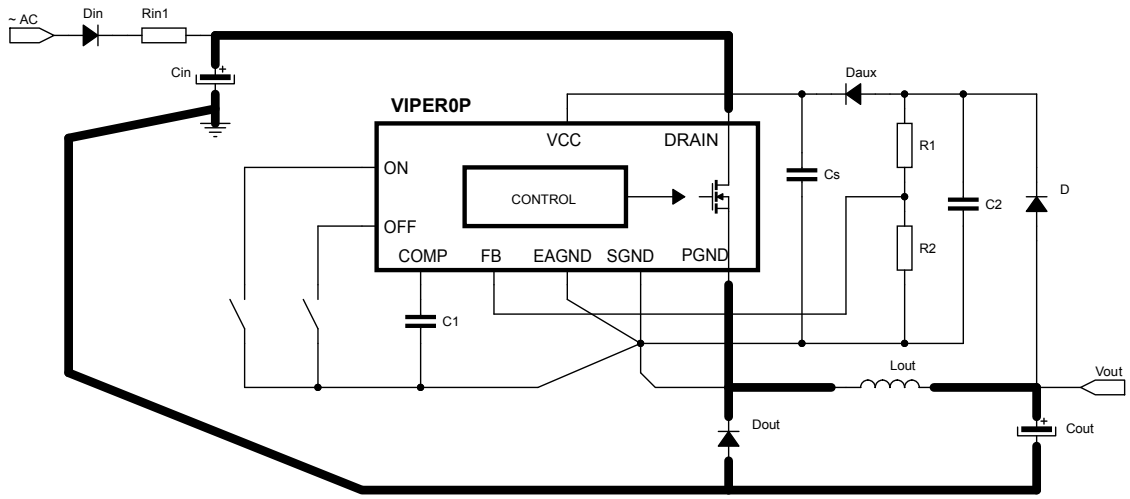
- **Reduce line lengths:** any wire will act as an antenna. With the very short rise times exhibited by EFT pulses, any antenna has the capability of receiving high voltage spikes. By reducing line lengths, the level of radiated energy that is received will be reduced, and the resulting spikes from electrostatic discharges will be lower. This will also keep both resistive and inductive effects to a minimum. In particular, all of traces carrying high currents, especially if pulsed (tracks of the power loops) should be as short and fat as possible.
- **Optimize track routing:** as levels of pickup from static discharges are likely to be greater closer to the extremities of the board, it is wise to keep any sensitive lines away from these areas. Input and output lines will often need to reach the PCB edge at some stage, but they can be routed away from the edge as soon as possible where applicable. Since vias are to be considered inductive elements, it is recommended to minimize their number in the signal path and avoid them when designing the power path.
- **Improve thermal dissipation:** an adequate copper area has to be provided under the DRAIN pins as heat sink, while it is not recommended to place large copper areas on the SGND and PGND.

Figure 42. Recommended routing for flyback converter



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Figure 43. **Recommended routing for buck converter**



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7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

7.1 SO16N package information

Figure 44. SO16N package outline

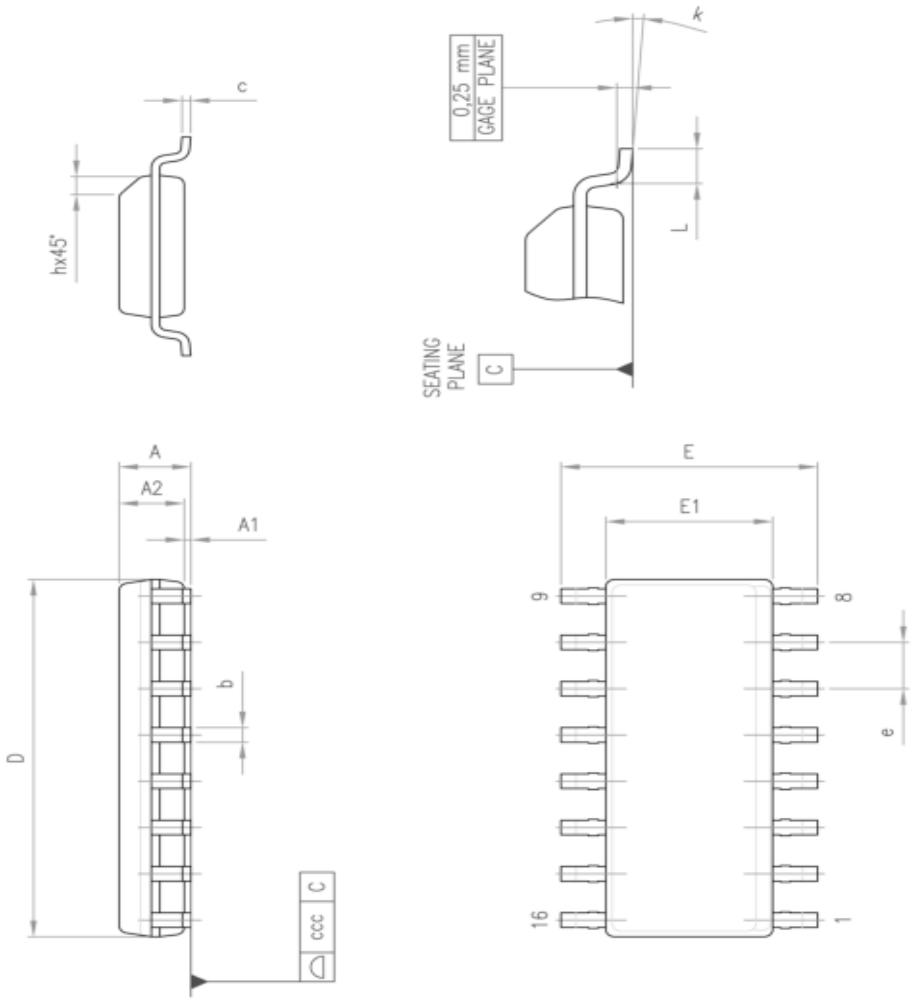


Table 11. **SO16N mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.1		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.8	9.9	10
E	5.8	6	6.2
E1	3.8	3.9	4
e		1.27	
h	0.25		0.5
L	0.4		1.27
k	0		8
ccc			0.1

8 Ordering information

Table 12. **Order codes**

Order code	Package	Packing	F_{OSC} ± jitter
VIPER0PLD	SO16N	Tube	60 kHz ±7%
VIPER0PHD			120 kHz ±7%
VIPER0PLDTR		Tape and reel	60 kHz ±7%
VIPER0PHDTR			120 kHz ±7%

Revision history

Table 13. **Document revision history**

Date	Revision	Changes
18-Aug-2015	1	Initial release
12-Apr-2016	2	Updated Table 4: "Avalanche characteristics", Table 6: "Supply section" and Table 7: "Controller section".Minor text changes.
01-Oct-2018	3	Updated V_{OFF} and V_{ON} values in Table 7. Controller section

Contents

1 **Description** 2
2 **Pin setting** 3
3 **Electrical and thermal ratings** 4
3.1 Electrical characteristics 5
4 **Typical electrical characteristics** 8
5 **General description** 12
5.1 Block diagram 12
5.2 Typical power capability 12
5.3 Primary MOSFET 12
5.4 High voltage startup 12
5.5 Soft startup 14
5.6 Oscillator 15
5.7 Pulse skipping 15
5.8 Direct feedback 16
5.9 Secondary feedback 16
5.10 Pulse frequency modulation 16
5.11 Zero-power mode 17
5.12 Overload protection (OLP) 18
5.13 Max. duty cycle counter protection 19
5.14 VCC clamp protection 19
5.15 Thermal shutdown 19
6 **Application information** 21
6.1 Typical schematics 21
6.2 Example of ZPM management using MCU 23
6.3 Energy saving performances 24
6.4 Layout guidelines and design recommendations 25
7 **Package information** 28
7.1 SO16N package information 28
8 **Ordering information** 30

Revision history 31

List of tables

Table 1. Pin description . . . 3
Table 2. Absolute maximum ratings . . . 4
Table 3. Thermal data . . . 4
Table 4. Avalanche characteristics . . . 4
Table 5. Power section . . . 5
Table 6. Supply section . . . 6
Table 7. Controller section . . . 6
Table 8. Typical power . . . 12
Table 9. Power supply efficiency, V_{OUT} = 12 V . . . 24
Table 10. Input power consumption . . . 24
Table 11. SO16N mechanical data . . . 29
Table 12. Order codes . . . 30
Table 13. Document revision history . . . 31

List of figures

Figure 1. Basic application schematic . . . 1
Figure 2. Connection diagram . . . 3
Figure 3. I_{DLIM} vs T_J . . . 8
Figure 4. I_{ON} vs V_{ON} . . . 8
Figure 5. F_{OSC} vs T_J . . . 8
Figure 6. V_{HV_START} vs T_J . . . 8
Figure 7. V_{FB_REF} vs T_J . . . 8
Figure 8. Quiescent current I_q vs T_J . . . 8
Figure 9. Operating current I_{CC} vs T_J . . . 9
Figure 10. I_{COMP} vs T_J . . . 9
Figure 11. I_{CH1} vs T_J . . . 9
Figure 12. I_{CH1} vs V_{DRAIN} . . . 9
Figure 13. I_{CH2} vs T_J . . . 9
Figure 14. I_{CH2} vs V_{DRAIN} . . . 9
Figure 15. I_{CH3} vs T_J . . . 10
Figure 16. I_{CH3} vs V_{DRAIN} . . . 10
Figure 17. G_M vs T_J . . . 10
Figure 18. $R_{DS(on)}$ vs T_J . . . 10
Figure 19. Static drain source on resistance . . . 10
Figure 20. Output characteristic . . . 10
Figure 21. V_{BVDSS} vs T_J . . . 11
Figure 22. Max avalache energy vs T_J . . . 11
Figure 23. SOA SO16N package . . . 11
Figure 24. Block diagram . . . 12
Figure 25. IC supply modes: self-supply and external supply . . . 13
Figure 26. Power-ON and power-OFF . . . 14
Figure 27. Soft startup . . . 14
Figure 28. Pulse skipping during start-up for F_{OSC} = 60 kHz . . . 16
Figure 29. ZPM managed in mixed mode . . . 18
Figure 30. ZPM fully managed by MCU . . . 18
Figure 31. Overload condition . . . 19
Figure 32. Thermal shutdown timing diagram . . . 20
Figure 33. Flyback converter (non-isolated) . . . 21
Figure 34. Negative output flyback converter (non-isolated) . . . 21
Figure 35. Isolated flyback converter with secondary feedback . . . 22
Figure 36. Primary side regulation isolated flyback converter . . . 22
Figure 37. Buck converter (positive output) . . . 23
Figure 38. Buck-boost converter (negative output) . . . 23
Figure 39. Example of interfacing the VIPer0P to a MCU supplied from a negative rail . . . 24
Figure 40. P_{IN} versus V_{IN} in ZPM and no load . . . 25
Figure 41. P_{IN} versus V_{IN} in light load . . . 25
Figure 42. Recommended routing for flyback converter . . . 26
Figure 43. Recommended routing for buck converter . . . 27
Figure 44. SO16N package outline . . . 28

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