STP9N80K5, STW9N80K5

N-channel 800 V, 0.73 Ω typ., 7 A MDmesh™ K5 Power MOSFETs in a TO-220 and TO-247 packages

Datasheet - production data

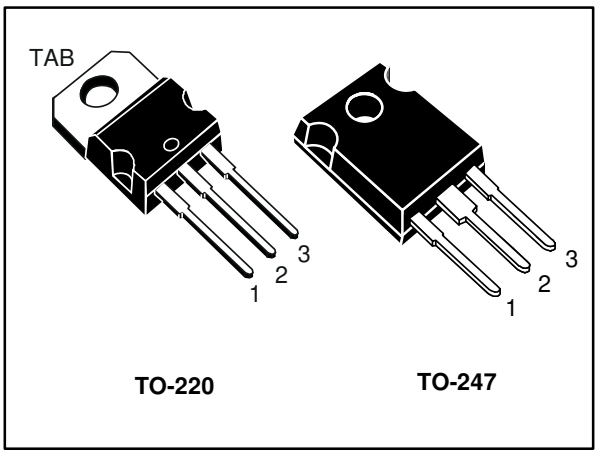
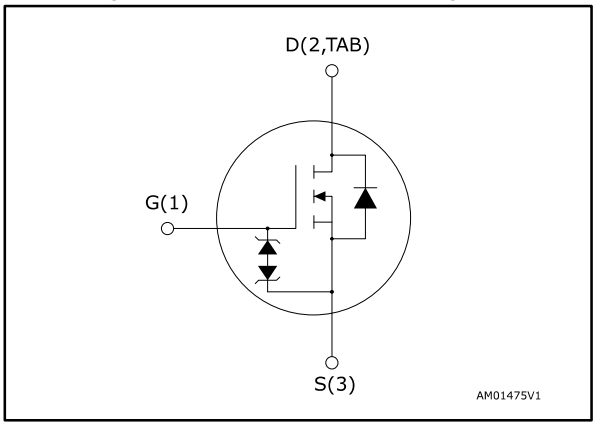


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STP9N80K5	800 V	0.90 Ω	7 A
STW9N80K5			

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFET are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STP9N80K5	9N80K5	TO-220	Tube
STW9N80K5		TO-247	

This is information on a product in full production. www.st.com

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at T_C= 25 °C	7	A
I_D	Drain current (continuous) at T_C = 100 °C	4.4	A
I_D (1)	Drain current (pulsed)	28	A
P_{TOT}	Total dissipation at T_C = 25 °C	110	W
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	
T_J	Operating unction temperature range	- 55 to 150	°C
T_{stg}	Storage temperature range		

Notes:

(1)Pulse width limited by safe operating area.

(2)I_{SD} ≤ 7 A, di/dt≤ 100 A/µs; V_{DS} peak < $V_{(BR)DSS}$,V_{DD}= 640 V

(3)V_{DS} ≤ 640 V

Table 3: Thermal data

Symbol	Parameter	Value		Unit
		TO-220	TO-247	
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.14		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	50	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by Tjmax)	2.4	A
E_{AS}	Single pulse avalanche energy (starting Tj = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	200	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	800			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 800 V			1	µA
		V_{GS} = 0 V, V_{DS} = 800 V T_C = 125 °C(1)			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 3.5 A		0.73	0.90	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	340	-	pF
C_{oss}	Output capacitance		-	37	-	pF
C_{rss}	Reverse transfer capacitance		-	0.65	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0 V, V_{DS} = 0 to 640 V	-	61	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related			22		pF
R_g	Intrinsic gate resistance	f = 1 MHz open drain	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 640 V, I_D = 7 A V_{GS}= 10 V See (*Figure 16: "Test circuit for gate charge behavior"*)	-	12	-	nC
Q_{gs}	Gate-source charge		-	3.8	-	nC
Q_{gd}	Gate-drain charge		-	6.7	-	nC

Notes:

(1)$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as Coss while V_{DS} is rising from 0 to 80% V_{DSS}.

(2)$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as Coss while V_{DS} is rising from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}= 400 V, I_D =3.5 A, R_G = 4.7 Ω V_{GS} = 10 V See (*Figure 15: "Test circuit for resistive load switching times"* and *Figure 20: "Switching time waveform"*)	-	11	-	ns
t_r	Rise time		-	5.7	-	ns
$t_{d(off)}$	Turn-off delay time		-	65.3	-	ns
t_f	Fall time		-	13.6	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7	A
I_{SDM}(1)	Source-drain current (pulsed)		-		28	A
V_{SD}(2)	Forward on voltage	I_{SD} = 7 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 7 A, di/dt = 100 A/µs, V_{DD} = 60 V See *Figure 17: "Test circuit for inductive load switching and diode recovery times"*	-	292		ns
Q_{rr}	Reverse recovery charge		-	2.66		µC
I_{RRM}	Reverse recovery current		-	18.2		A
t_{rr}	Reverse recovery time	I_{SD} = 7 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C See *Figure 17: "Test circuit for inductive load switching and diode recovery times"*	-	477		ns
Q_{rr}	Reverse recovery charge		-	3.91		µC
I_{RRM}	Reverse recovery current		-	16.4		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS}= ± 1mA,I_D= 0 A	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

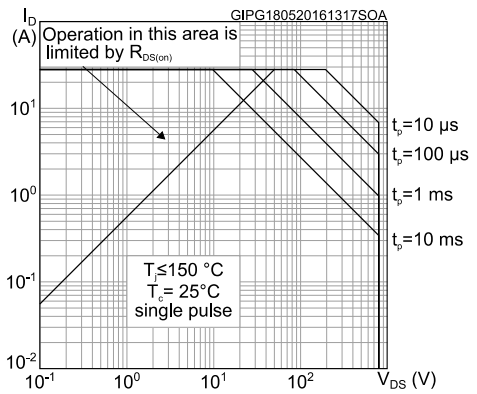


Figure 3: Thermal impedance

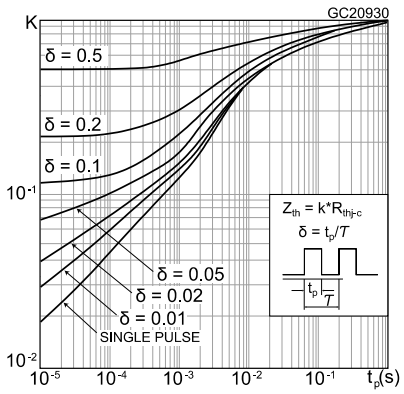


Figure 4: Output characteristics

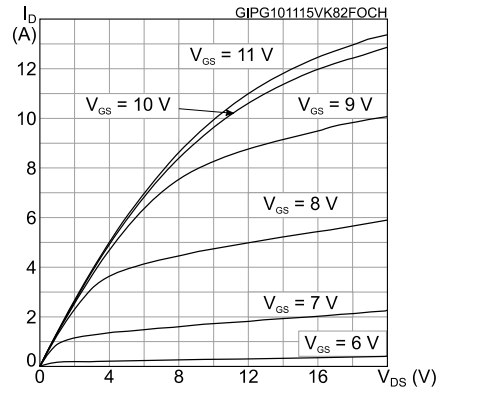


Figure 5: Transfer characteristics

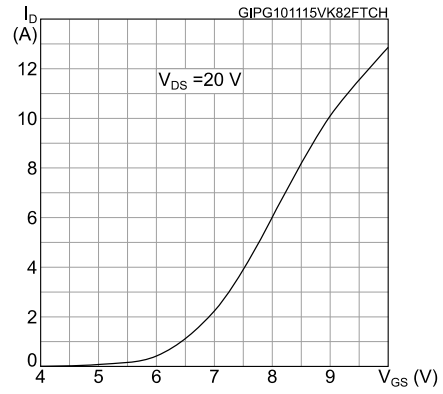


Figure 6: Gate charge vs gate-source voltage

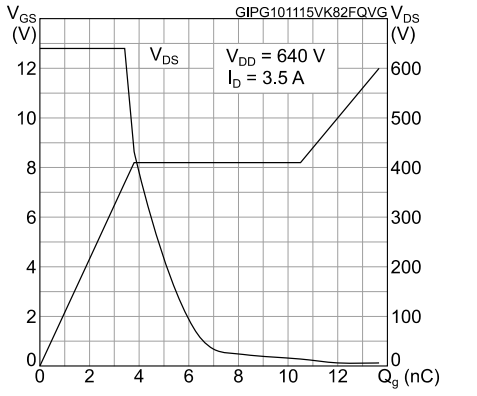


Figure 7: Static drain-source on-resistance

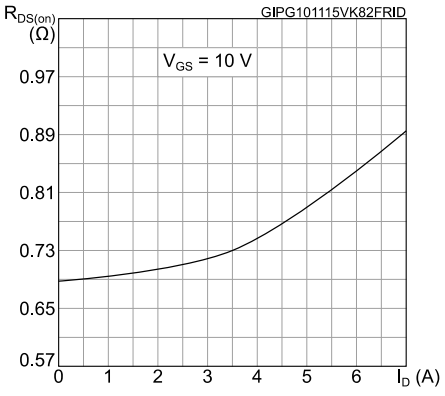


Figure 8: Capacitance variations

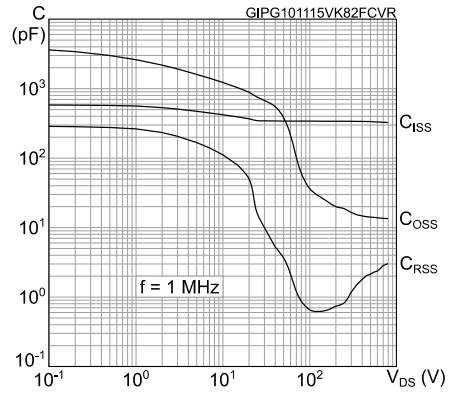


Figure 9: Normalized gate threshold voltage vs temperature

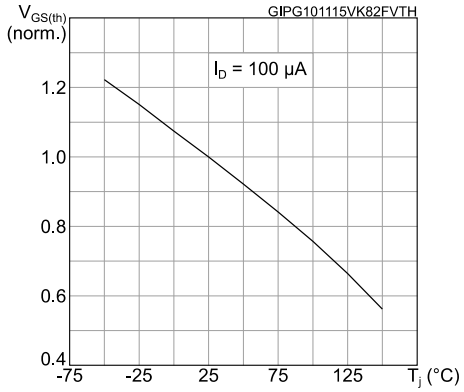


Figure 10: Normalized on-resistance vs temperature

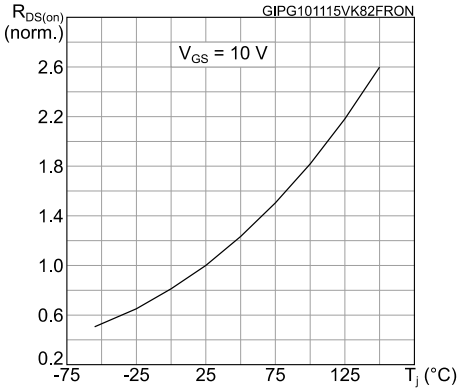


Figure 11: Normalized V(BR)DSS vs temperature

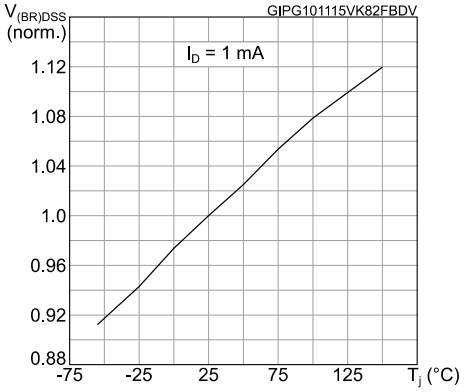


Figure 12: Output capacitance stored energy

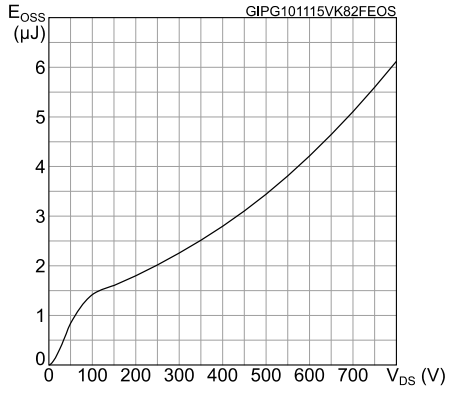


Figure 13: Source-drain diode forward characteristics

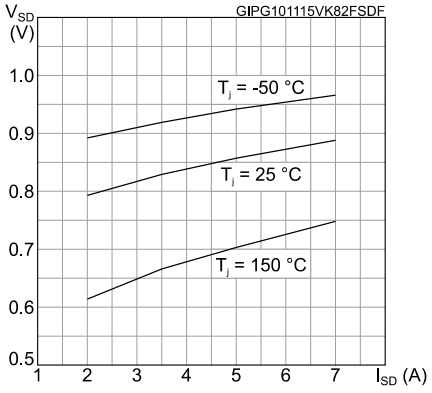
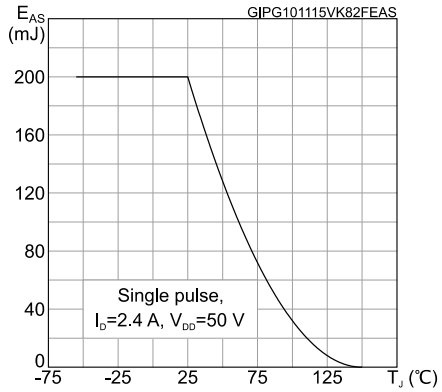


Figure 14: Maximum avalanche energy vs starting TJ



3 Test circuits

Figure 15: Test circuit for resistive load switching times

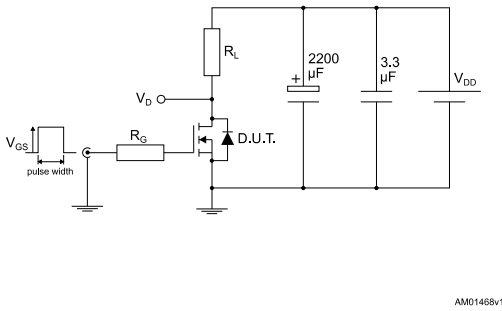


Figure 16: Test circuit for gate charge behavior

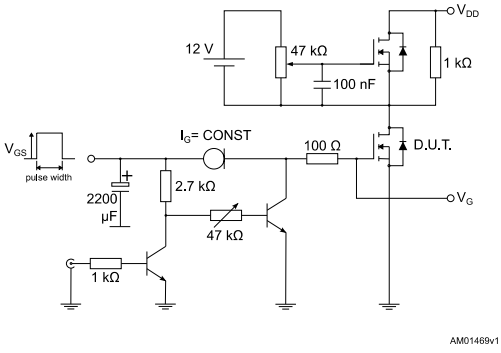


Figure 17: Test circuit for inductive load switching and diode recovery times

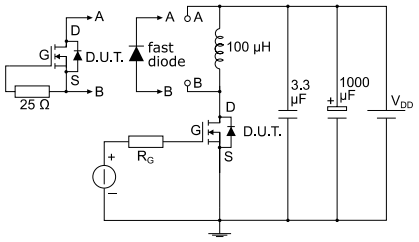


Figure 18: Unclamped inductive load test circuit

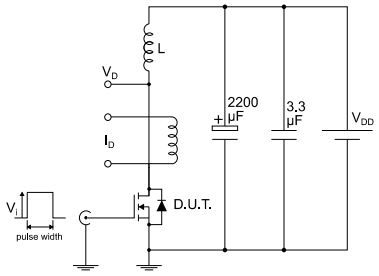


Figure 19: Unclamped inductive waveform

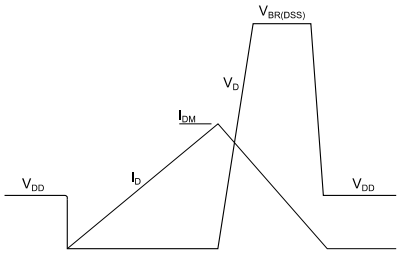
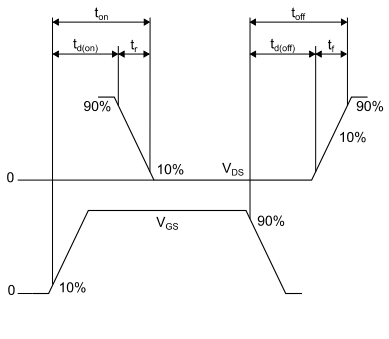


Figure 20: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-220 type A package information

Figure 21: TO-220 type A package outline

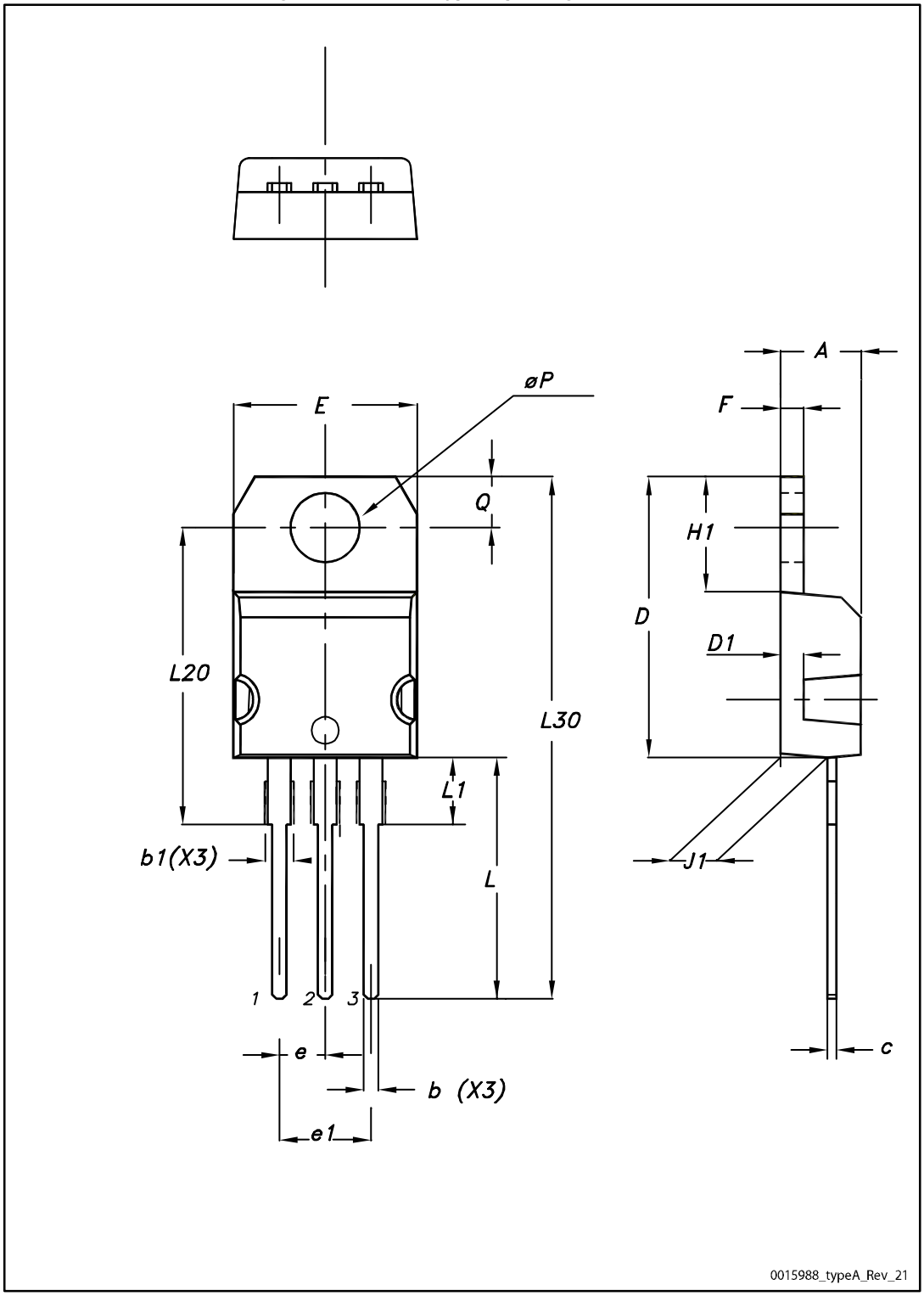


Table 10: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.2 TO-247 package information

Figure 22: TO-247 package outline

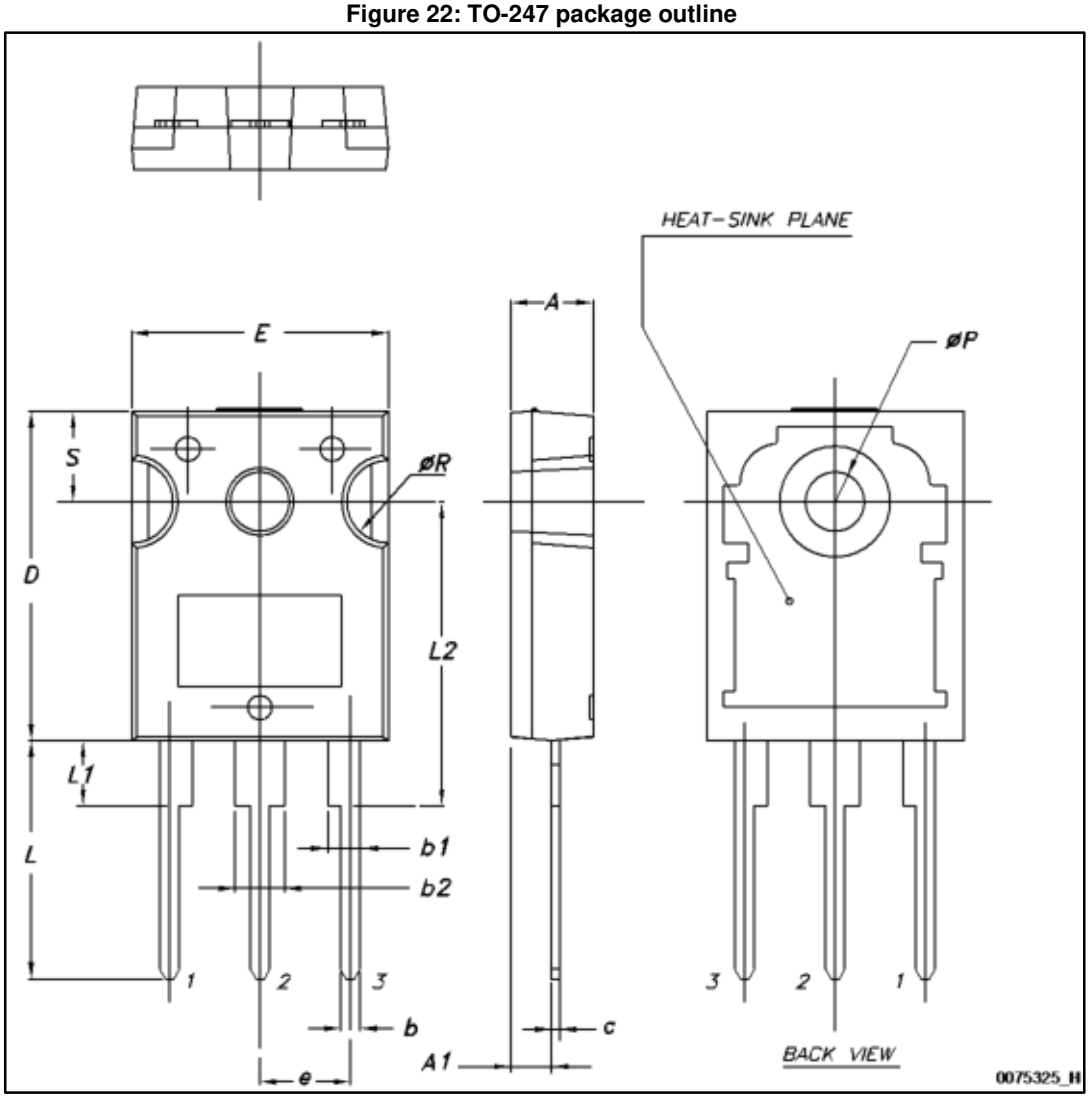


Table 11: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 12: Document revision history

Date	Revision	Changes
13-Oct-2015	1	First release.
20-May-2016	2	Modified: *Table 4: "Avalanche characteristics"*, *Table 6: "Dynamic"*, *Table 7: "Switching times"* and *Table 8: "Source-drain diode"*. Minor text changes
26-Jul-2016	3	Updated features in cover page.

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