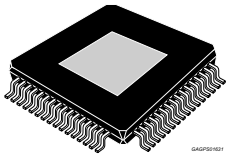
FDA801

4 x 50 W class-D digital input power amplifier with I^{2}C diagnostics and low voltage operation

Data brief



LQFP64 (exposed pad up)

Features

- Integrated 110 dB D/A conversion
- I^{2}S and TDM digital input (3.3/1.8 V)
- Input sampling frequency: 44.1 kHz, 48 kHz, 96 kHz, 192 kHz
- Class-D channels with 93% efficiency
- EMI control for AM compatibility
- EMI compliance evaluated following normative IEC61967-4 and IEC62132-4
- Low radiation function (LRF)
- Idle tones free DAC
- Output lowpass filter included in the feedback allowing lower cost filter components
- Max. output power
  - 4 x 50 W/4 Ω @ 15.2 V, 1 kHz
- High output power capability
  - 28 W/4 Ω 10 % THD, Vd = 14.4 V
- Full I^{2}C bus driving (3.3/1.8 V):
  - Channels independent tristate
  - Channel independent soft play/mute
  - I^{2}C bus diagnostics, including DC and AC load detection
- Integrated fault protection
- Input and output offset detector
- Clipping detector
- ESD protection
- 6 V operation (“Start - Stop” engines compatibility)
- 2 and 1 Ω load driving capability

Description

FDA801 is a new BCD technology quad BRIDGE class D amplifier, specially intended for automotive applications.

Thanks to the technology used, it is possible to integrate a high performance D/A converter together with powerful MOSFET outputs in class D, to get an outstanding efficiency compared with the standard class AB.

The integrated D/A converter allows to reach outstanding performances (110 dB S/N ratio with 108 dB of dynamic range). The feedback loop includes the output L-C low-pass filter, allowing superior frequency response linearity and lower distortion independently from the inductor and capacitor quality.

FDA801 is fully configurable through I^{2}C bus interface and integrates a full diagnostics array specially intended for automotive applications. Thanks to the solutions implemented to contain EMI emissions, the device is intended to be used in the standard single DIN car-radio box together with the tuner.

Moreover FDA801 is able to work with power supply as low as 6 V, thus supporting the most recent low voltage ('start-stop') car-makers specification.

Table 1. Device summary

Order code	Package	Packing
FDA801-VYY	LQFP64 (exp. pad up)	Tray
FDA801-VYT	LQFP64 (exp. pad up)	Tape & Reel

For further information contact your local STMicroelectronics sales office. www.st.com

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1 Block diagram and pins description

Figure 1. Block diagram

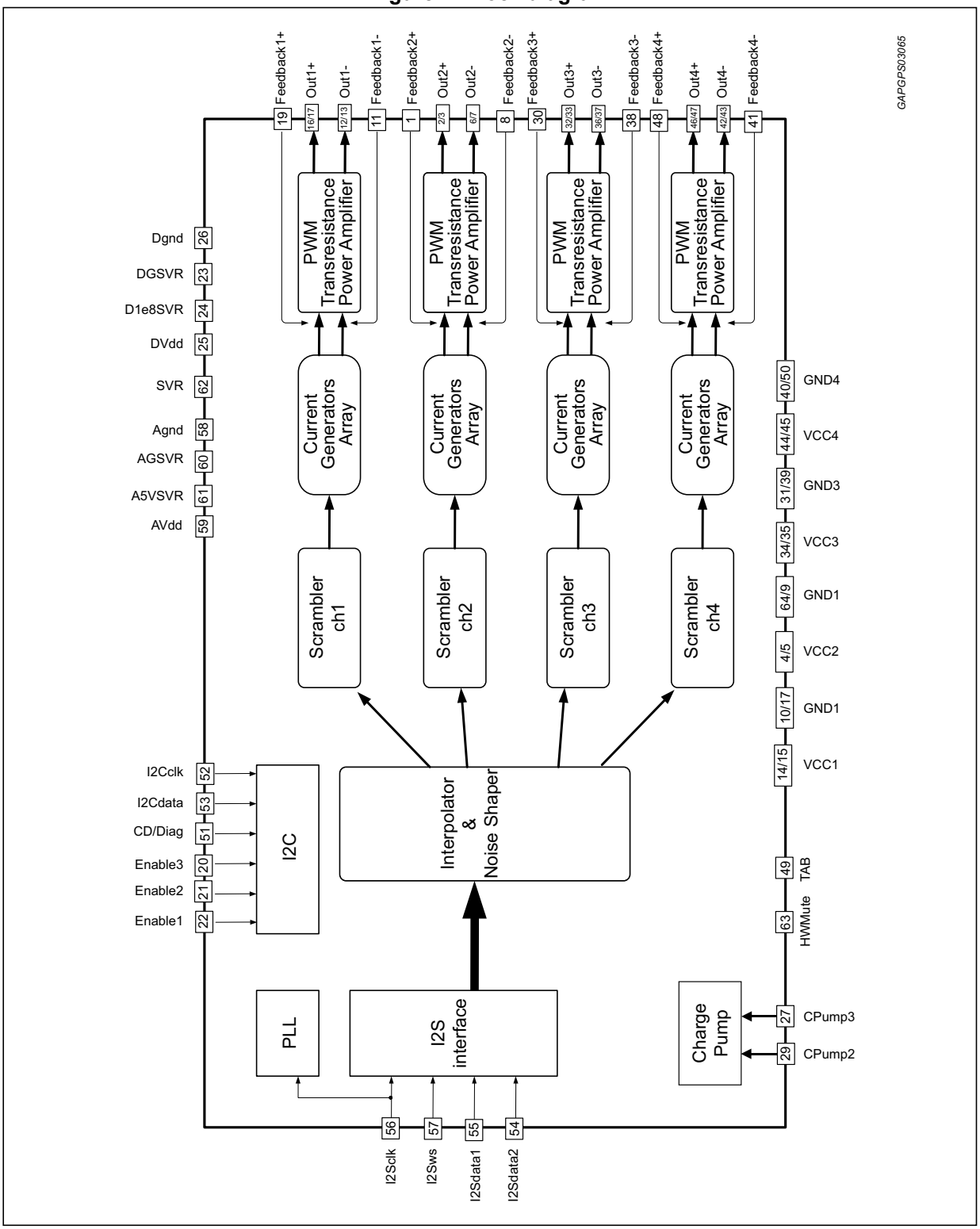


Figure 2. Tentative pins connection diagram (top view)

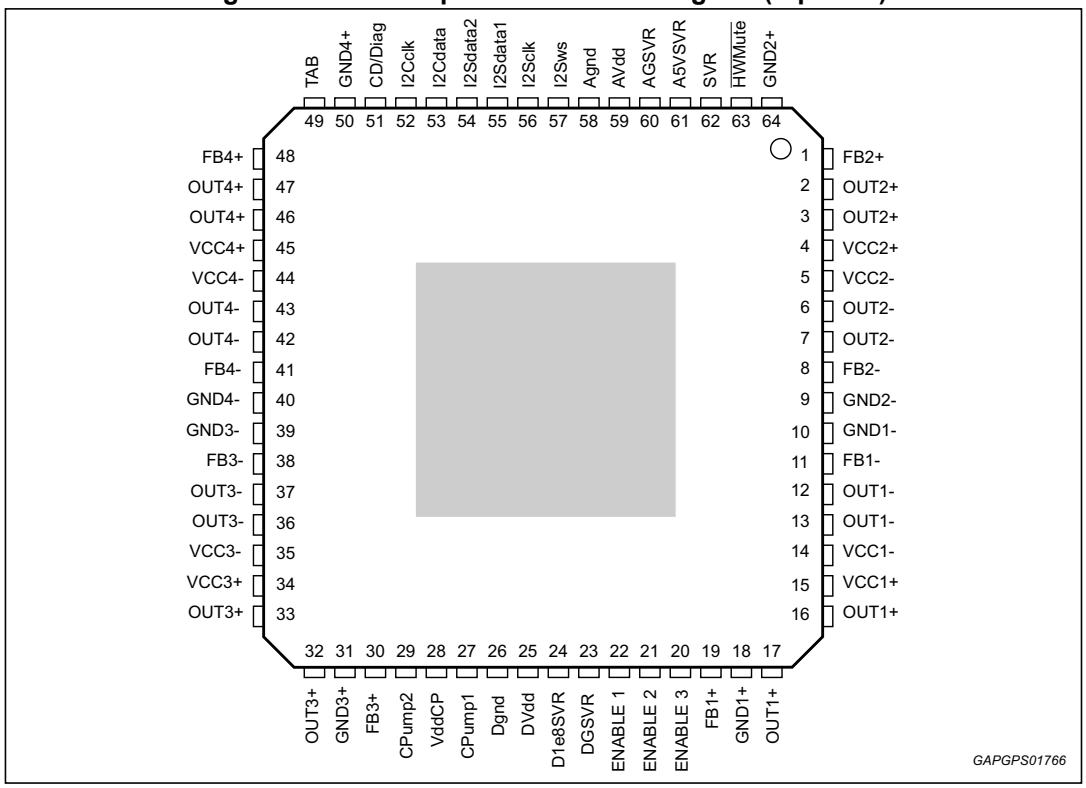


Table 2. Pins list description

N#	Pin	Function
1	FB2+	Channel 2, half bridge plus, Feedback
2	OUT2+	Channel 2, half bridge plus, Output
3	OUT2+	Channel 2, half bridge plus, Output
4	VCC2+	Channel 2, half bridge plus, Power Supply
5	VCC2-	Channel 2, half bridge minus, Power Supply
6	OUT2-	Channel 2, half bridge minus, Output
7	OUT2-	Channel 2, half bridge minus, Output
8	FB2-	Channel 2, half bridge minus, Feedback
9	GND2-	Channel 2, half bridge minus, Power Ground
10	GND1-	Channel 1, half bridge minus, Power Ground
11	FB1-	Channel 1, half bridge minus, Feedback
12	OUT1-	Channel 1, half bridge minus, Output
13	OUT1-	Channel 1, half bridge minus, Output
14	VCC1-	Channel 1, half bridge minus, Power Supply
15	VCC1+	Channel 1, half bridge plus, Power Supply
16	OUT1+	Channel 1, half bridge plus, Output

Table 2. Pins list description (continued)

N#	Pin	Function
17	OUT1+	Channel 1, half bridge plus, Output
18	GND1+	Channel 1, half bridge plus, Power Ground
19	FB1+	Channel 1, half bridge plus, Feedback
20	ENABLE 3	Enable 3
21	ENABLE 2	Enable 2
22	ENABLE 1	Enable 1
23	DGSVR	Negative digital supply V(SVR)-0.9V (Internally generated)
24	D1e8SVR	Positive digital supply V(SVR)+0.9V (Internally generated)
25	DVdd	Digital supply
26	Dgnd	Digital ground
27	CPump1	Charge Pump pin1
28	VddCP	Charge Pump output voltage
29	CPump2	Charge Pump pin2
30	FB3+	Channel 3, half bridge plus, Feedback
31	GND3+	Channel 3, half bridge plus, Power Ground
32	OUT3+	Channel 3, half bridge plus, Output
33	OUT3+	Channel 3, half bridge plus, Output
34	VCC3+	Channel 3, half bridge plus, Power Supply
35	VCC3-	Channel 3, half bridge minus, Power Supply
36	OUT3-	Channel 3, half bridge minus, Output
37	OUT3-	Channel 3, half bridge minus, Output
38	FB3-	Channel 3, half bridge minus, Feedback
39	GND3-	Channel 3, half bridge minus, Power Ground
40	GND4-	Channel 4, half bridge minus, Power Ground
41	FB4-	Channel 4, half bridge minus, Feedback
42	OUT4-	Channel 4, half bridge minus, Output
43	OUT4-	Channel 4, half bridge minus, Output
44	VCC4-	Channel 4, half bridge minus, Power Supply
45	VCC4+	Channel 4, half bridge plus, Power Supply
46	OUT4+	Channel 4, half bridge plus, Output
47	OUT4+	Channel 4, half bridge plus, Output
48	FB4+	Channel 4, half bridge plus, Feedback
49	TAB	Device slug connection
50	GND4+	Channel 4, half bridge plus, Power Ground

Table 2. Pins list description (continued)

N#	Pin	Function
51	CD/Diag	Clipping detector and diagnostic output pin: – Overcurrent protection intervention – Thermal warning – Offset detection
52	I2Cclk	I2C Clock
53	I2Cdata	I2C Data
54	I2Sdata2	I2S/TDM Data input 2
55	I2Sdata1	I2S/TDM Data input 1
56	I2Sclk	I2S/TDM Clock input
57	I2Sws	I2S/TDM Sinc input
58	Agnd	Analog ground
59	AVdd	Analog supply
60	AGSVR	Negative Analog Supply V(SVR)-2.5V (Internally generated)
61	A5VSVR	Positive Analog Supply V(SVR)+2.5V (Internally generated)
62	SVR	Supply Voltage Ripple Rejection Capacitor
63	$\overline{\text{HWMute}}$	Hardware mute pin
64	GND2+	Channel 2, half bridge plus, Power Ground

2 General introduction

FDA801 is a fully digital single chip class D amplifier with high immunity to the demodulation filter effects. The high integration level and the on-board signal processing allow excellent audio performance to be achieved.

Thanks to the digital input and to the feedback strategy in the power stage that make the amplifier immune from the output filter components non-linearity, the number and size of the external components are minimized.

A number of features are included to reduce EMI and the fully digital approach provides a strong GSM immunity.

FDA801 includes: digital I^2C and I^2S interfaces, internal 24 bits DAC conversion, digital signal processing for interpolation and noise shaping, innovative self-diagnostic functions and automatic detection of wrong load connections or variation of the load, internal PLL for a clock generation.

3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK® is an ST trademark.

3.1 LQFP64 (10x10x1.4 mm exp. pad up) package information

Figure 3. LQFP64 (10x10x1.4 mm exp. pad up) package outline

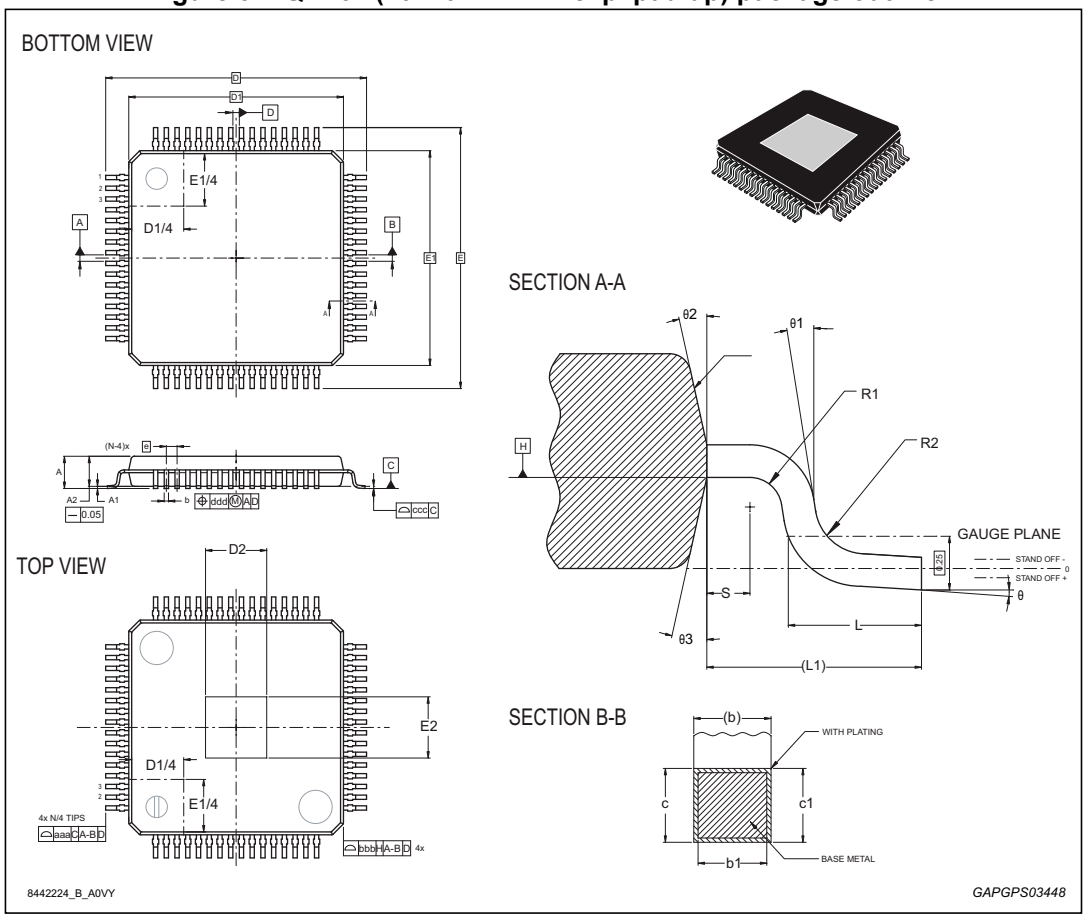


Table 3. LQFP64 (10x10x1.4 mm exp. pad up) package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
Θ	0°	3.5°	6°	0°	3.5°	6°
Θ1	0°	9°	12°	0°	9°	12°
Θ2	11°	12°	13°	11°	12°	13°
Θ3	11°	12°	13°	11°	12°	13°
A	-	-	1.49	-	-	0.0587
A1	-0.04	-	0.04	-0.0016	-	0.0016
A2	1.35	1.4	1.45	0.0531	0.0551	0.0571
b	-	-	0.255	-	-	0.0100
b1	0.17	0.20	0.23	0.0067	0.0079	0.0091
c	0.09	-	0.20	0.0035	-	0.0079
c1	0.09	-	0.16	0.0035	-	0.0063
D	-	12.00	-	-	0.4724	-
D1[2]	-	10.00	-	-	0.3937	-
D2[3]	-	6.00	-	-	02362	-
e	-	0.50	-	-	0.0197	-
E	-	12.00	-	-	0.4724	-
E1[2]	-	10.00	-	-	0.3937	-
E2[3]	-	6.00	-	-	0.2362	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
N	-	64.00	-	-	2.5197	-
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa	-	0.20	-	-	0.0079	-
bbb	-	0.20	-	-	0.0079	-
ccc	-	0.08	-	-	0.0031	-
ddd	-	0.08	-	-	0.0031	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimensions D1 and E1 do not include mold flash or protrusions.
   Allowable mold flash or protrusion is “0.25 mm” per side.
3. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.

4 Revision history

Table 4. Document revision history

Date	Revision	Changes
13-Nov-2015	1	Initial release.

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