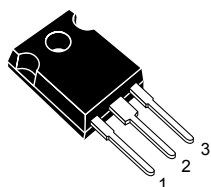
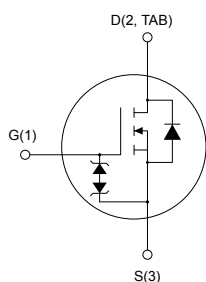


## N-channel 600 V, 150 mΩ typ., 20 A MDmesh M2 Power MOSFET in a TO-247 package


**TO-247**


AM15572V1\_TAB


**Product status link**
[STW27N60M2-EP](#)
**Product summary**

|            |               |
|------------|---------------|
| Order code | STW27N60M2-EP |
| Marking    | 27N60M2EP     |
| Package    | TO-247        |
| Packing    | Tube          |

### Features

| Order code    | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|---------------|----------|-------------------|-------|
| STW27N60M2-EP | 600 V    | 163 mΩ            | 20 A  |

- Extremely low gate charge
- Excellent output capacitance ( $C_{OSS}$ ) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications
- Tailored for very high frequency converters ( $f > 150$  kHz)

### Description

This device is an N-channel Power MOSFET developed using MDmesh M2 enhanced performance (EP) technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance, optimized switching characteristics with very low turn-off switching losses, rendering it suitable for the most demanding very high frequency converters.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol         | Parameter                                                         | Value      | Unit               |
|----------------|-------------------------------------------------------------------|------------|--------------------|
| $V_{DS}$       | Drain-source voltage                                              | 600        | V                  |
| $V_{GS}$       | Gate-source voltage                                               | $\pm 25$   | V                  |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$  | 20         | A                  |
| $I_D$          | Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$ | 13         | A                  |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                                            | 80         | A                  |
| $P_{TOT}$      | Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$     | 170        | W                  |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope                                 | 15         | V/ns               |
| $dv/dt^{(3)}$  | MOSFET $dv/dt$ ruggedness                                         | 50         | V/ns               |
| $T_{stg}$      | Storage temperature range                                         | -55 to 150 | $^{\circ}\text{C}$ |
| $T_J$          | Operating junction temperature range                              |            |                    |

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 20\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS}(\text{peak}) < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .
3.  $V_{DD} = 480\text{ V}$ .

**Table 2. Thermal data**

| Symbol     | Parameter                               | Value | Unit                        |
|------------|-----------------------------------------|-------|-----------------------------|
| $R_{thJC}$ | Thermal resistance, junction-to-case    | 0.74  | $^{\circ}\text{C}/\text{W}$ |
| $R_{thJA}$ | Thermal resistance, junction-to-ambient | 50    | $^{\circ}\text{C}/\text{W}$ |

**Table 3. Avalanche characteristics**

| Symbol   | Parameter                                                                                                              | Value | Unit |
|----------|------------------------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max.)                                    | 3.6   | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 260   | mJ   |

## 2 Electrical characteristics

( $T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 4. On/off states**

| Symbol        | Parameter                         | Test conditions                                                                             | Min. | Typ. | Max.     | Unit             |
|---------------|-----------------------------------|---------------------------------------------------------------------------------------------|------|------|----------|------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$                                                 | 600  | -    | -        | V                |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$                                             | -    | -    | 1        | $\mu\text{A}$    |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$ | -    | -    | 100      | $\mu\text{A}$    |
| $I_{GSS}$     | Gate body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$                                          | -    | -    | $\pm 10$ | $\mu\text{A}$    |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                                          | 2    | 3    | 4        | V                |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 10\text{ A}$                                                | -    | 150  | 163      | $\text{m}\Omega$ |

1. Specified by design, not tested in production.

**Table 5. Dynamic**

| Symbol                     | Parameter                     | Test conditions                                                                                                                                  | Min. | Typ. | Max. | Unit     |
|----------------------------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|----------|
| $C_{iss}$                  | Input capacitance             | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$                                                                             | -    | 1320 | -    | pF       |
| $C_{oss}$                  | Output capacitance            |                                                                                                                                                  | -    | 70   | -    | pF       |
| $C_{rss}$                  | Reverse transfer capacitance  |                                                                                                                                                  | -    | 1    | -    | pF       |
| $C_{oss\text{ eq.}}^{(1)}$ | Equivalent output capacitance | $V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$                                                                                      | -    | 146  | -    | pF       |
| $R_g$                      | Intrinsic gate resistance     | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$                                                                                                          | -    | 4    | -    | $\Omega$ |
| $Q_g$                      | Total gate charge             | $V_{DD} = 480\text{ V}$ , $I_D = 20\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$<br>(see the Figure 14. Test circuit for gate charge behavior) | -    | 33   | -    | nC       |
| $Q_{gs}$                   | Gate-source charge            |                                                                                                                                                  | -    | 5.2  | -    | nC       |
| $Q_{gd}$                   | Gate-drain charge             |                                                                                                                                                  | -    | 16   | -    | nC       |

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

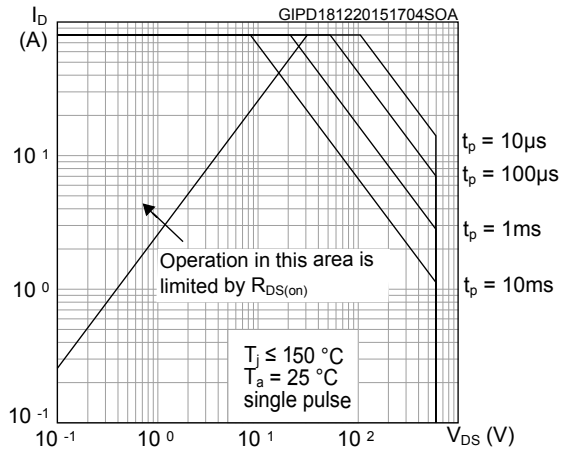
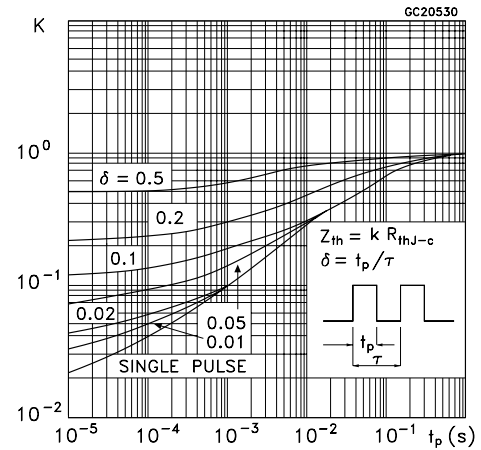
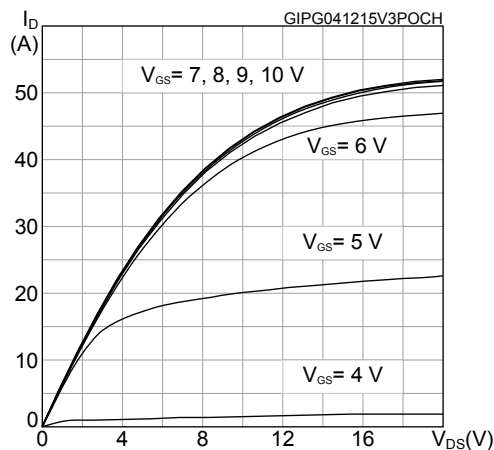
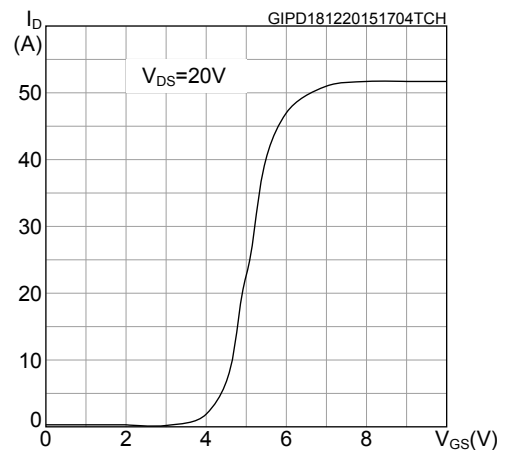
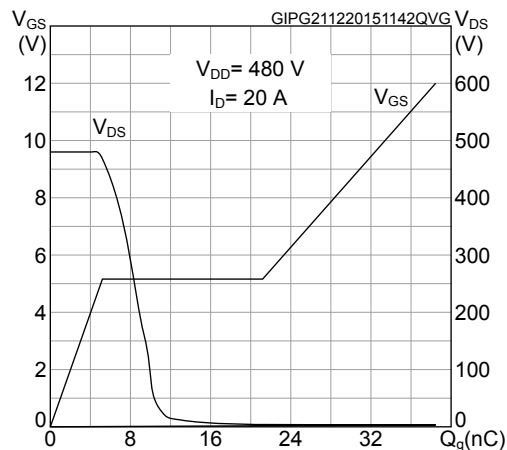
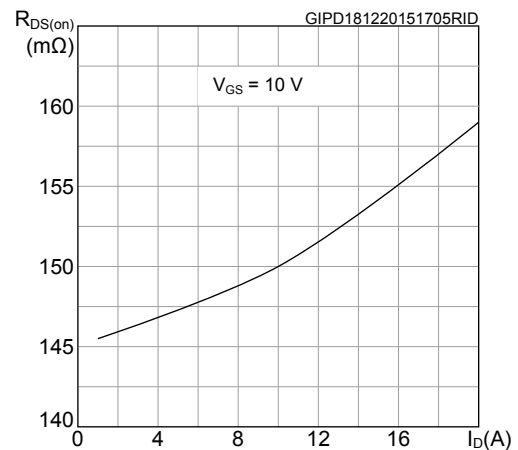
| Symbol       | Parameter           | Test conditions                                                                                                | Min. | Typ. | Max. | Unit |
|--------------|---------------------|----------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 300\text{ V}$ , $I_D = 10\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$          | -    | 13.4 | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                | -    | 8.1  | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time | (see the Figure 13. Test circuit for resistive load switching times and<br>Figure 18. Switching time waveform) | -    | 55.6 | -    | ns   |
| $t_f$        | Fall time           |                                                                                                                | -    | 6.3  | -    | ns   |

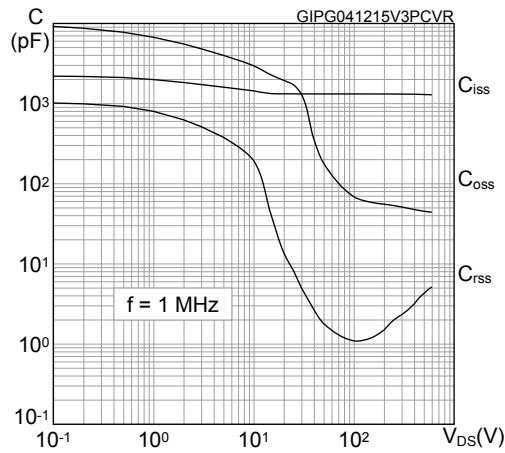
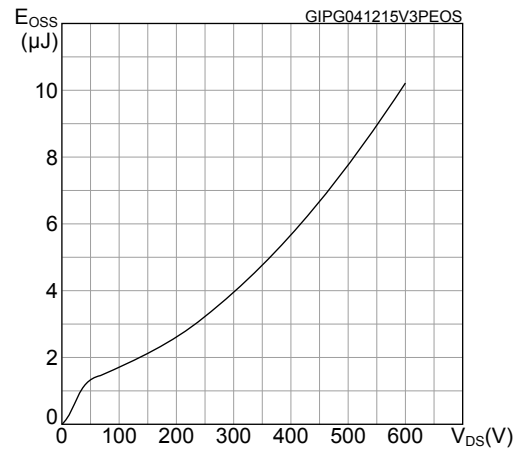
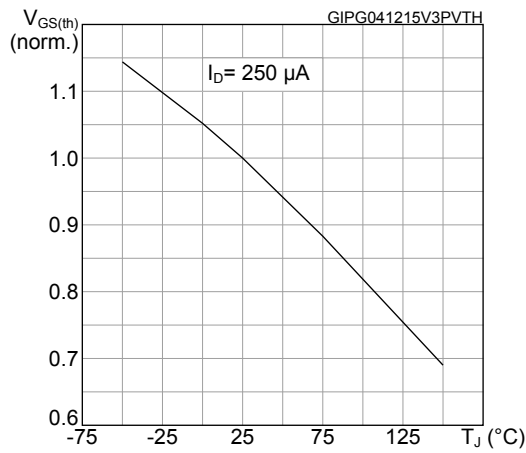
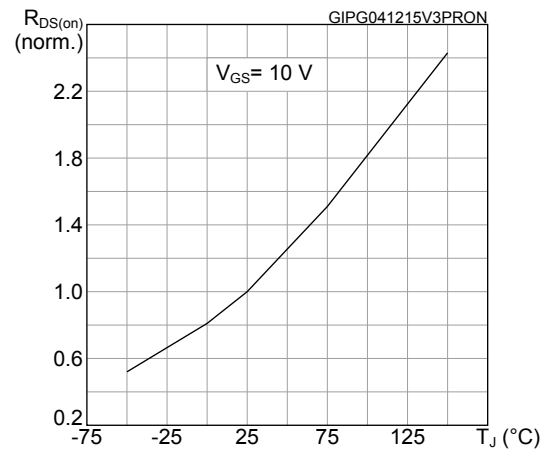
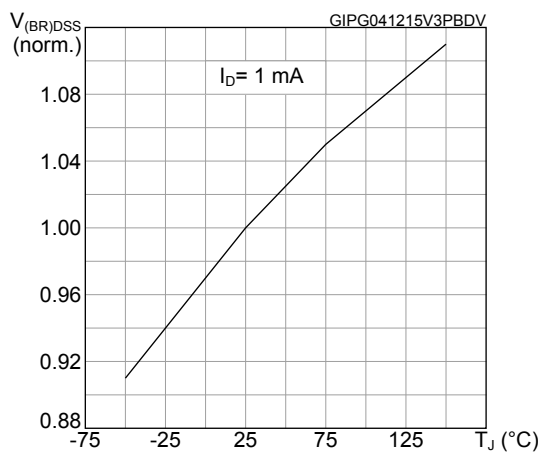
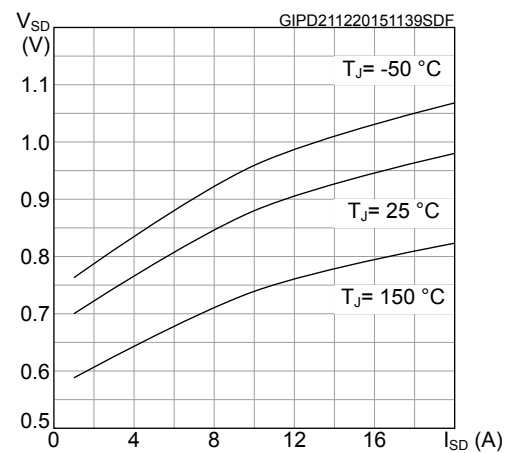
**Table 7. Source-drain diode**

| Symbol          | Parameter                     | Test conditions                                                                                                                                                                                                        | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                                                                                        | -    | -    | 20   | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                                        | -    | -    | 80   | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 20\text{ A}$ , $V_{GS} = 0\text{ V}$                                                                                                                                                                         | -    | -    | 1.6  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 20\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$<br>(see the Figure 15. Test circuit for inductive load switching and diode recovery times)                                        | -    | 271  | -    | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                        | -    | 3.44 | -    | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                        | -    | 25.4 | -    | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 20\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$<br>(see the Figure 15. Test circuit for inductive load switching and diode recovery times) | -    | 352  | -    | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                        | -    | 4.82 | -    | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                        | -    | 27.4 | -    | A             |

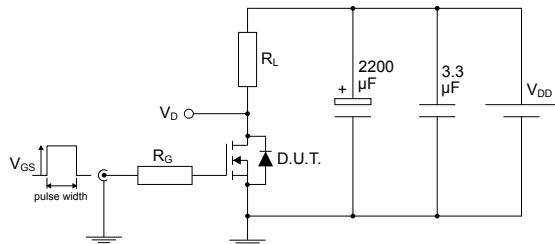
1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

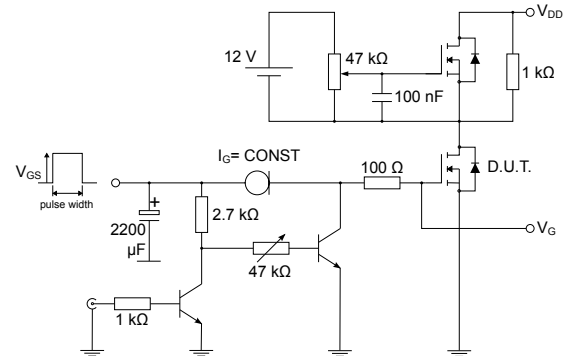
**Figure 1. Safe operating area**

**Figure 2. Normalized transient thermal impedance**

**Figure 3. Typical output characteristics**

**Figure 4. Typical transfer characteristics**

**Figure 5. Typical gate charge characteristics**

**Figure 6. Typical drain-source on-resistance**


**Figure 7. Typical capacitance characteristics**

**Figure 8. Typical output capacitance stored energy**

**Figure 9. Normalized gate threshold vs temperature**

**Figure 10. Normalized on-resistance vs temperature**

**Figure 11. Normalized breakdown voltage vs temperature**

**Figure 12. Typical reverse diode forward characteristics**


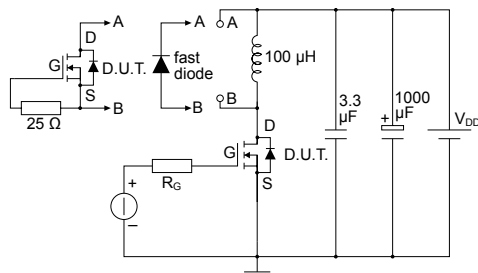
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


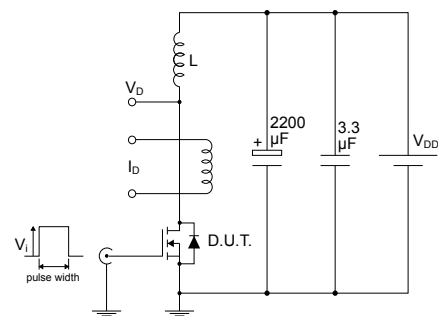
AM01468v1

**Figure 14. Test circuit for gate charge behavior**


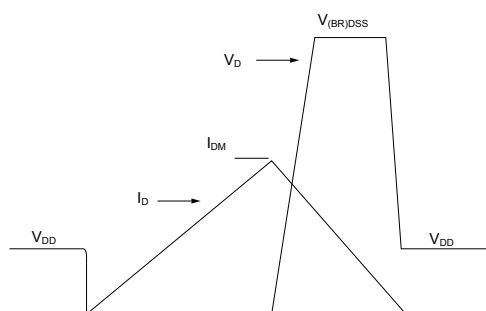
AM01469v1

**Figure 15. Test circuit for inductive load switching and diode recovery times**


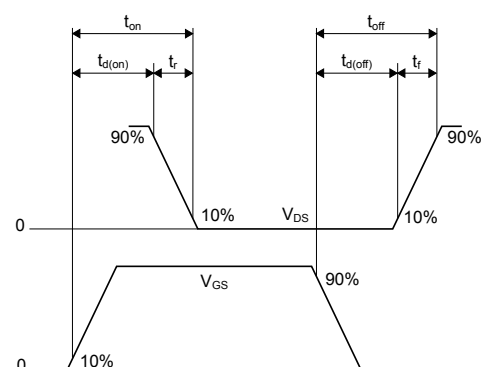
AM01470v1

**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


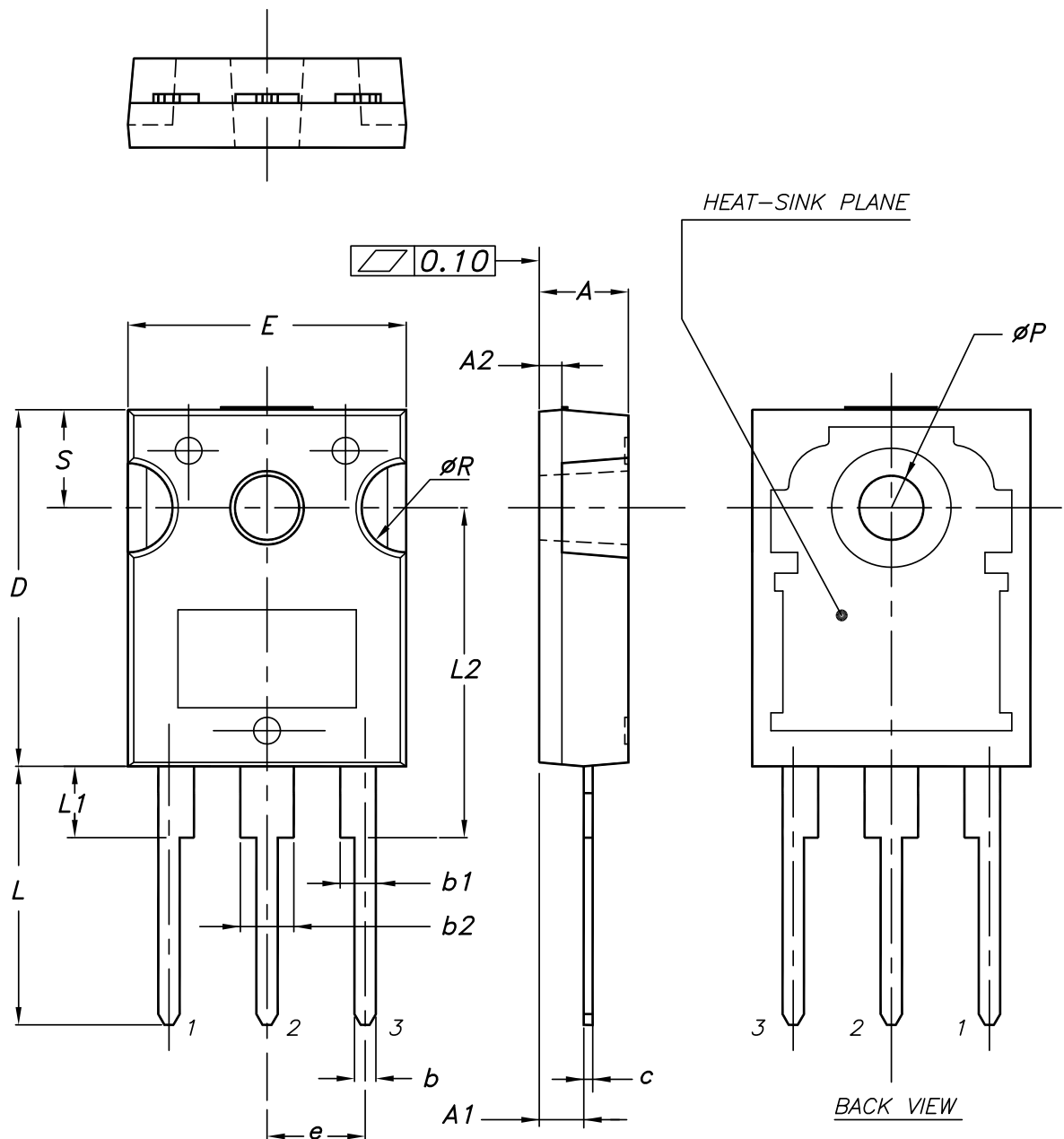
AM01473v1

## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-247 package information

Figure 19. TO-247 package outline



0075325\_11

**Table 8. TO-247 package mechanical data**

| Dim. | mm    |       |       |
|------|-------|-------|-------|
|      | Min.  | Typ.  | Max.  |
| A    | 4.85  |       | 5.15  |
| A1   | 2.20  |       | 2.60  |
| A2   |       | 1.27  |       |
| b    | 1.0   |       | 1.40  |
| b1   | 2.0   |       | 2.40  |
| b2   | 3.0   |       | 3.40  |
| c    | 0.40  |       | 0.80  |
| D    | 19.85 |       | 20.15 |
| E    | 15.45 |       | 15.75 |
| e    | 5.30  | 5.45  | 5.60  |
| L    | 14.20 |       | 14.80 |
| L1   | 3.70  |       | 4.30  |
| L2   |       | 18.50 |       |
| ØP   | 3.55  |       | 3.65  |
| ØR   | 4.50  |       | 5.50  |
| S    | 5.30  | 5.50  | 5.70  |

## Revision history

**Table 9. Document revision history**

| Date        | Revision | Changes                                                                                                              |
|-------------|----------|----------------------------------------------------------------------------------------------------------------------|
| 15-Dec-2015 | 1        | First release.                                                                                                       |
| 21-Apr-2026 | 2        | Removed order code STP27N60M2-EP.<br>Updated <a href="#">Section 4: Package information</a> .<br>Minor text changes. |

## Contents

|          |                                     |           |
|----------|-------------------------------------|-----------|
| <b>1</b> | <b>Electrical ratings</b>           | <b>2</b>  |
| <b>2</b> | <b>Electrical characteristics</b>   | <b>3</b>  |
| 2.1      | Electrical characteristics (curves) | 5         |
| <b>3</b> | <b>Test circuits</b>                | <b>7</b>  |
| <b>4</b> | <b>Package information</b>          | <b>8</b>  |
| 4.1      | TO-247 package information          | 8         |
|          | <b>Revision history</b>             | <b>10</b> |

**IMPORTANT NOTICE – READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2026 STMicroelectronics – All rights reserved