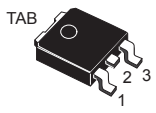
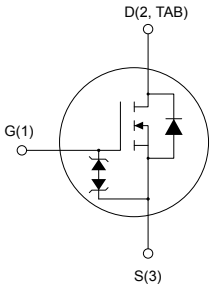
STD7LN80K5

Datasheet

N-channel 800 V, 0.95 Ω typ., 5 A, MDmesh K5 Power MOSFET in a DPAK package



DPAK



AM01476v1_tab

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD7LN80K5	800 V	1.15 Ω	5 A

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Product status link
STD7LN80K5

Product summary	
Order code	STD7LN80K5
Marking	7LN80K5
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current at T_C = 25 °C	5	A
	Drain current at T_C = 100 °C	3.4	
I_{DM} (1)	Drain current (pulsed)	20	A
P_{TOT}	Total power dissipation at T_C = 25 °C	85	W
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	V/ns
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 5 A, di/dt ≤ 100 A/µs, V_{DS} (peak) ≤ $V_{(BR)DSS}$, V_{DD} = 640 V.*
3. *V_{DS} ≤ 640 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.47	°C/W
R_{thJA} (1)	Thermal resistance, junction-to-ambient	50	°C/W

1. *When mounted on FR-4 board of 1 inch², 2oz Cu.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max)	1.5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	200	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	800			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 800 V			1	µA
		V_{GS} = 0 V, V_{DS} = 800 V, T_C = 125 °C(1)			50	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.5 A		0.95	1.15	Ω

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	270	-	pF
C_{oss}	Output capacitance		-	22	-	pF
C_{rss}	Reverse transfer capacitance		-	0.5	-	pF
$C_{o(tr)}$(1)	Equivalent output capacitance time related	V_{GS} = 0 V, V_{DS} = 0 to 640 V	-	17	-	pF
$C_{o(er)}$(2)	Equivalent output capacitance energy related		-	48	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	7.5	-	Ω
Q_g	Total gate charge	V_{DD} = 640 V, I_D = 5 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	12	-	nC
Q_{gs}	Gate-source charge		-	2.6	-	nC
Q_{gd}	Gate-drain charge		-	8.6	-	nC

1. *$C_{o(tr)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
2. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 2.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	9.3	-	ns
t_r	Rise time		-	6.7	-	ns
$t_{d(off)}$	Turn-off delay time		-	23.6	-	ns
t_f	Fall time		-	17.4	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5	A
I_{SDM} (1)	Source-drain current (pulsed)		-		20	A
V_{SD} (2)	Forward on voltage	I_{SD} = 5 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs,	-	276		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V	-	2.13		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	15.4		A
t_{rr}	Reverse recovery time	I_{SD} = 5 A, di/dt = 100 A/µs,	-	402		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_J = 150 °C	-	2.79		µC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	13.9		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

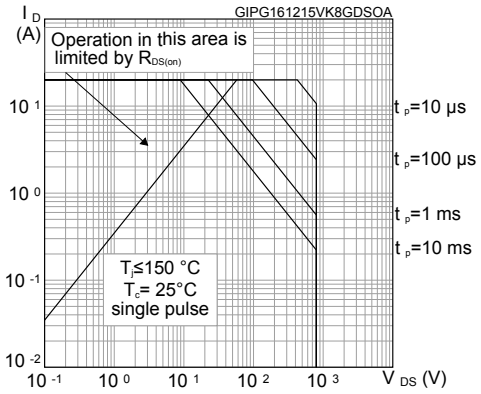


Figure 2. Normalized transient thermal impedance

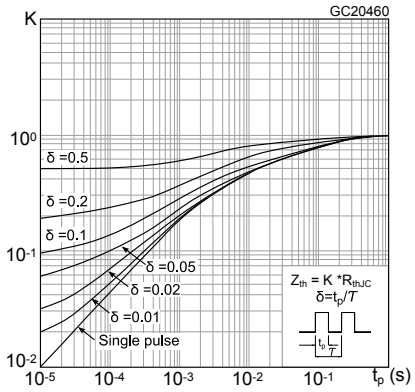


Figure 3. Typical output characteristics

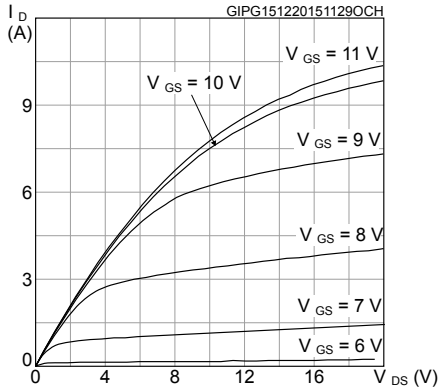


Figure 4. Typical transfer characteristics

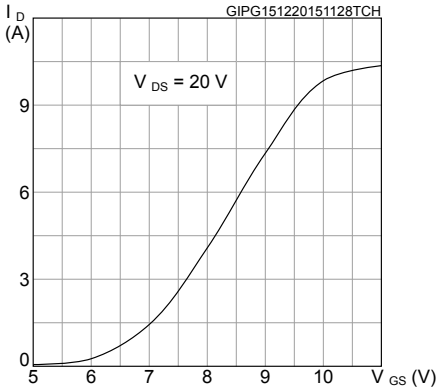


Figure 5. Typical gate charge characteristics

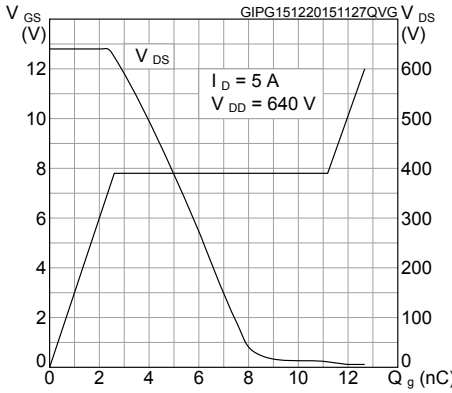


Figure 6. Typical drain-source on-resistance

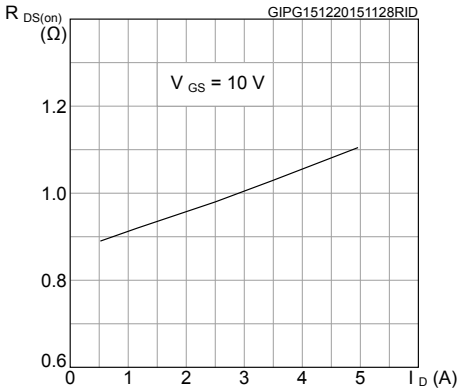


Figure 7. Typical capacitance characteristics

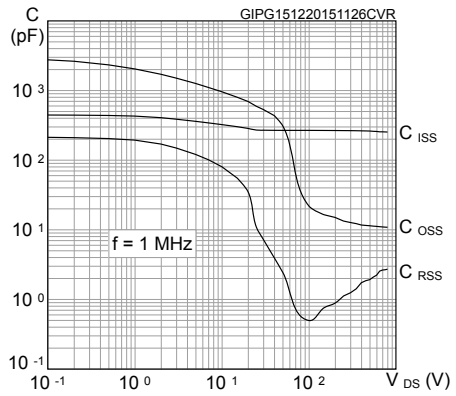


Figure 8. Normalized gate threshold voltage vs temperature

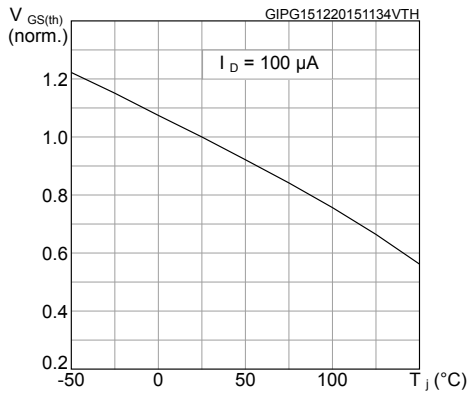


Figure 9. Normalized $V_{(BR)DSS}$ vs temperature

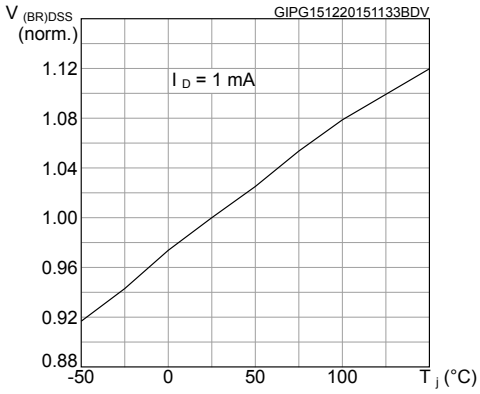


Figure 10. Normalized on-resistance vs temperature

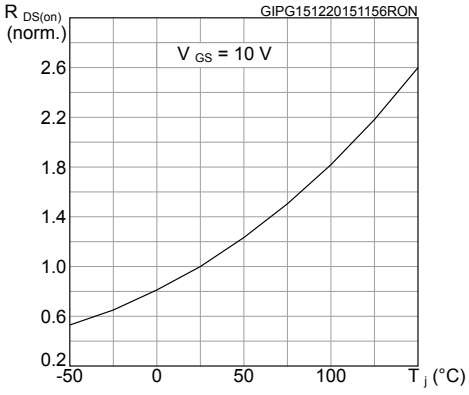


Figure 11. Typical reverse diode forward characteristics

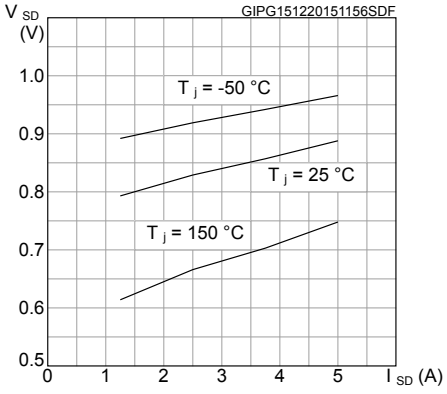
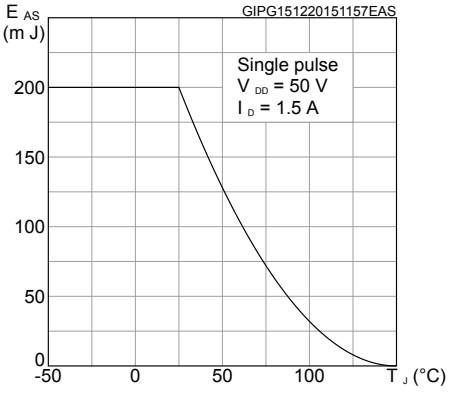
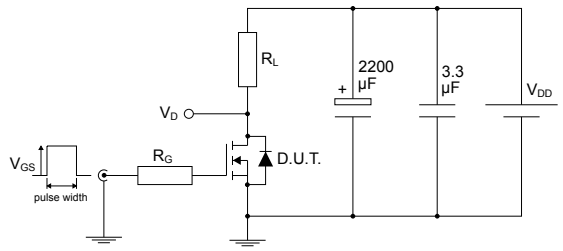


Figure 12. Maximum avalanche energy vs temperature



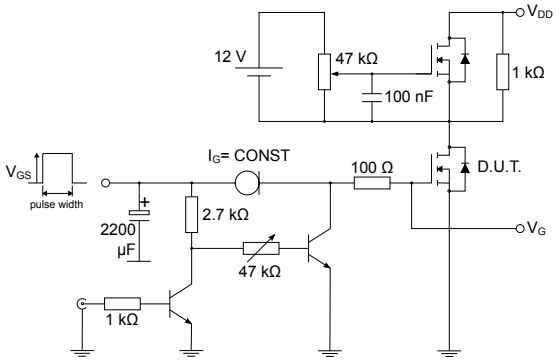
3 Test circuits

Figure 13. Test circuit for resistive load switching times



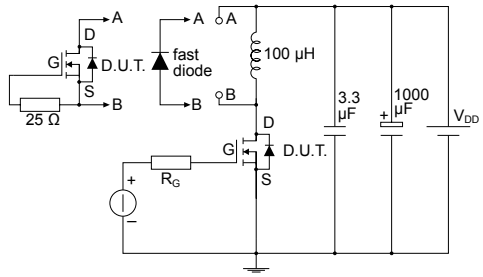
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Figure 14. Test circuit for gate charge behavior



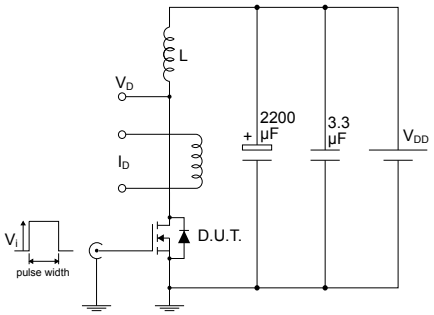
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Figure 15. Test circuit for inductive load switching and diode recovery times



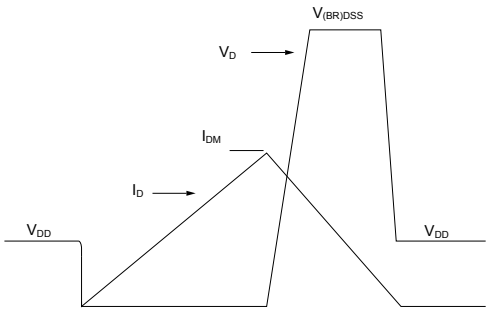
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Figure 16. Unclamped inductive load test circuit



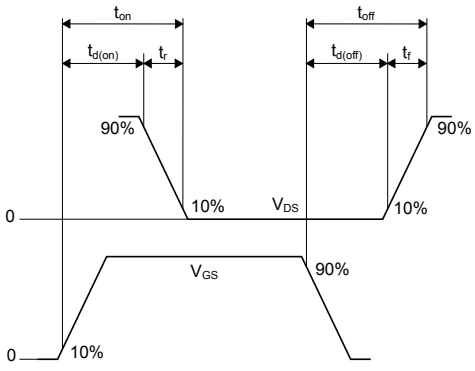
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Figure 17. Unclamped inductive waveform



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Figure 18. Switching time waveform



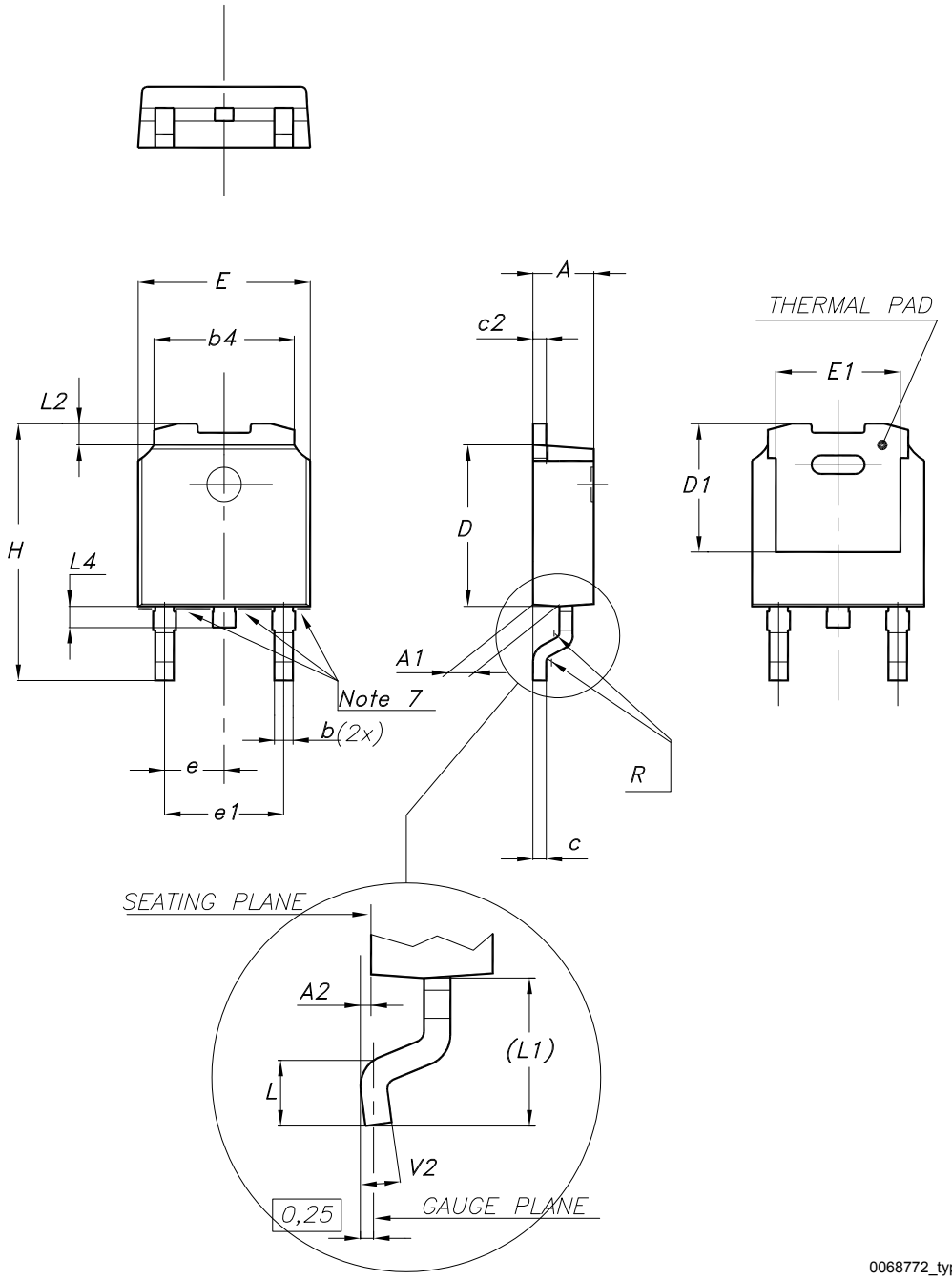
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 19. DPAK (TO-252) type A2 package outline



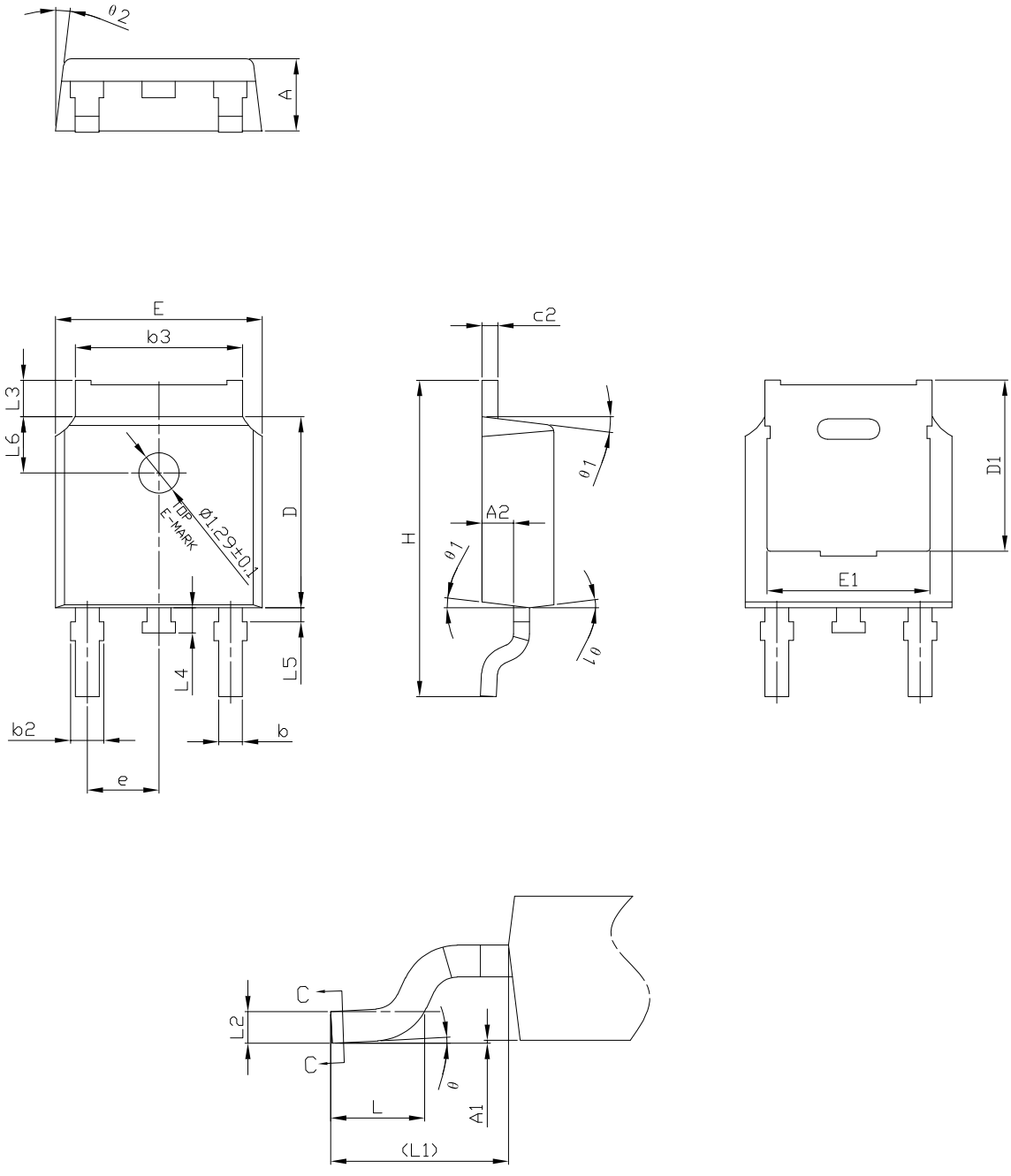
0068772_type-A2_rev34

Table 8. **DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C3 package information

Figure 20. DPAK (TO-252) type C3 package outline

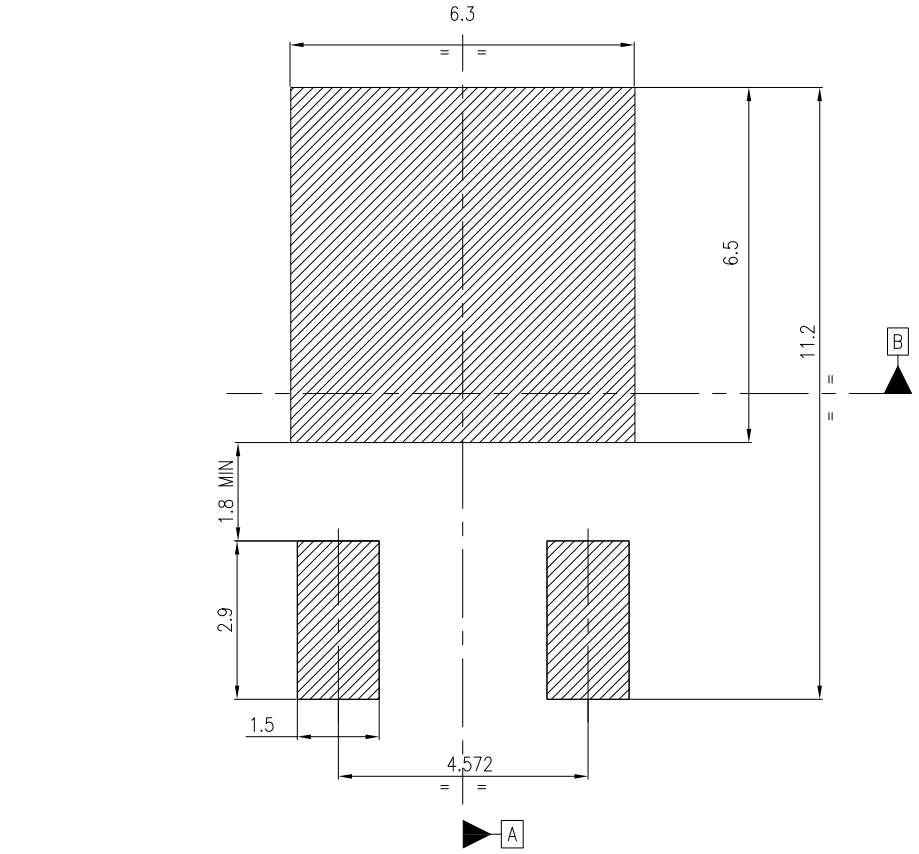


0068772_type-C3_rev34

Table 9. **DPAK (TO-252) type C3 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.00		0.10
A2	0.90	1.01	1.10
b	0.72		0.85
b2	0.72		1.10
b3	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.20	5.45	5.70
E	6.50	6.60	6.70
E1	5.00	5.20	5.40
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.51 BSC		
L3	0.90		1.25
L4	0.60	0.80	1.00
L5	0.15		0.75
L6	1.80 REF		
θ	0°		8°
θ1	5°	7°	9°
θ2	5°	7°	9°

Figure 21. DPAK (TO-252) recommended footprint (dimensions are in mm)



Notes:
1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664−1)
2) The device must be positioned within ⌖ 0.05 A B

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4.3 DPAK (TO-252) packing information

Figure 22. **DPAK (TO-252) tape outline**

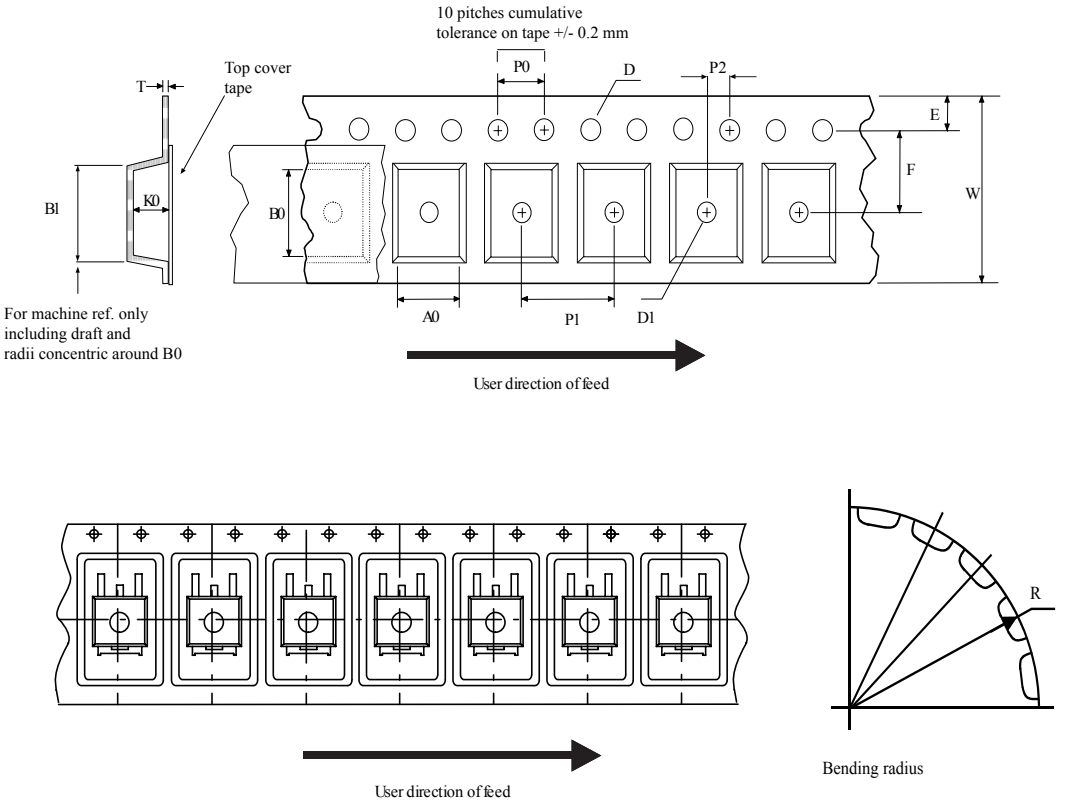
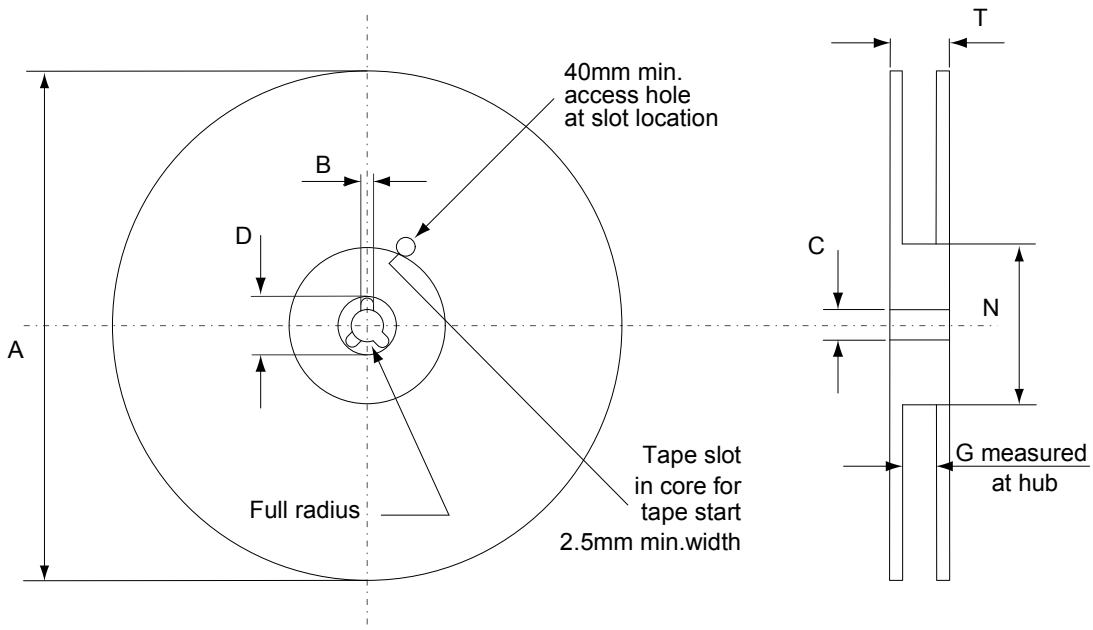


Figure 23. **DPAK (TO-252) reel outline**



AM06038v1

Table 10. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 11. **Document revision history**

Date	Revision	Changes
16-Dec-2015	1	First release.
19-Apr-2023	2	Updated DPAK (TO-252) type A2 package information Added Section 4.2 DPAK (TO-252) type C3 package information Minor text changes.

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