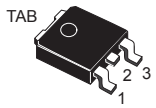
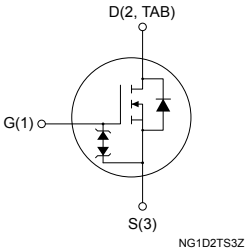
N-channel 600 V, 370 mΩ typ., 10 A MDmesh DM2 Power MOSFET in a DPAK package



DPAK



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$max.	I_D	P_{TOT}
STD11N60DM2	650 V	420 mΩ	10 A	110 W

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM2 fast-recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Product status
STD11N60DM2

Product summary	
Order code	STD11N60DM2
Marking	11N60DM2
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	10	A
	Drain current (continuous) at T_C = 100 °C	6.3	
I_{DM} (1)	Drain current (pulsed)	40	A
P_{TOT}	Total power dissipation at T_C = 25 °C	110	W
dv/dt(2)	Peak diode recovery voltage slope	50	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 10 A, di/dt=900 A/µs; $V_{DS}(peak) < V_{(BR)DSS}$, V_{DD} = 400 V*
3. *V_{DS} ≤ 480 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.14	°C/W
R_{thJA} (1)	Thermal resistance, junction-to-ambient	50	

1. *When mounted on 1 inch² FR-4 board, 2oz Cu.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR} (1)	Avalanche current, repetitive or not repetitive	2.5	A
E_{AS} (2)	Single pulse avalanche energy	250	mJ

1. *pulse width limited by T_{jmax}*
2. *starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.*

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1.5	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 5 A		370	420	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	614	-	pF
C_{oss}	Output capacitance		-	32	-	
C_{rss}	Reverse transfer capacitance		-	1.08	-	
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	57	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	6.2	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 10 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	16.5	-	nC
Q_{gs}	Gate-source charge		-	3.8	-	
Q_{gd}	Gate-drain charge		-	9.2	-	

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	11.7	-	ns
t_r	Rise time		-	6.3	-	
$t_{d(off)}$	Turn-off delay time		-	31	-	
t_f	Fall time		-	9.5	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		10	A
I_{SDM} (1)	Source-drain current (pulsed)		-		40	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 10 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 10 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	90		ns
Q_{rr}	Reverse recovery charge		-	248		nC
I_{RRM}	Reverse recovery current		-	5.5		A
t_{rr}	Reverse recovery time	I_{SD} = 10 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	160		ns
Q_{rr}	Reverse recovery charge		-	664		nC
I_{RRM}	Reverse recovery current		-	8.3		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

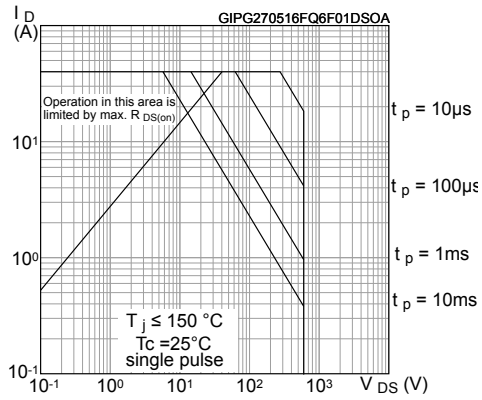


Figure 2. Thermal impedance

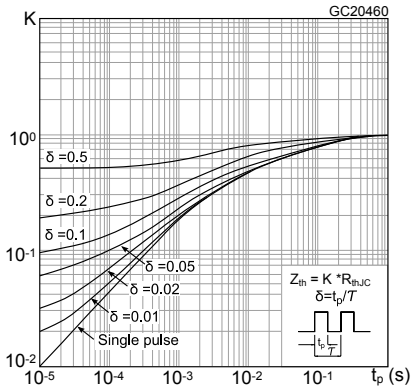


Figure 3. Output characteristics

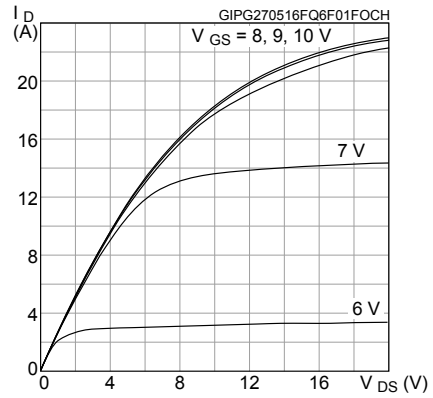


Figure 4. Transfer characteristics

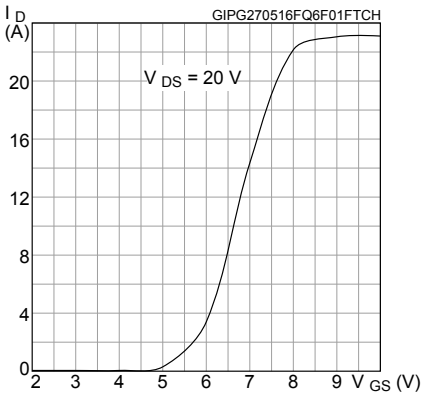


Figure 5. Gate charge vs gate-source voltage

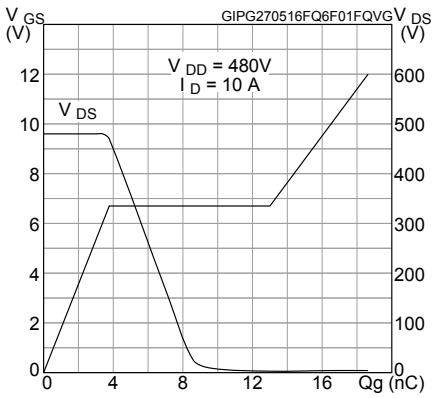


Figure 6. Static drain-source on-resistance

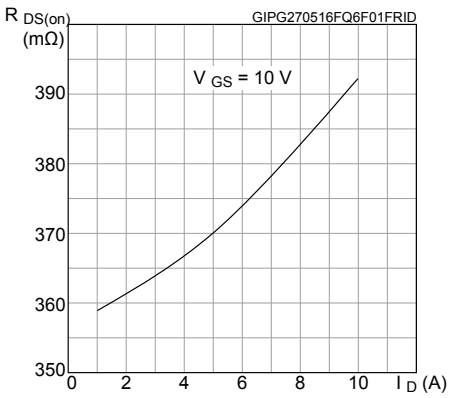


Figure 7. Capacitance variations

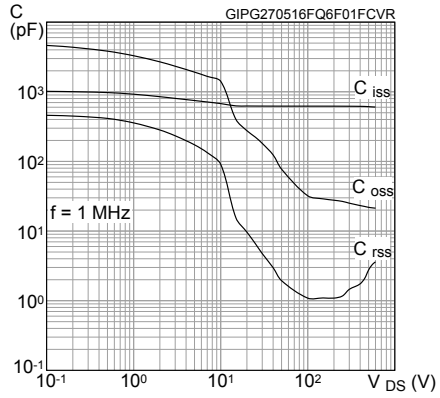


Figure 8. Normalized gate threshold voltage vs temperature

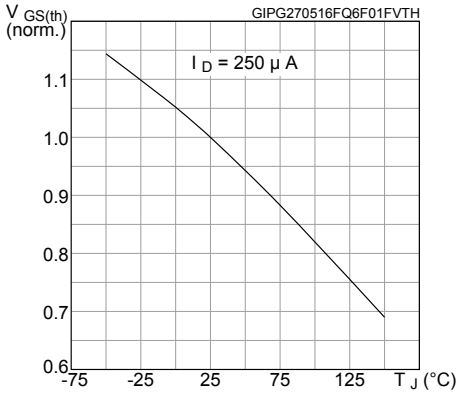


Figure 9. Normalized on-resistance vs temperature

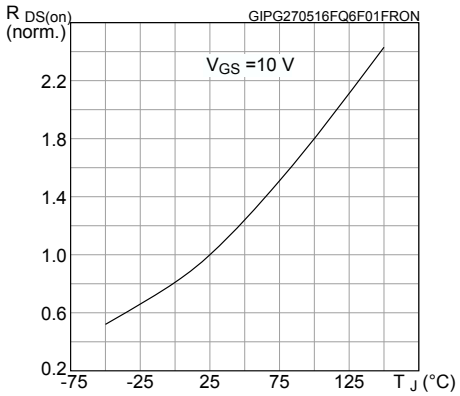


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

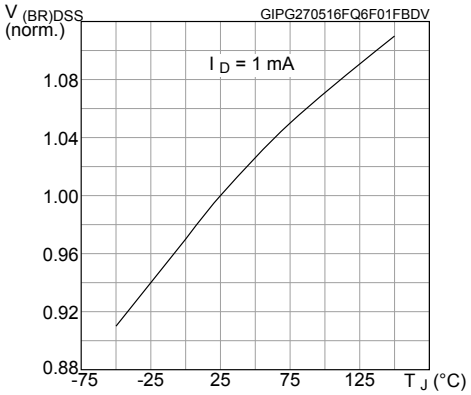


Figure 11. Output capacitance stored energy

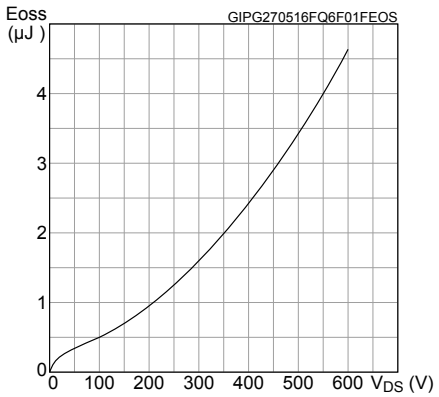
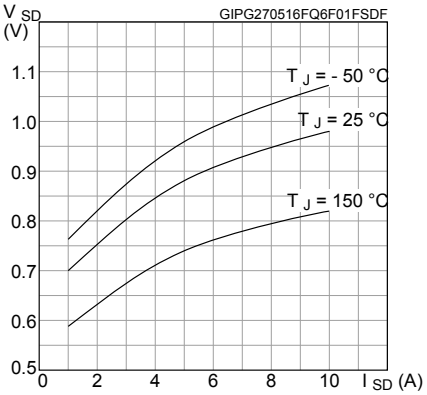
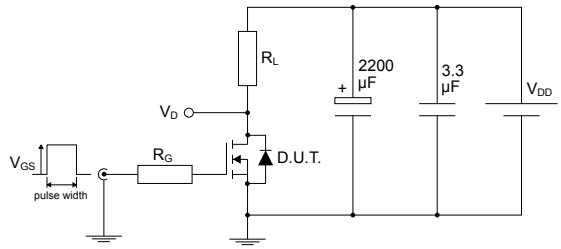


Figure 12. Source-drain diode forward characteristics



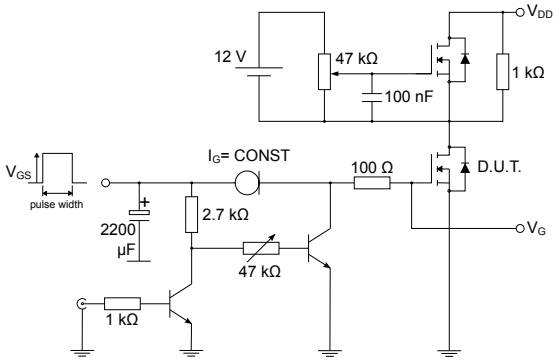
3 Test circuits

Figure 13. Test circuit for resistive load switching times



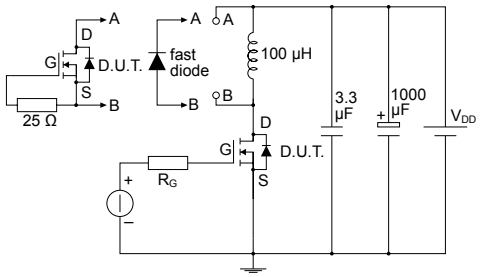
AM01468v1

Figure 14. Test circuit for gate charge behavior



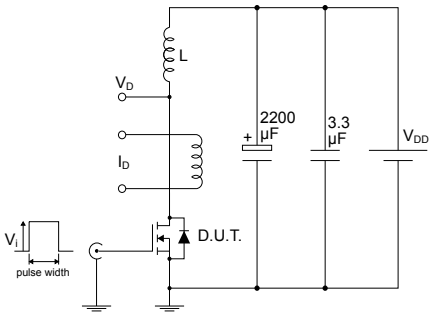
AM01469v1

Figure 15. Test circuit for inductive load switching and diode recovery times



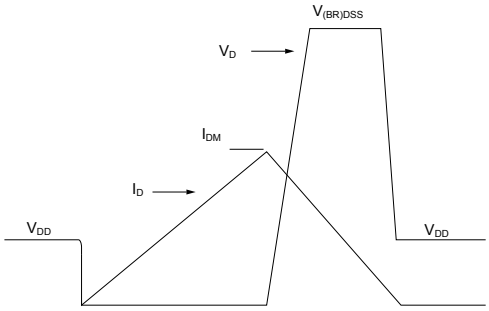
AM01470v1

Figure 16. Unclamped inductive load test circuit



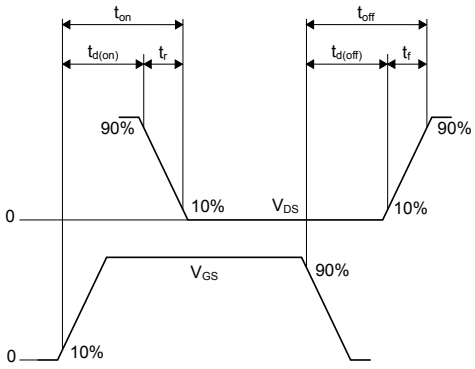
AM01471v1

Figure 17. Unclamped inductive waveform



AM01472v1

Figure 18. Switching time waveform



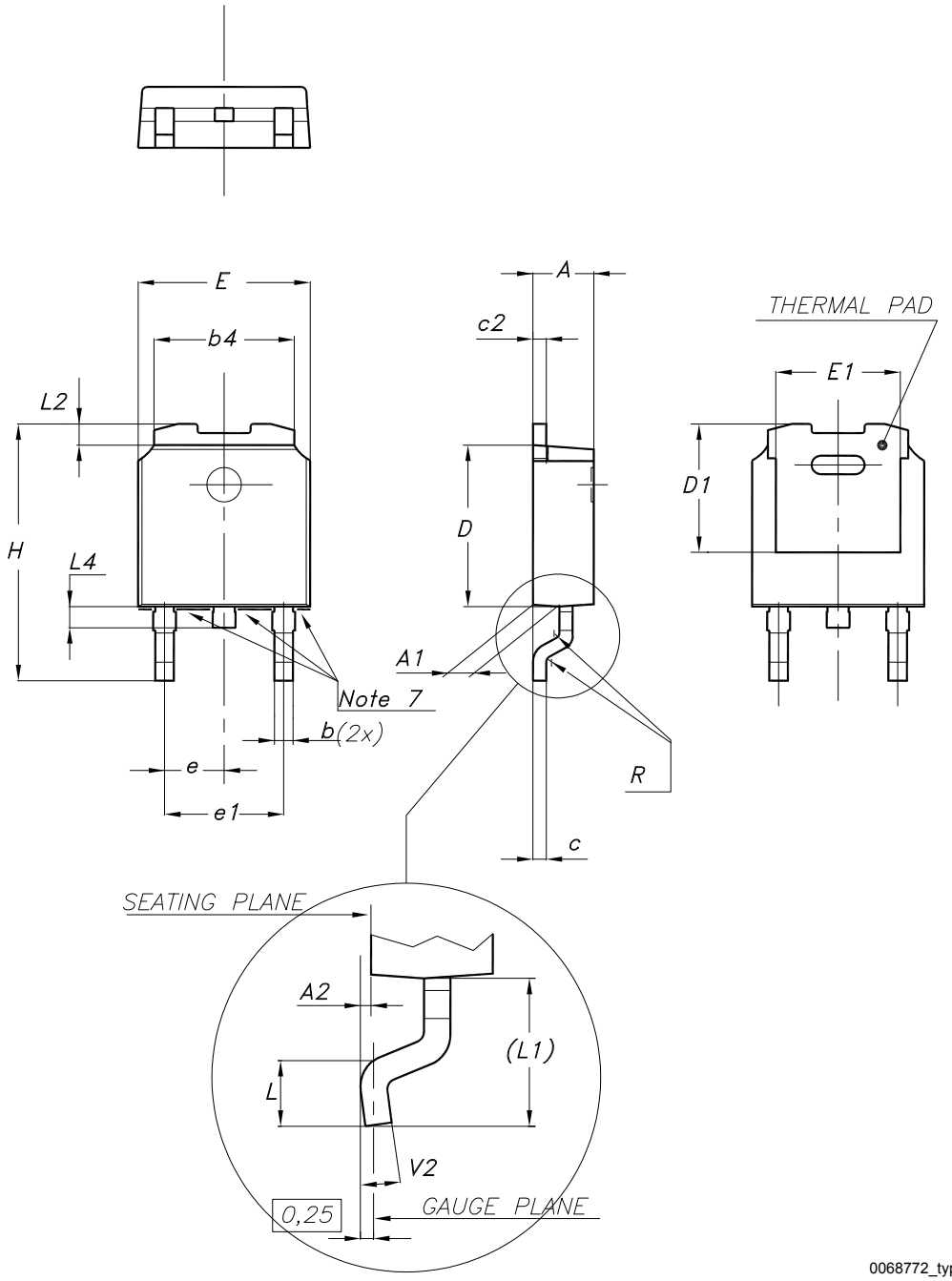
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 19. DPAK (TO-252) type A2 package outline



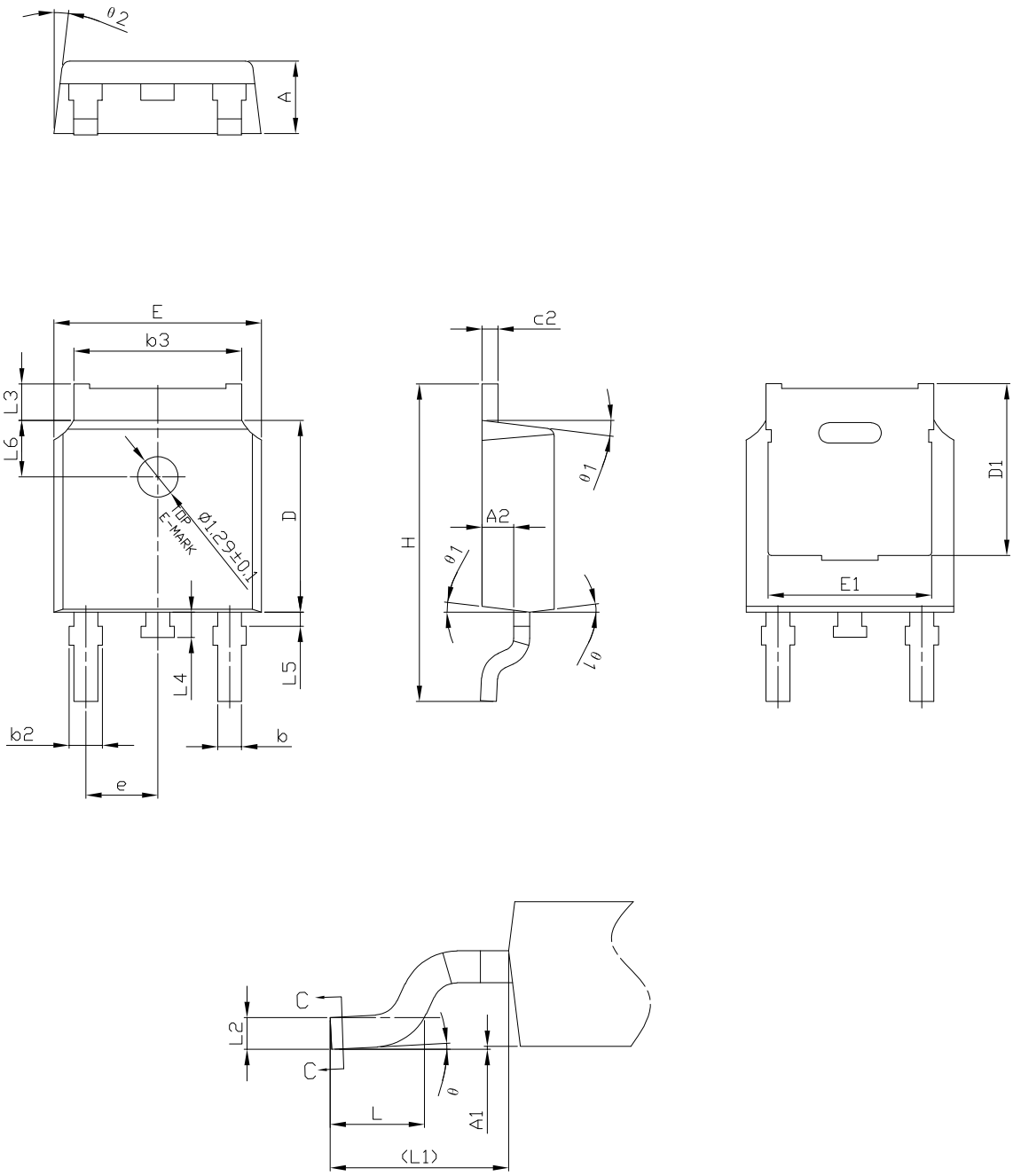
0068772_type-A2_rev34

Table 8. **DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C3 package information

Figure 20. DPAK (TO-252) type C3 package outline

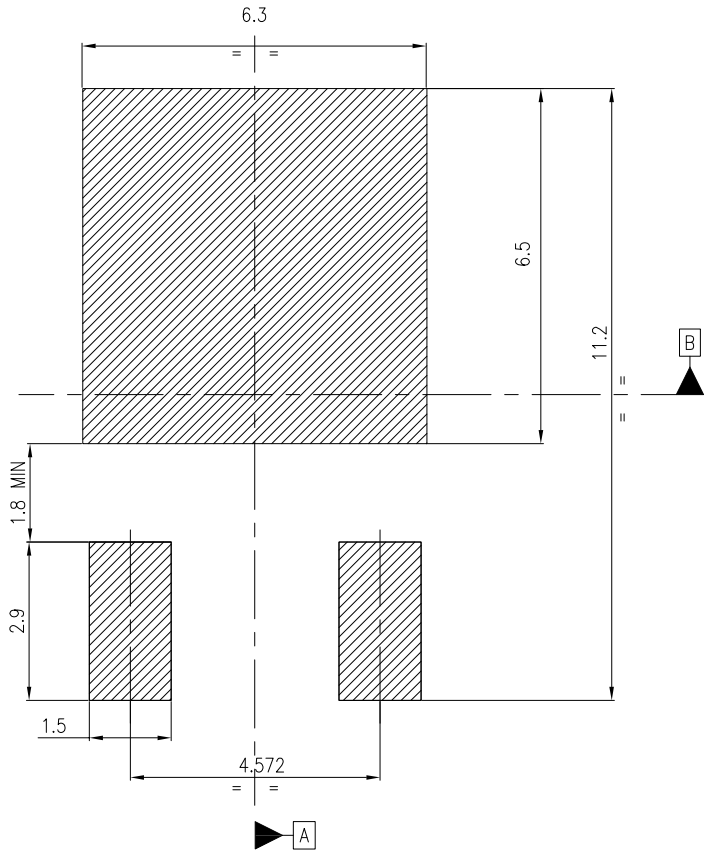


0068772_type-C3_rev34

Table 9. **DPAK (TO-252) type C3 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.00		0.10
A2	0.90	1.01	1.10
b	0.72		0.85
b2	0.72		1.10
b3	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.20	5.45	5.70
E	6.50	6.60	6.70
E1	5.00	5.20	5.40
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.51 BSC		
L3	0.90		1.25
L4	0.60	0.80	1.00
L5	0.15		0.75
L6	1.80 REF		
θ	0°		8°
θ1	5°	7°	9°
θ2	5°	7°	9°

Figure 21. **DPAK (TO-252) recommended footprint (dimensions are in mm)**



Notes:

1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664−1)

2) The device must be positioned within ⌖ 0.05 A B

FP_0068772_34

4.3 DPAK (TO-252) packing information

Figure 22. **DPAK (TO-252) tape outline**

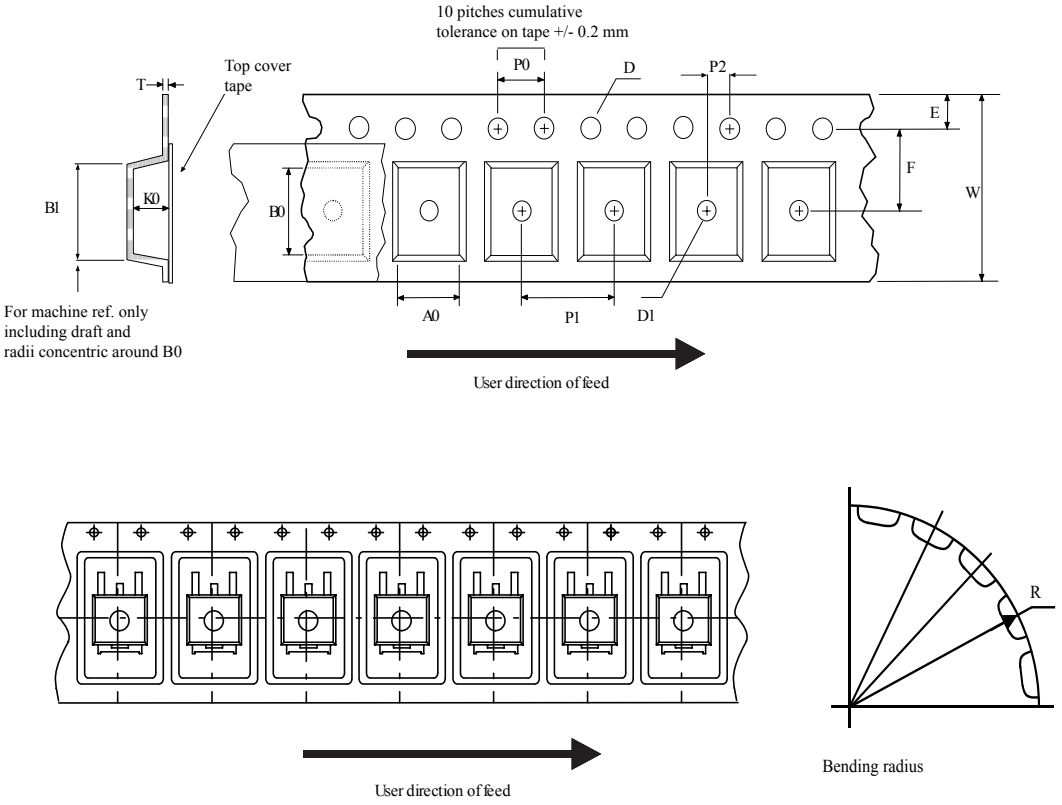
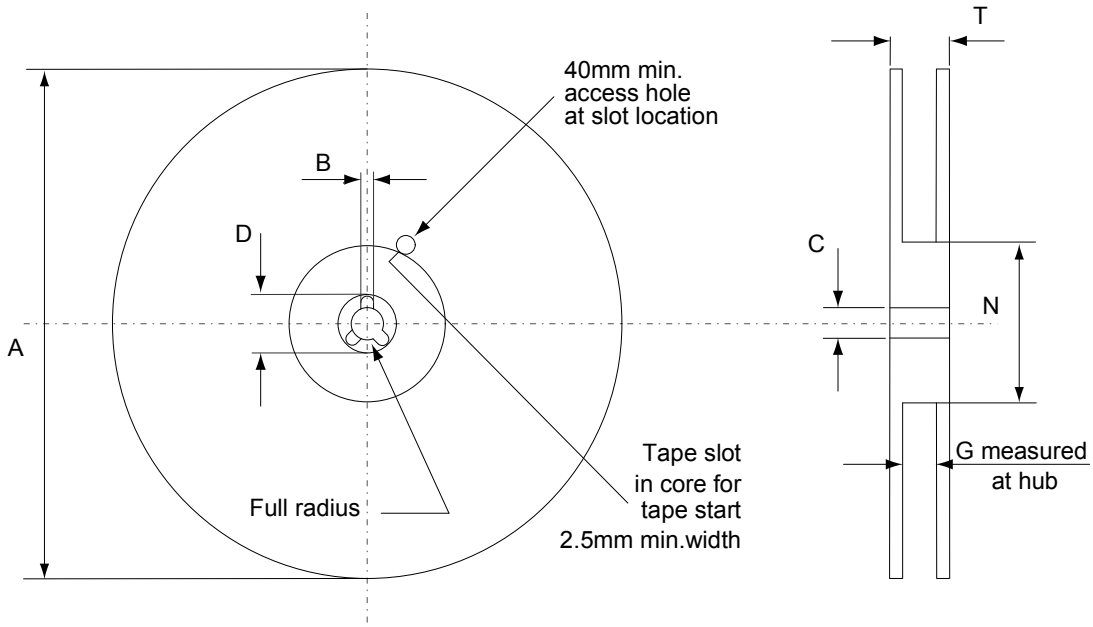


Figure 23. **DPAK (TO-252) reel outline**



AM06038v1

Table 10. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 11. **Document revision history**

Date	Revision	Changes
17-Jun-2016	1	First release.
04-Nov-2019	2	Modified *Table 1. Absolute maximum ratings* and *Table 4. Static*. Updated *Section 4.1 DPAK (TO-252) type A2 package information*. Minor text changes.
05-May-2023	3	Updated Section 4.1 DPAK (TO-252) type A2 package information. Added Section 4.2 DPAK (TO-252) type C3 package information. Minor text changes.

Contents

1 **Electrical ratings** 2
2 **Electrical characteristics** 3
2.1 Electrical characteristics (curves) 5
3 **Test circuits** 7
4 **Package information** 8
4.1 DPAK (TO-252) type A2 package information 8
4.2 DPAK (TO-252) type C3 package information 10
4.3 DPAK (TO-252) packing information 13
Revision history 15

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2023 STMicroelectronics – All rights reserved