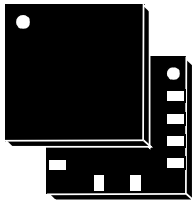
ISM303DAC

High-performance, low-power, compact 3D accelerometer and 3D magnetometer module

Datasheet - production data



LGA-12 (2.0x2.0x1.0 mm)

Features

- 3 magnetic field channels and 3 acceleration channels
- Up to ±50 gauss magnetic dynamic range
- ±2/±4/±8/±16 *g* selectable acceleration full scales
- Dynamic switching between high-resolution, high-frequency and low-power modes
- 16-bit data output
- SPI / I^2C serial interfaces
- Analog supply voltage 1.71 V to 1.98 V
- Programmable interrupt generators for free-fall, motion and magnetic field detection
- Embedded self-test both for the accelerometer and magnetometer
- Embedded 256-level FIFO
- Embedded temperature sensor
- ECOPACK®, RoHS and “Green” compliant

Applications

- Dual mode anti-tampering in smart meters
- Antenna pointing
- Motion tracking
- Robotics and appliances
- Positioning and navigation systems
- Positional and distance sensor

Description

The ISM303DAC is a high-performance, low-power system-in-package featuring a 3D digital linear acceleration sensor and a 3D digital magnetic sensor.

The ISM303DAC has user-selectable linear acceleration full scales of ±2*g*/±4*g*/±8*g*/±16 *g* and is capable of measuring accelerations with output data rates from 1 Hz to 6400 Hz. The device has a magnetic field dynamic range of up to ±50 gauss with output data rates from10 Hz to 150 Hz. The ISM303DAC includes an I^2C serial bus interface that supports standard, fast mode, fast mode plus, and high-speed (100 kHz, 400 kHz, 1 MHz, and 3.4 MHz) and an SPI serial standard interface.

The ISM303DAC has an integrated 256-level first-in, first-out (FIFO) buffer for the accelerometer data which can be used to limit the intervention of the host processor.

The embedded self-test capability allows the user to check the functioning of the sensor in the final application.

The system can be configured to generate an interrupt signal for free-fall, motion detection and magnetic field detection. The magnetic and accelerometer blocks can be enabled or put into power-down mode separately.

The ISM303DAC is available in a plastic land grid array package (LGA) and is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Part number	Temp. range [°C]	Package	Packaging
ISM303DACTR	-40 to +85	LGA-12	Tape and reel

This is information on a product in full production. www.st.com

Contents

1 **Block diagram and pin description 10**

1.1 Block diagram 10

1.2 Pin description 11

2 **Module specifications 13**

2.1 Sensor characteristics 13

2.2 Temperature sensor characteristics 15

2.3 Electrical characteristics 15

2.4 Communication interface characteristics 17

2.4.1 SPI - serial peripheral interface 17

2.4.2 I^2C - inter-IC control interface 18

2.5 Absolute maximum ratings 20

3 **Terminology 21**

3.1 Sensitivity 21

3.1.1 Linear acceleration sensor sensitivity 21

3.1.2 Magnetic sensor sensitivity 21

3.2 Zero-g level 21

3.3 Zero-gauss level 21

3.4 Magnetic dynamic range 21

4 **Functionality 22**

4.1 Magnetometer 22

4.1.1 Magnetometer power modes 22

4.1.2 Magnetometer offset cancellation 24

4.1.3 Magnetometer interrupt 25

4.1.4 Magnetometer hard-iron compensation 27

4.1.5 Magnetometer self-test 27

4.2 Accelerometer 29

4.2.1 Accelerometer power modes 29

4.2.2 Accelerometer bandwidth 31

4.2.3 Accelerometer 6D / 4D orientation detection 33

4.2.4 Accelerometer activity/inactivity function 33

4.2.5 Accelerometer self-test . . . 33
4.2.6 Accelerometer data stabilization time vs. ODR setting . . . 35
4.3 IC interface . . . 35
4.4 FIFO . . . 36
4.4.1 Bypass mode . . . 36
4.4.2 FIFO mode . . . 37
4.4.3 Continuous mode . . . 37
4.4.4 Continuous-to-FIFO mode . . . 37
4.4.5 Bypass-to-Continuous mode . . . 39
4.4.6 Module-to-FIFO . . . 40
4.5 Factory calibration . . . 40

5 Application hints . . . 41
5.1 Soldering information . . . 42
5.2 High-current wiring effects . . . 42

6 Digital interfaces . . . 43
6.1 I^2C serial interface . . . 43
6.1.1 I^2C operation . . . 44
6.2 SPI bus interface . . . 46
6.2.1 Accelerometer SPI write . . . 47
6.2.2 Accelerometer SPI read in 3-wire mode . . . 48
6.2.3 Magnetometer SPI write . . . 49
6.2.4 Magnetometer SPI write in 3-wire mode . . . 50

7 Register mapping . . . 51

8 Register description . . . 54
8.1 Module_8bit_A (0Ch) . . . 54
8.2 WHO_AM_I_A (0Fh) . . . 54
8.3 CTRL1_A (20h) . . . 54
8.4 CTRL2_A (21h) . . . 56
8.5 CTRL3_A (22h) . . . 57
8.6 CTRL4_A (23h) . . . 58
8.7 CTRL5_A (24h) . . . 58
8.8 FIFO_CTRL_A (25h) . . . 59

8.9 OUT_T_A (26h) . . . 60
8.10 STATUS_A (27h) . . . 60
8.11 OUT_X_L_A (28h) . . . 61
8.12 OUT_X_H_A (29h) . . . 61
8.13 OUT_Y_L_A (2Ah) . . . 61
8.14 OUT_Y_H_A (2Bh) . . . 61
8.15 OUT_Z_L_A (2Ch) . . . 62
8.16 OUT_Z_H_A (2Dh) . . . 62
8.17 FIFO_THS_A (2Eh) . . . 62
8.18 FIFO_SRC_A (2Fh) . . . 62
8.19 FIFO_SAMPLES_A (30h) . . . 63
8.20 TAP_6D_THS_A (31h) . . . 63
8.21 INT_DUR_A (32h) . . . 64
8.22 WAKE_UP_THS_A (33h) . . . 64
8.23 WAKE_UP_DUR_A (34h) . . . 65
8.24 FREE_FALL_A (35h) . . . 65
8.25 STATUS_DUP_A (36h) . . . 66
8.26 WAKE_UP_SRC_A (37h) . . . 67
8.27 TAP_SRC_A (38h) . . . 67
8.28 6D_SRC_A (39h) . . . 68
8.29 FUNC_SRC_A (3Eh) . . . 68
8.30 FUNC_CTRL_A (3Fh) . . . 69
8.31 OFFSET_X_REG_L_M (45h) and OFFSET_X_REG_H_M (46h) . . . 69
8.32 OFFSET_Y_REG_L_M (47h) and OFFSET_Y_REG_H_M (48h) . . . 69
8.33 OFFSET_Z_REG_L_M (49h) and OFFSET_Z_REG_H_M (4Ah) . . . 69
8.34 WHO_AM_I_M (4Fh) . . . 69
8.35 CFG_REG_A_M (60h) . . . 70
8.36 CFG_REG_B_M (61h) . . . 71
8.37 CFG_REG_C_M (62h) . . . 72
8.38 INT_CTRL_REG_M (63h) . . . 72
8.39 INT_SOURCE_REG_M (64h) . . . 73
8.40 INT_THS_L_REG_M (65h) . . . 73
8.41 INT_THS_H_REG_M (66h) . . . 73

8.42 STATUS_REG_M (67h) 74
8.43 OUTX_L_REG_M, OUTX_H_REG_M (68h - 69h) 74
8.44 OUTY_L_REG_M, OUTY_H_REG_M (6Ah - 6Bh) 75
8.45 OUTZ_L_REG_M, OUTZ_H_REG_M (6Ch - 6Dh) 75

9 Package information 76
9.1 LGA-12 package information 76
9.2 LGA-12 packing information 77

10 Revision history 79

List of tables

Table 1. Device summary . . . 1
Table 2. Pin description . . . 12
Table 3. Sensor characteristics . . . 13
Table 4. Temperature sensor characteristics . . . 15
Table 5. Electrical characteristics . . . 15
Table 6. SPI slave timing values . . . 17
Table 7. I^2C slave timing values (standard and fast mode) . . . 18
Table 8. I^2C slave timing values (fast mode plus and high speed) . . . 18
Table 9. Absolute maximum ratings . . . 20
Table 10. RMS noise of operating modes . . . 22
Table 11. Current consumption of operating modes . . . 22
Table 12. Operating mode and turn-on time . . . 23
Table 13. Maximum ODR in single measurement mode (HR and LP modes) . . . 23
Table 14. Accelerometer operating modes . . . 29
Table 15. Low-pass filter in low-power, high-resolution and high-frequency modes . . . 30
Table 16. Current consumption of operating modes . . . 30
Table 17. Accelerometer LPF cutoff frequency . . . 31
Table 18. Number of samples to be discarded . . . 35
Table 19. Pin status . . . 42
Table 20. Serial interface pin description . . . 43
Table 21. I^2C terminology . . . 43
Table 22. Transfer when master is writing one byte to slave . . . 44
Table 23. Transfer when master is writing multiple bytes to slave . . . 44
Table 24. Transfer when master is receiving (reading) one byte of data from slave . . . 44
Table 25. Transfer when master is receiving (reading) multiple bytes of data from slave . . . 45
Table 26. SAD+Read/Write patterns . . . 45
Table 27. SAD + Read/Write patterns . . . 45
Table 28. Register map . . . 51
Table 29. Module_8bit_A register . . . 54
Table 30. Module_8bit_A register description . . . 54
Table 31. WHO_AM_I_A register default values . . . 54
Table 32. CTRL1_A register . . . 54
Table 33. CTRL1_A register description . . . 54
Table 34. ODR register setting: power down (PD) and low power (LP) . . . 54
Table 35. ODR register setting: high resolution (HR) and high frequencies (HF) . . . 55
Table 36. CTRL2_A register . . . 56
Table 37. CTRL2_A register description . . . 56
Table 38. CTRL3_A register . . . 57
Table 39. CTRL3_A register description . . . 57
Table 40. Self-test mode selection . . . 57
Table 41. CTRL4_A register . . . 58
Table 42. CTRL4_A register description . . . 58
Table 43. CTRL5_A register . . . 58
Table 44. CTRL5_A register description . . . 58
Table 45. FIFO_CTRL_A register . . . 59
Table 46. FIFO_CTRL_A register description . . . 59
Table 47. FIFO mode selection . . . 59
Table 48. OUT_T_A register . . . 60

Table 49. OUT_T_A register description . . . 60
Table 50. STATUS_A register . . . 60
Table 51. STATUS_A register description . . . 60
Table 52. OUT_X_L_A register default values . . . 61
Table 53. OUT_X_H_A register default values . . . 61
Table 54. OUT_Y_L_A register default values . . . 61
Table 55. OUT_Y_H_A register default values . . . 61
Table 56. OUT_Z_L_A register default values . . . 62
Table 57. OUT_Z_H_A register default values . . . 62
Table 58. FIFO_THS_A register . . . 62
Table 59. FIFO_SRC_A register . . . 62
Table 60. FIFO_SRC register description . . . 63
Table 61. FIFO_SAMPLES_A register . . . 63
Table 62. FIFO_SAMPLES_A register description . . . 63
Table 63. TAP_6D_THS_A register . . . 63
Table 64. TAP_6D_THS_A register description . . . 63
Table 65. 4D/6D threshold setting FS @ 2 g . . . 63
Table 66. INT_DUR_A register . . . 64
Table 67. INT_DUR_A register description . . . 64
Table 68. WAKE_UP_THS_A register . . . 64
Table 69. WAKE_UP_THS_A register description . . . 64
Table 70. WAKE_UP_DUR_A register . . . 65
Table 71. WAKE_UP_DUR_A register description . . . 65
Table 72. FREE_FALL_A register . . . 65
Table 73. FREE_FALL_A register description . . . 65
Table 74. FREE_FALL_A threshold decoding @ 2 g FS . . . 65
Table 75. STATUS_DUP_A register . . . 66
Table 76. STATUS_DUP_A register description . . . 66
Table 77. WAKE_UP_SRC_A register . . . 67
Table 78. WAKE_UP_SRC_A register description . . . 67
Table 79. TAP_SRC_A register . . . 67
Table 80. TAP_SRC_A register description . . . 67
Table 81. 6D_SRC_A register . . . 68
Table 82. 6D_SRC_A register description . . . 68
Table 83. FUNC_SRC_A register . . . 68
Table 84. FUNC_SRC_A register description . . . 68
Table 85. FUNC_CTRL_A register . . . 69
Table 86. FUNC_CTRL_A register description . . . 69
Table 87. CFG_REG_A_M register . . . 70
Table 88. CFG_REG_A_M register description . . . 70
Table 89. Output data rate configuration . . . 70
Table 90. System mode . . . 70
Table 91. CFG_REG_B_M register . . . 71
Table 92. CFG_REG_B_M register description . . . 71
Table 93. Digital low-pass filter . . . 71
Table 94. CFG_REG_C_M register . . . 72
Table 95. CFG_REG_C_M register description . . . 72
Table 96. INT_CRTL_REG_M register . . . 72
Table 97. INT_CTRL_REG_M register description . . . 72
Table 98. INT_SOURCE_REG_M register . . . 73
Table 99. INT_SOURCE_REG_M register description . . . 73
Table 100. INT_THS_L_REG_M register . . . 73

Table 101. INT_THS_L_REG_M register description . . . 73
Table 102. INT_THS_H_REG_M register . . . 73
Table 103. INT_THS_H_REG_M register description . . . 73
Table 104. STATUS_REG_M register . . . 74
Table 105. STATUS_REG_M register description . . . 74
Table 106. OUTX_L_REG_M register . . . 74
Table 107. OUTX_H_REG_M register . . . 74
Table 108. OUTY_L_REG_M register . . . 75
Table 109. OUTY_H_REG_M register . . . 75
Table 110. OUTZ_L_REG_M register . . . 75
Table 111. OUTZ_H_REG_M register . . . 75
Table 112. Reel dimensions for carrier tape of LGA-12 package . . . 78
Table 113. Document revision history . . . 79

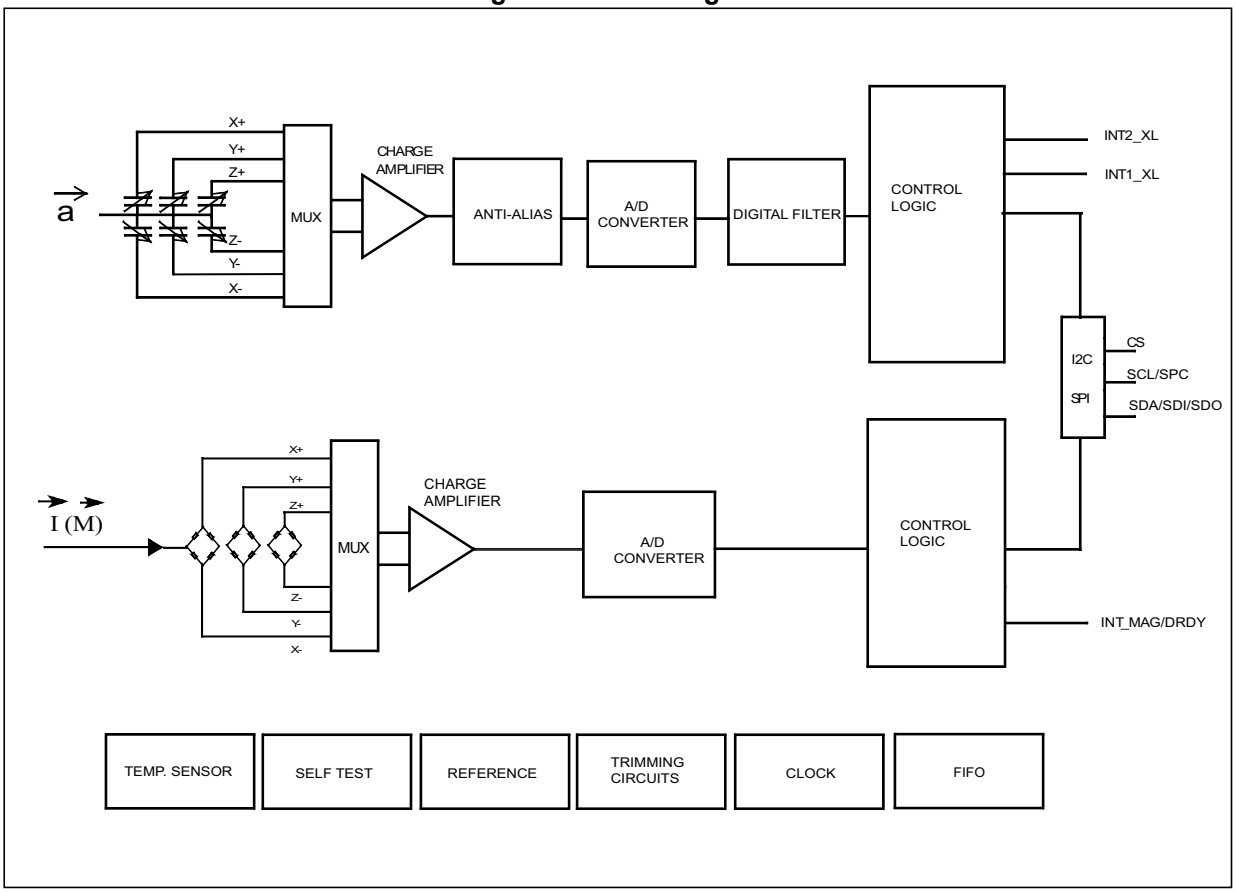
List of figures

Figure 1. Block diagram . . . 10
Figure 2. Pin connections . . . 11
Figure 3. SPI slave timing diagram . . . 17
Figure 4. I^2C slave timing diagram . . . 19
Figure 5. Interrupt function . . . 25
Figure 6. Magnetometer self-test procedure . . . 28
Figure 7. Accelerometer sampling chain . . . 31
Figure 8. Accelerometer slope filter . . . 32
Figure 9. Accelerometer self-test procedure . . . 34
Figure 10. Continuous-to-FIFO mode . . . 37
Figure 11. Trigger event to FIFO for Continuous-to-FIFO mode . . . 38
Figure 12. Bypass-to-Continuous mode . . . 39
Figure 13. Trigger event to FIFO for Bypass-to-Continuous mode . . . 39
Figure 14. Module-to-FIFO mode example . . . 40
Figure 15. ISM303DAC electrical connections . . . 41
Figure 16. Read and write protocol . . . 46
Figure 17. Accelerometer SPI write protocol . . . 47
Figure 18. Accelerometer multiple byte SPI write protocol (2-byte example) . . . 47
Figure 19. Accelerometer SPI read protocol in 3-wire mode . . . 48
Figure 20. Magnetometer SPI write protocol . . . 49
Figure 21. Magnetometer multiple byte SPI write protocol (2-byte example) . . . 49
Figure 22. Magnetometer SPI read protocol in 3-wire mode . . . 50
Figure 23. LGA-12 2x2x1 mm package outline and mechanical data . . . 76
Figure 24. Carrier tape information for LGA-12 package . . . 77
Figure 25. LGA-12 package orientation in carrier tape . . . 77
Figure 26. Reel information for carrier tape of LGA-12 package . . . 78

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

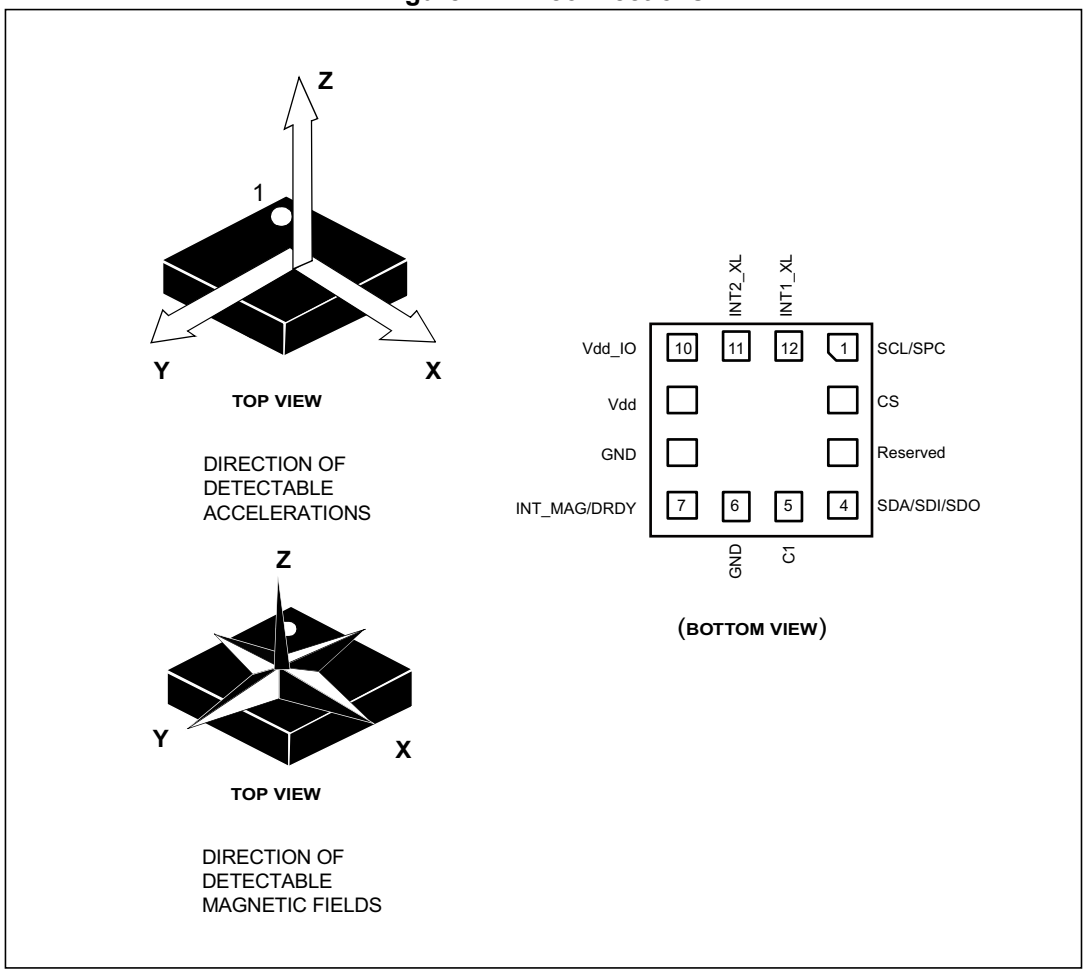


Table 2. Pin description

Pin#	Name	Function
1	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
2	CS	I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
3	Reserved	Reserved, connected to GND
4	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	C1	Capacitor connection (C1 = 220 nF)
6	GND	0 V
7	INT_MAG/DRDY	Magnetometer interrupt/data-ready signal
8	GND	0 V
9	Vdd	Power supply
10	Vdd_IO	Power supply for I/O pins
11	INT2_XL	Accelerometer interrupt 2
12	INT1_XL	Accelerometer interrupt 1

2 Module specifications

2.1 Sensor characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted [a].

Noise density is the same for all ODR.

Table 3. Sensor characteristics

Symbol	Parameter	Test conditions	Min.(1)	Typ.(2)	Max.(1)	Unit
LA_FS	Linear acceleration measurement range			±2		*g*
				±4		
				±8		
				±16		
M_FS	Magnetic dynamic range(3)		±25	±49.152		gauss
LA_So	Sensitivity 16-bit(4)(5)	@ FS ±2 *g*	-7%	0.061	+7%	mg/digit
		@ FS ±4 *g*	-7%	0.122	+7%	
		@ FS ±8 *g*	-7%	0.244	+7%	
		@ FS ±16 *g*	-7%	0.488	+7%	
M_So	Magnetic sensitivity(5)		-10%	1.5	+10%	mgauss/ LSB
LA_TCSo	Linear acceleration sensitivity change vs. temperature(6)			0.01		%/°C
M_TCSo	Magnetic sensitivity change vs. temperature(6)			±0.03		%/°C
LA_TyOff	Typical zero-*g* level offset accuracy(7)(8)		-80	±30	+80	mg
M_TyOff	Magnetic sensor offset	With offset cancellation(9)(10)	-60	0	+60	mgauss
LA_TCOff	Zero-*g* level change vs. temp.(6)	Max. delta from 25 °C		±0.2		mg/°C
M_TCOff	Magnetic sensor offset change vs. temp.	With offset cancellation(9)	-0.3		+0.3	mgauss/ °C
LA_AN	Noise density - high-performance mode (HR or HF mode)(11)	@ FS ±2 *g*		120		µg/√Hz
		@ FS ±4 *g*		150		
		@ FS ±8 *g*		200		
		@ FS ±16 *g*		300		
LA_RMS	RMS noise - low-power mode(12)	@ FS ±2 *g*		6.3		mg(RMS)
		@ FS ±4 *g*		8.2		
		@ FS ±8 *g*		11		
		@ FS ±16 *g*		17		

a. The product is factory calibrated at 1.8 V. The operational power supply range is from 1.71 V to 1.98 V.

Table 3. Sensor characteristics (continued)

Symbol	Parameter	Test conditions	Min.(1)	Typ.(2)	Max.(1)	Unit
M_R	Magnetic RMS noise(13)	High-performance mode		3	5	mgauss (RMS)
ST	Self-test positive difference(14) (accelerometer only)		70		1500	mg
M_ST	Magnetic self-test(15)		15		500	mgauss
Top	Operating temperature range		-40		+85	°C

1. Min/Max values are based on characterization results, not tested in production and not guaranteed.
2. Typical specifications are not guaranteed.
3. The typical value of the magnetic dynamic range applies when the magnetic field is fully aligned with one of the sensitive axes. In presence of a stray field in the cross-axis direction, the magnetic dynamic range (max module) can decrease down to the min value.
4. Sensitivity calculated at 16-bit.
5. Values after calibration test and trimming.
6. Measurements are performed in a uniform temperature setup and they are based on characterization data in a limited number of samples, not measured during final test for production.
7. Typical zero-*g* level offset value after calibration and trimming.
8. Offset can be eliminated by enabling the slope filter.
9. Based on characterization data on a limited number of samples, not measured during final test for production.
10. Excluding drift due to magnetic shock.
11. Noise density is the same for all ODR.
12. RMS noise is the same for all ODR.
13. With low-pass filter or offset cancellation enabled.
14. “Self-test positive difference” is defined as: $\text{OUTPUT[mg]}_{\text{(CTRL3 ST2, ST1 bits=01)}} - \text{OUTPUT[mg]}_{\text{(CTRL3 ST2, ST1 bits=00)}}$.
15. Magnetic “self-test” is defined as $\text{OUTPUT[gauss]}_{\text{(self-test enabled)}} - \text{OUTPUT[gauss]}_{\text{(self-test disabled)}}$.

2.2 Temperature sensor characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted.[b]

Table 4. Temperature sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
TSDr	Temperature sensor output change vs. temp.			1		digit/°C[2]
TODR	Temperature refresh rate			12.5		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. 8-bit resolution.

2.3 Electrical characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted.[b]

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.[1]	Typ.[2]	Max.[1]	Unit
Vdd	Supply voltage		1.71		1.98	V
Vdd_IO	Module power supply for I/O		1.71	1.8	Vdd+0.1	V
LA_Idd_HR	Accelerometer current consumption in high-resolution mode Magnetic sensor in power-down	12.5Hz-6400Hz ODR range		162		µA
LA_Idd_LP	Accelerometer current consumption in low-power mode Magnetic sensor in power-down.	100 Hz ODR		16		µA
		50 Hz ODR		10		µA
		12.5 Hz ODR		6		µA
		1 Hz ODR		4.5		µA
M_Idd_HR	Magnetic current consumption in high-resolution mode Accelerometer in power-down mode	ODR = 100 Hz		1180		µA
M_Idd_LP	Magnetic current consumption in low-power mode[3] Linear accel. in power-down mode	ODR = 10 Hz		25		µA
Idd_PD	Current consumption in power-down			2.5		µA
VIH	Digital high-level input voltage		0.8*Vdd_IO			V
VIL	Digital low-level input voltage				0.2*Vdd_IO	V
VOH	High-level output voltage	IOH = 4 mA	Vdd_IO - 0.2			V

b. The product is factory calibrated at 1.8 V.The operational power supply range is from 1.71 V to 1.98 V.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.(1)	Typ.(2)	Max.(1)	Unit
VOL	Low-level output voltage	IOL = 4 mA			0.2	V
T_{OP}	Operating temperature range		-40		+85	°C

1. Min/Max values are based on characterization results, not tested in production and not guaranteed.
2. Typical specifications are not guaranteed.
3. Offset cancellation turned off.

2.4 Communication interface characteristics

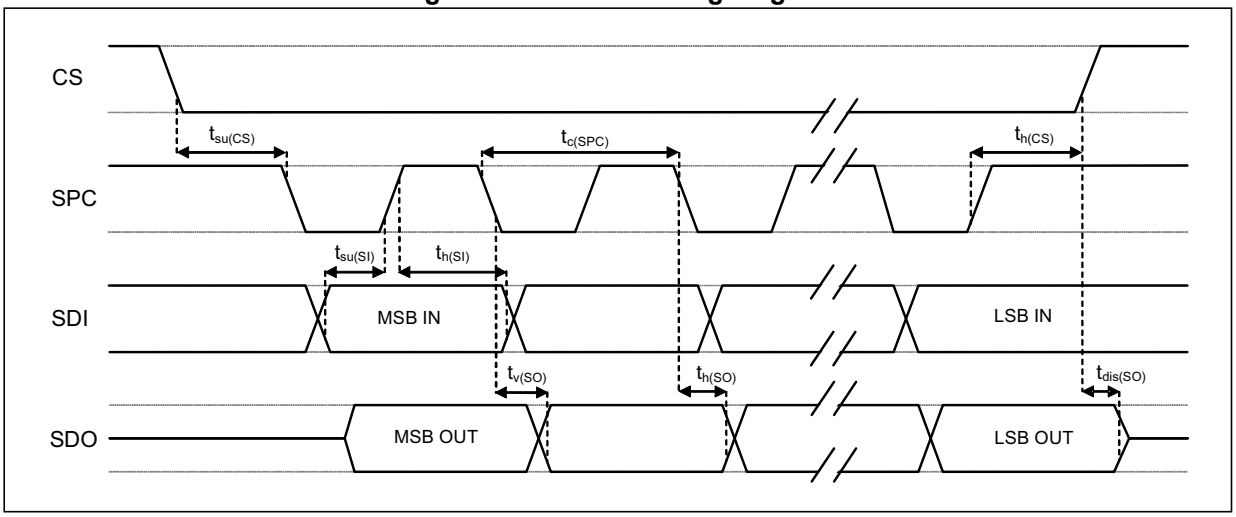
2.4.1 SPI - serial peripheral interface

Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value (1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

Figure 3. SPI slave timing diagram



Note: Values are guaranteed at 10 MHz clock frequency for SPI with 3 wires, based on characterization results, not tested in production.

Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter-IC control interface

Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values (standard and fast mode)

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	Low period of the SCL clock	4.7		1.3		µs
$t_{w(SCLH)}$	High period of the SCL clock	4.0		0.6		
$t_{su(SDA)}$	Data setup time	250		100		ns
$t_{h(SDA)}$	Data hold time	0	3.45	0	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		
$t_{su(SR)}$	Setup time for a repeated START condition	4.7		0.6		
$t_{su(SP)}$	Setup time for STOP condition	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

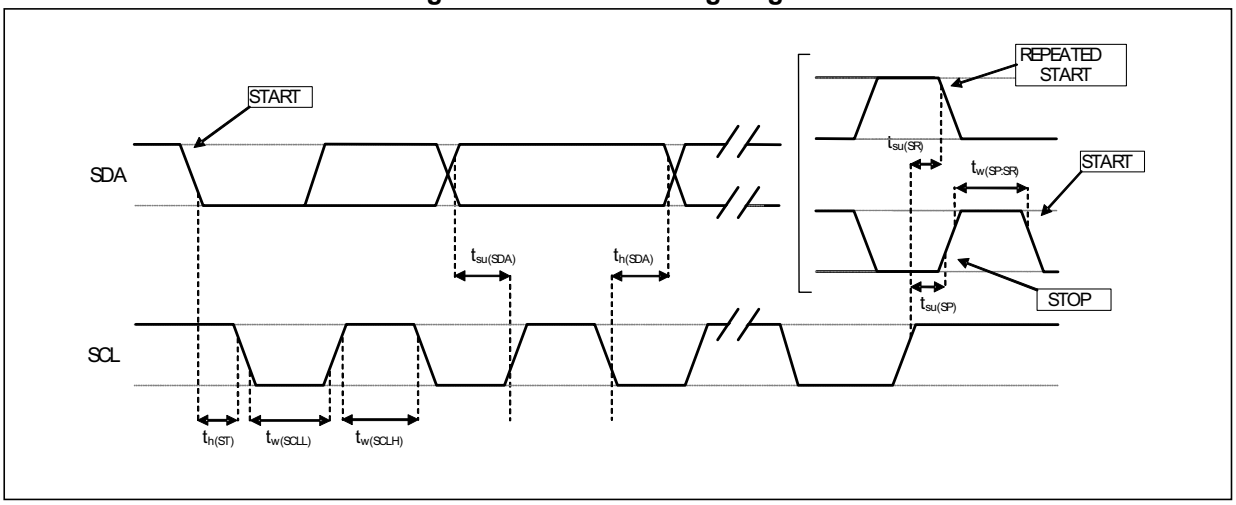
1. Data based on standard I²C protocol requirement, not tested in production.

Table 8. I²C slave timing values (fast mode plus and high speed)

Symbol	Parameter	I²C fast mode plus(1)		I²C high speed(1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	1	0	3.4	MHz
$t_{w(SCLL)}$	Low period of the SCL clock	0.5		0.16		µs
$t_{w(SCLH)}$	High period of the SCL clock	0.26		0.06		
$t_{su(SDA)}$	Data setup time	50		10		ns
$t_{h(SDA)}$	Data hold time	0		0	0.07	µs
$t_{h(ST)}$	START condition hold time	0.26		0.16		
$t_{su(SR)}$	Setup time for a repeated START condition	0.26		0.16		
$t_{su(SP)}$	Setup time for STOP condition	0.26		0.16		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	0.5				

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 9. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 2.2	V
Vdd_IO	I/O pins supply voltage	-0.3 to 2.2	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 1.8 V)	3000 for 0.5 ms	*g*
		10000 for 0.2 ms	*g*
A_{UNP}	Acceleration (any axis, unpowered)	3000 for 0.5 ms	*g*
		10000 for 0.2 ms	*g*
M_{EF}	Maximum exposed field	10000	gauss
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection (HBM)	2	kV

Note: Supply voltage on any pin should never exceed 2.2 V.



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 Terminology

3.1 Sensitivity

3.1.1 Linear acceleration sensor sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

3.1.2 Magnetic sensor sensitivity

Sensitivity describes the ratio of the output digital data expressed in LSB units and the applied magnetic field expressed in mG (milligauss). It can be measured, for example, by applying a known magnetic field along one axis and measuring the digital output of the device.

3.2 Zero-*g* level

The zero-*g* level offset (LA_TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on the X-axis and 0 *g* on the Y-axis whereas the Z-axis will measure 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset. Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little with temperature, see *Table 3* "Zero-*g* level change vs. temperature" (LA_TCOff). The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a population of sensors.

3.3 Zero-*gauss* level

Zero-*g*auss level offset (M_TyOff) describes the deviation of an actual output signal from the ideal output if no magnetic field is present.

3.4 Magnetic dynamic range

The magnetic dynamic range of the sensor can be fully exploited when the applied magnetic field is entirely aligned with one of the sensitive axes of the sensor.

In presence of a stray field in the cross-axis direction, the exploitable magnetic dynamic range (maximum module) can decrease.

4 Functionality

4.1 Magnetometer

4.1.1 Magnetometer power modes

The ISM303DAC magnetometer provides two different power modes: high-resolution and low-power modes.

The tables below summarize the magnetometer RMS noise values and current consumption in different product configurations.

When the low-pass filter is enabled, the bandwidth is reduced while noise performance is improved without any increase in power consumption.

Table 10. RMS noise of operating modes

CFG_REG_B_M[LPF] or CFG_REG_B_M[OFF_CANC]	(CFG_REG_A_M [LP = 0]) high-resolution mode		(CFG_REG_A_M [LP = 1]) low-power mode	
	BW [Hz]	Noise RMS [mg]	BW [Hz]	Noise RMS [mg]
0 (disable)	ODR/2	4.5	ODR/2	9
1 (enable)	ODR/4	3	ODR/4	6

Table 11. Current consumption of operating modes

ODR (Hz)	Current consumption (µA) (CFG_REG_A_M [LP] = 0) high-resolution CFG_REG_B_M [OFF_CANC] = 0	Current consumption (µA) (CFG_REG_A_M [LP] = 1) low-power CFG_REG_B_M [OFF_CANC] = 0	Current consumption (µA) (CFG_REG_A_M [LP] = 0) high-resolution CFG_REG_B_M [OFF_CANC] = 1	Current consumption (µA) (CFG_REG_A_M [LP] = 1) low-power CFG_REG_B_M [OFF_CANC] = 1
10	100	25	125	55
20	200	50	240	105
50	475	125	590	255
100	950	250	1180	505

The following table summarizes the turn-on time of the magnetometer in the two different power modes with the offset cancellation function enabled or disabled (see *Section 4.1.2: Magnetometer offset cancellation*).

Table 12. Operating mode and turn-on time

Operating mode	Turn-on time	
CFG_REG_A_M[LP]	CFG_REG_A_M[OFF_CANC = 0]	CFG_REG_A_M[OFF_CANC = 1]
0 (high-resolution)	9.4 ms	9.4 ms + 1/ODR
1 (low-power)	6.4 ms	6.4 ms + 1/ODR

The ISM303DAC offers single measurement mode in both high-resolution and low-power modes.

Single measurement mode is enabled by writing bits MD[1:0] to '01' in *CFG_REG_A_M (60h)*.

In single measurement mode, once the measurement has been performed, the DRDY pin is set to high, data is available in the output register and the ISM303DAC is automatically configured in idle mode by setting the MD[1] bit to '1'.

Single measurement is independent of the programmed ODR but depends on the frequency at which the MD[1:0] bits are written by the microcontroller/application processor.

Maximum ODR frequency achievable in single mode measurement is given in the following table.

Table 13. Maximum ODR in single measurement mode (HR and LP modes)

Maximum ODR	Power mode (CFG_REG_A_M[LP])
100 Hz	High resolution (LP = ‘0’)
150 Hz	Low power (LP = ‘1’)

In single measurement mode, for ODR < 10 Hz, current consumption can be calculated with the following formula:

(Current_consumption_10Hz - Current_consumption_in_power_down) / (10 Hz / ODR) + Current_consumption_in_power_down

Where Current_consumption_in_power_down and Current_consumption_10Hz can be found, respectively, in *Table 5* and *Table 11*.

4.1.2 Magnetometer offset cancellation

The ISM303DAC is based on AMR technology: a set pulse is needed to set an initial operating condition.

Offset cancellation is the result of performing a set and reset pulse in the magnetic sensor and it can be enabled to remove the intrinsic sensor offset.

The offset cancellation technique is defined as follows:

$$H_{out} = \frac{H_n - H_{n-1}}{2}$$

where H_n and H_{n-1} are two consecutive magnetic field measurements, one after a set pulse, the other after a reset pulse.

Considering a magnetic offset (H_{off}), the two magnetic field measurements are:

- Set: $H_n = H + H_{off}$
- Reset: $H_{n-1} = -H + H_{off}$

The offset is cancelled according to the offset cancellation technique:

$$H_{out} = \frac{H_n - H_{n-1}}{2} = \frac{2H + H_{off} + (-H_{off})}{2} = H$$

If the device is operating in Continous mode, the offset cancellation is enabled by setting the OFF_CANC bit to 1 in *CFG_REG_B_M (61h)*. In this case, set/reset pulses are continuously performed; a set pulse is applied to one measurement, a reset pulse is applied to the next measurement. If the offset cancellation is disabled (OFF_CANC = 0) and Continuous mode is selected, the set pulse frequency can be configured by setting the Set_FREQ bit in *CFG_REG_B_M (61h)*. If Set_FREQ is set to 0, the set pulse is released every 63 ODR, otherwise if Set_FREQ is set to 1, the set pulse is released only at power-on from Idle mode (a set of the magnetic sensor is performed anyway, even if the offset cancellation is disabled).

If the device is operating in Single mode, in order to enable the offset cancellation, both OFF_CANC and OFF_CANC_ONE_SHOT bits must be set to 1 in *CFG_REG_B_M (61h)*. Enabling these bits, the impulse polarity is inverted between a single read and the next one. While offset cancellation is automatically managed by the device in Continuous mode, if this feature is enabled in Single mode, the user has to remove the offset manually using the formula below:

$$H_{out} = \frac{H_n - H_{n-1}}{2}$$

Offset cancellation using single reads is effective only if the reads are close in time, thus ensuring the offset does not drift between two consecutive reads.

4.1.3 Magnetometer interrupt

In LSM303AH magnetometer interrupt signal generation is based on the comparison between data and a programmable threshold.

To enable the interrupt function, in INT_CTRL_REG_M register (63h) the "IEN" bit must be set to '1'.

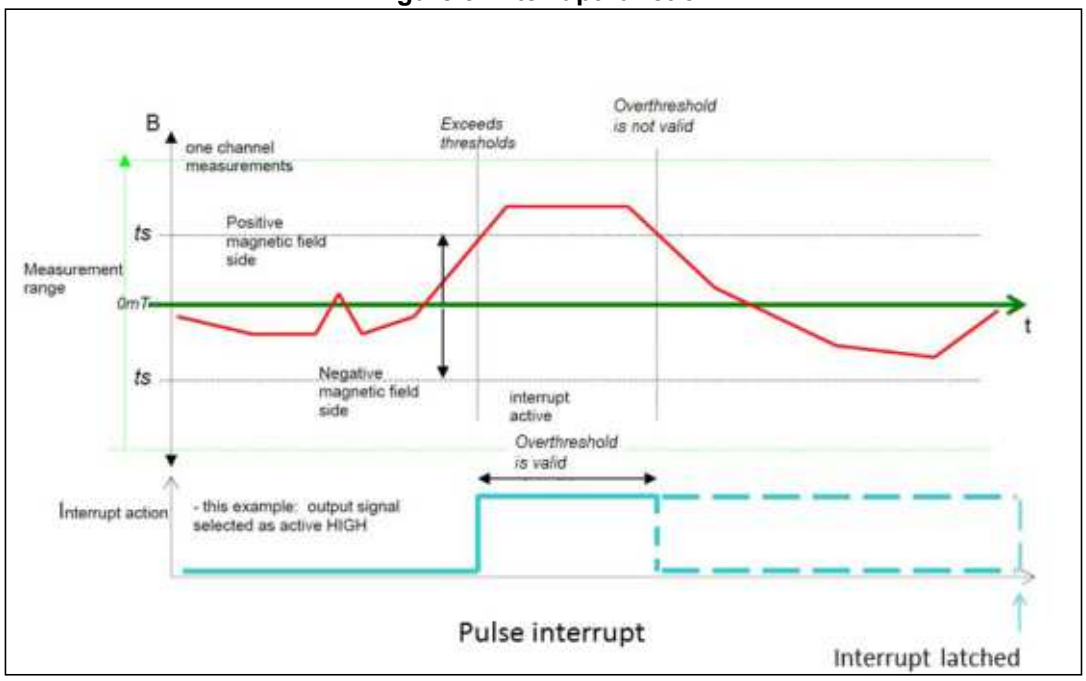
In the LSM303AH the user can select the axis/axes in which the interrupt function can be enabled. In order to do this, the XIEN, YIEN, and ZIEN bits in *INT_CTRL_REG_M (63h)* need be set properly.

The threshold value can be programmed by setting the *INT_THS_L_REG_M (65h)* and *INT_THS_H_REG_M (66h)* registers.

The threshold is expressed in absolute value as a 15-bit unsigned number. The threshold has the same sensitivity as the magnetic data.

When magnetic data exceeds the positive or the negative threshold, the interrupt signal is generated and the information about the type of interrupt is stored in the *INT_SOURCE_REG_M (64h)* register. In particular, when magnetic data exceeds the positive threshold the P_TH_S_axis bit is set to '1', while if data exceeds the negative threshold the N_TH_S_axis bit is set to '1'. If magnetic data lay between the positive and the negative thresholds, no interrupt signal is released.

Figure 5. Interrupt function



Two different approaches for the interrupt function are available:

- Typical: comparison is between magnetic data read by the sensor and the programmable threshold;
- Advanced: comparison is made between magnetic data after hard-iron correction and the programmable threshold.

These approaches are configurable by setting the INT_on_DataOFF bit in *CFG_REG_B_M (61h)*.

If INT_on_DataOFF is set to '0' the typical approach is selected, otherwise if it is set to '1' the advanced approach is selected.

Two different interrupts are available:

- Pulsed interrupt signal: it goes high when the magnetic data exceed one of the two thresholds and goes low when the magnetic data are between the two thresholds. This kind of interrupt is selected by setting the IEL bit in *INT_CTRL_REG_M (63h)* to '0'.
- Latched interrupt signal: it goes high when the data exceed one of the two thresholds but is reset only once the source register is read and not when the magnetic data returns between the two thresholds. This kind of interrupt is selected by setting the IEL bit in *INT_CTRL_REG_M (63h)* to '1'.

The interrupt signal polarity can be set using the IEA bit in *INT_CTRL_REG_M (63h)*.

If IEA is set to '1' then the interrupt signal is active high, while if it is set to '0' the interrupt signal is active low.

In order to drive the interrupt signal from the DRDY pad, the INT_MAG_PIN bit in *CFG_REG_C_M (62h)* must be set to '1'.

4.1.4 Magnetometer hard-iron compensation

Hard-iron distortion occurs when a magnetic object is placed near the magnetometer and appears as a permanent bias in the sensor's outputs.

The hard-iron correction consists of compensating magnetic data from hard-iron distortion.

The operation is defined as follows:

$H_{out} = H_{read} – H_{HI}$

where:

- H_{read} is the generic uncompensated magnetic field data, as read by the sensor;
- H_{HI} is the hard-iron distortion field;
- H_{out} is the compensated magnetic data.

The computation of the hard-iron distortion field should be performed by an external processor. After the computation of the hard iron-distortion field has been performed, the measured magnetic data can be compensated.

The ISM303DAC offers the possibility of storing hard-iron data inside six dedicated registers from 45h to 4Ah.

Each register contains eight bits so that the hard-iron data can be expressed as a 16-bit two's complement number. The OFFSET_axis_REG_H registers contain the MSBs of the hard-iron data, while the OFFSET_axis_REG_L registers contain the LSBs.

Hard-iron data have the same format and weight of the magnetic output data. The hard-iron values stored in dedicated registers are automatically subtracted from the output data.

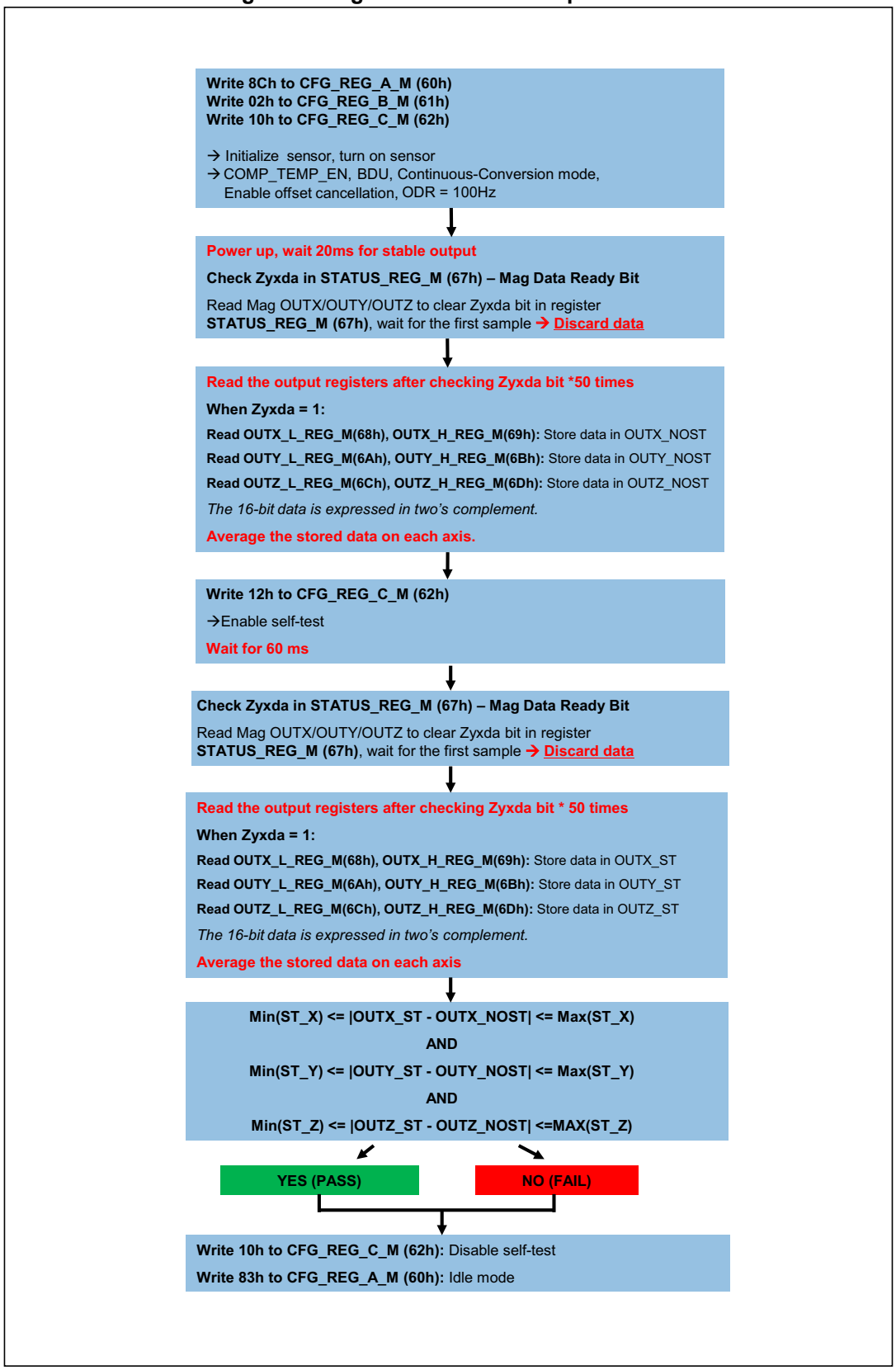
4.1.5 Magnetometer self-test

The self-test function is available for the magnetic sensor. When the magnetic self-test is enabled, a current is forced into a coil inside the device. This current will generate a magnetic field that will produce a variation of the magnetometer output signals. If the output signals change within the amplitude limits specified in *Table 3* then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

When the magnetometer self-test is activated, the sensor output level is given by the algebraic sum of the signals produced by the magnetic field acting on the sensor and by the forced current.

The self-test procedure is described in the following figure.

Figure 6. Magnetometer self-test procedure



4.2 Accelerometer

4.2.1 Accelerometer power modes

The ISM303DAC accelerometer provides two different power modes: high-resolution (including high-frequency mode) and low-power modes.

The following tables summarize the selection of the different operating modes as well as the low-pass filter and current consumption.

Table 14. Accelerometer operating modes

CTRL1_A(ODR[3:1])	CTRL1_A(HF_ODR)	ODR selection [Hz]	Bit resolution	Mode
Accelerometer low-power mode				
0000	-	-	-	PD
1000	-	1	10	LP
1001	-	12.5		
1010	-	25		
1011	-	50		
1100	-	100		
1101	-	200		
1110	-	400		
1111	-	800		
Accelerometer high-resolution mode				
0001	-	12.5	14	HR
0010	-	25		
0011	-	50		
0100	-	100		
0101	0	200		
0110	0	400		
0111	0	800		
0101	1	1600	12	HF
0110	1	3200		
0111	1	6400		

Table 15. Low-pass filter in low-power, high-resolution and high-frequency modes

ODR [Hz]	LPF cutoff [Hz]
Low-power mode	
800	3200
400	
200	
100	
50	
25	
12.5	
1	
High-resolution mode	
800	355
400	177
200	88
100	44
50	22
25	11
12.5	5.5
High-frequency mode	
6400	2840
3200	1420
1600	710

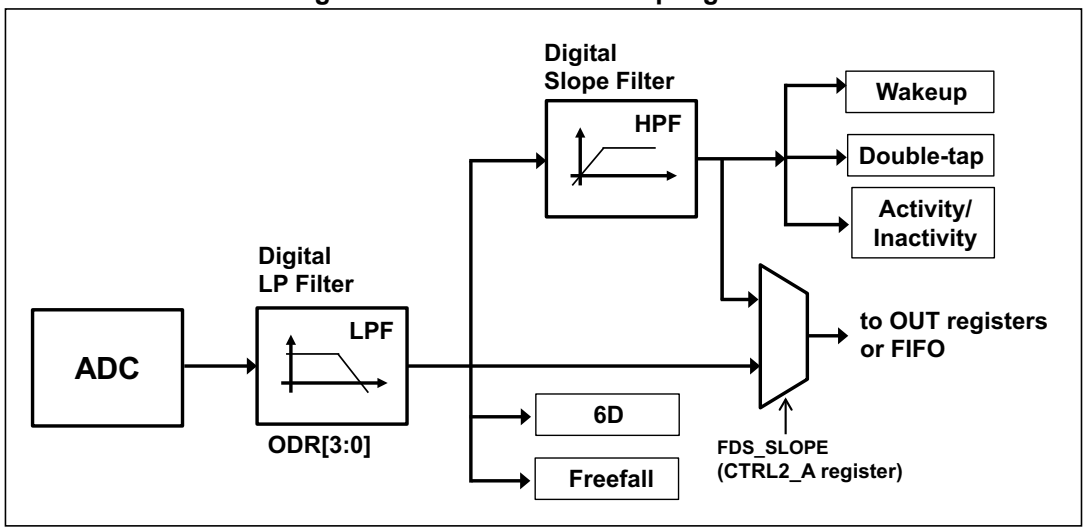
Table 16. Current consumption of operating modes

ODR (Hz)	Typical current consumption in high-resolution/high-frequency mode [µA]	Typical current consumption in low-power mode [µA]
1	-	4.5
12.5	162	6
25		7.5
50		10
100		16
200		26.5
400		48.5
800		92.5
1600		
3200		
6400		

4.2.2 Accelerometer bandwidth

The accelerometer sampling chain (*Figure 7: Accelerometer sampling chain*) is represented by a cascade of a few blocks: an ADC converter, a digital low-pass filter and a digital slope filter.

Figure 7. Accelerometer sampling chain



The digital signal is filtered by a low-pass digital filter (LPF) whose cutoff frequency depends on the selected accelerometer ODR, as shown in *Table 17*.

Table 17. Accelerometer LPF cutoff frequency

Mode	ODR selection [Hz]	LPF cutoff [Hz]
LP	1	3200
	12.5	3200
	25	3200
	50	3200
	100	3200
	200	3200
	400	3200
	800	3200
HR	12.5	5.5
	25	11
	50	22
	100	44
	200	88
	400	177
	800	355
HF	1600	710
	3200	1420
	6400	2840

The selection of the signal (LPF or HPF) which is sent to the OUT registers is determined by the FDS_SLOPE bit of *CTRL2_A (21h)* register. When it is logic '1', the HPF signal is selected, LPF otherwise.

The signal that is sent to the digital functions (wakeup, double-tap, activity/inactivity and 6D orientation) is always the HPF signal. Anti-aliasing filtering is guaranteed by the ADC sampling frequency and the digital LPF cutoff frequency. Anti-aliasing filtering is available in HR/HF mode only. When the accelerometer is in LP mode, the circuitry is periodically turned on/off (reducing power consumption) with a fixed on-time and a period that is a function of the selected ODR. For this reason the LPF cutoff is fixed to 3.2 kHz, so the user must take care to select the proper ODR value Vs application sampling frequency in order to avoid aliasing (based on the noise characteristics of the system in use).

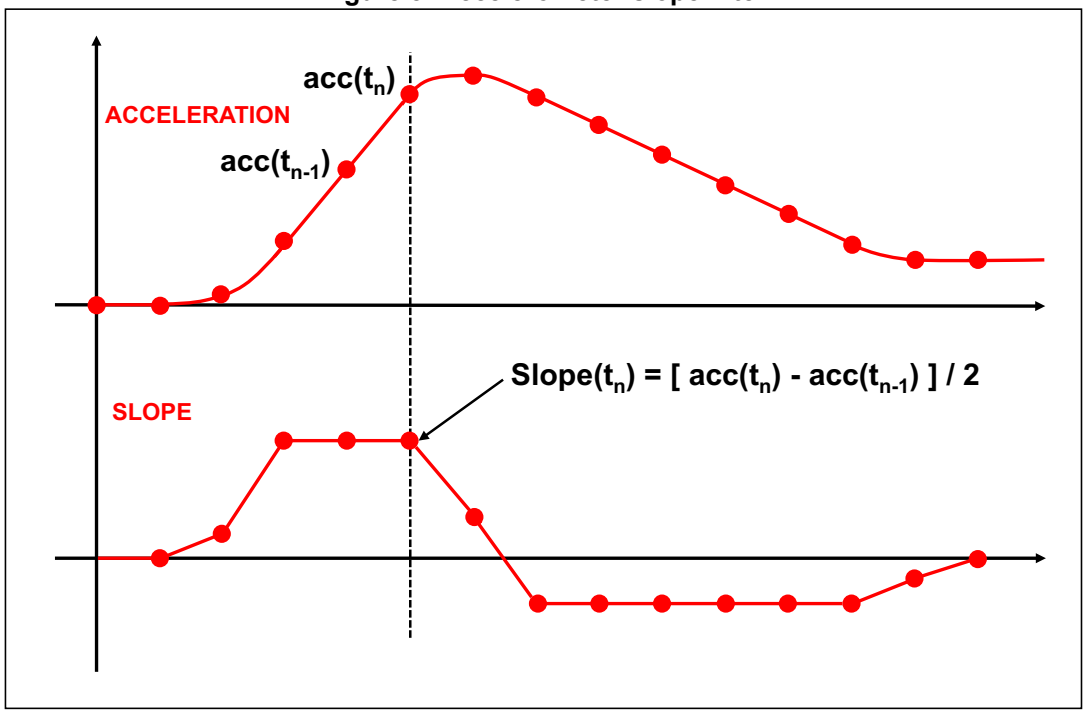
Accelerometer slope filter

As shown in *Figure 8*, the ISM303DAC device embeds a digital slope filter which is used for wakeup and single/double-tap features. The slope filter output data is computed using the following formula:

$$slope(t_n) = [\ acc(t_n) - acc(t_{n-1})\ ] / 2$$

An example of a slope data signal is illustrated in *Figure 8*.

Figure 8. Accelerometer slope filter



Slope filter bandwidth is ~ ODR/4 and its data is available in the output registers and FIFO by setting the FDS_SLOPE bit of *CTRL2_A (21h)* to '1'.

4.2.3 Accelerometer 6D / 4D orientation detection

The ISM303DAC includes 6D / 4D orientation detection which applies only to the accelerometer.

In this configuration the interrupt is generated when the device is stable in a known direction. In 4D configuration, detection of the position of the Z-axis is disabled.

4.2.4 Accelerometer activity/inactivity function

The Activity/Inactivity recognition function allows reducing the power consumption of the system in order to develop new smart applications and is applicable only to the accelerometer block of the device.

When the Activity/Inactivity recognition function is activated, the ISM303DAC is able to automatically go to 12.5 Hz sampling rate and to wake up as soon as the interrupt event has been detected, increasing the output data rate and bandwidth.

With this feature the system may be efficiently switched from low-power mode to full performance depending on user-selectable positioning and acceleration events, thus ensuring power saving and flexibility.

The Activity/Inactivity recognition function is activated by writing the desired threshold in the *WAKE_UP_THS_A (33h)* register. The high-pass filter is automatically enabled.

If the device is in Sleep (Inactivity) mode, when at least one of the axes exceeds the threshold in the *WAKE_UP_THS_A (33h)* the device goes into Sleep-to-Wake (as Wake-Up).

Activity/Inactivity threshold and duration can be configured in the control registers:

WAKE_UP_THS_A (33h)

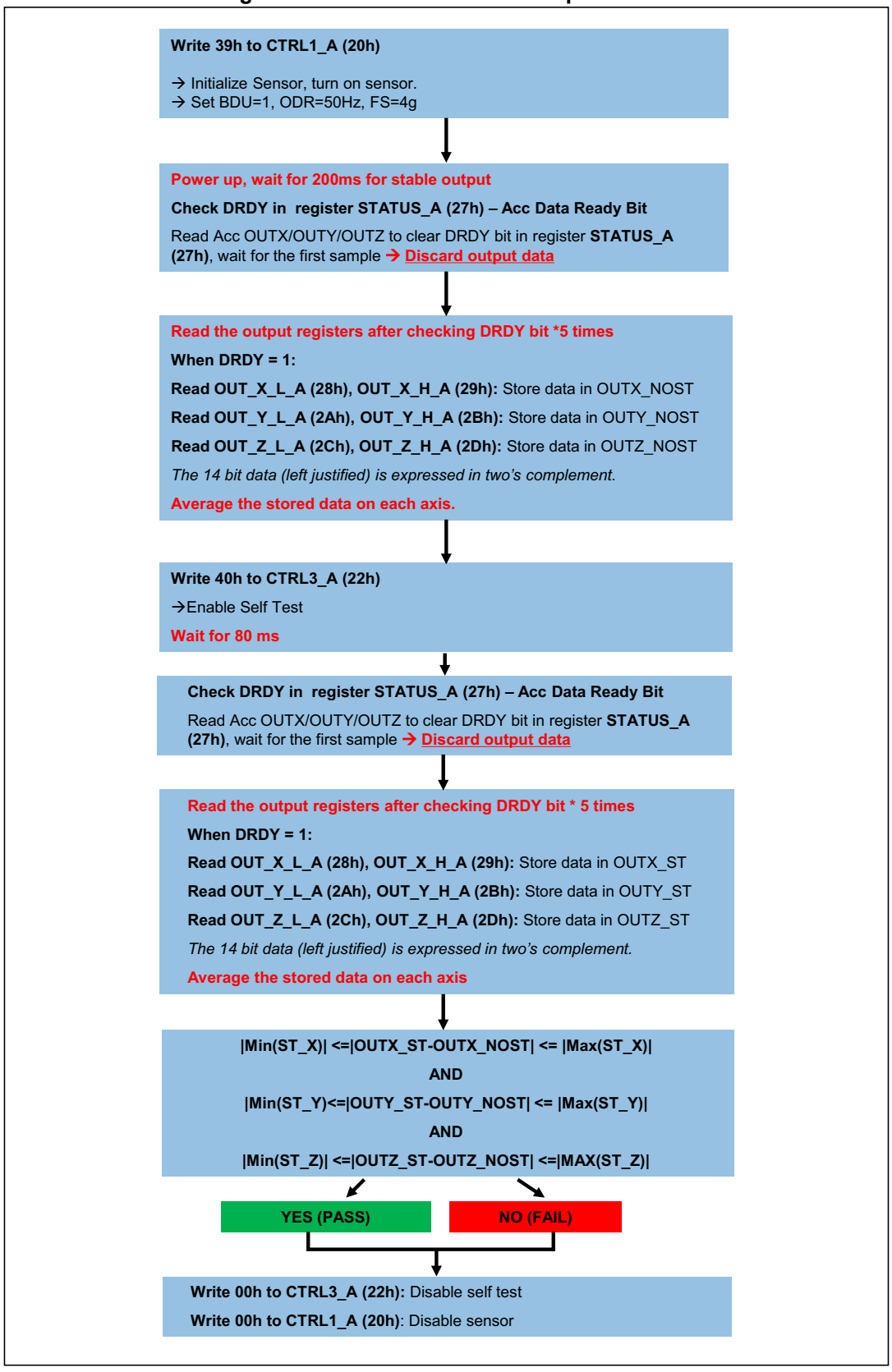
WAKE_UP_DUR_A (34h)

4.2.5 Accelerometer self-test

The self-test allows the user to check the sensor functionality without moving it. When the self-test is enabled, an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs will exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified inside *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

The self-test procedure is described in the following figure.

Figure 9. Accelerometer self-test procedure



4.2.6 Accelerometer data stabilization time vs. ODR setting

The data stabilization time required when an ODR change is applied in order to have valid usable data depends on the ODR selected and accelerometer setting.

The table below provides the number of samples to be discarded in order to obtain valid usable data for the accelerometer.

Table 18. Number of samples to be discarded

ODR [Hz]	HF	HR	LP
6400	6	-	-
3200	2	-	-
1600	1	-	-
800	-	1	0
400	-	1	0
200	-	1	0
100	-	1	0
50	-	0	0
25	-	0	0
12.5	-	0	0
1	-	-	0

4.3 IC interface

The complete measurement chain is composed of a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage using an analog-to-digital converter.

The acceleration and magnetic data may be accessed through an I^2C/SPI interface, thus making the device particularly suitable for direct interfacing with a microcontroller.

The ISM303DAC features a data-ready signal which indicates when new sets of measured acceleration and magnetic data are available, thus simplifying data synchronization in the digital system that uses the device.

4.4 FIFO

The FIFO buffer applies only to the accelerometer. The ISM303DAC embeds 256 slots of 14-bit data FIFO for each of the three output channels, X, Y and Z of the acceleration module. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

The internal FIFO allows collecting 256 samples (14-bit size data) for each axis or storing the output of the module computation up to 768 samples (14-bit size data).

This buffer can work according to the following 5 different modes:

- Bypass mode
- FIFO mode
- Continuous-to-FIFO
- Bypass-to-Continuous
- Continuous

Each mode is selected by the FIFO_MODE bits in the *FIFO_CTRL_A (25h)* register.

Programmable FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the *FIFO_SRC_A (2Fh)* and *FIFO_SAMPLES_A (30h)* registers and can be set to generate dedicated interrupts on the INT1 and INT2 pins using the *CTRL4_A (23h)* and *CTRL5_A (24h)* registers.

FIFO_SRC_A (2Fh) (FIFO_FTH) goes to '1' when the number of unread samples *FIFO_SRC_A (2Fh)* and *FIFO_SAMPLES_A (30h)* (Diff[8:0]) is greater than or equal to FTH [7:0] in *FIFO_THS_A (2Eh)*.

If FTH [7:0] is equal to '0', *FIFO_SRC_A (2Fh)* (FIFO_FTH) goes to '0'.

FIFO_SRC_A (2Fh) (FIFO_OVRN) is equal to '1' if a FIFO slot is overwritten.

FIFO_SRC_A (2Fh) and *FIFO_SAMPLES_A (30h)* (Diff[8:0]) contain stored data levels of unread samples. When Diff[8:0] is equal to '000000000', FIFO is empty. When Diff[8:0] is equal to '100000000', FIFO is full and the unread samples are 256.

To guarantee the correct acquisition of data during the switching into and out of FIFO mode, the first sample acquired must be discarded.

When the FIFO threshold status flag is '0'-logic, FIFO filling is lower than the threshold level and when '1'-logic, FIFO filling is equal to or higher than the threshold level.

4.4.1 Bypass mode

In Bypass mode (*FIFO_CTRL_A (25h)* (FMODE [2:0])= 000), the FIFO is not operational, no data is collected in FIFO memory, and it remains empty with the only actual sample available in the output registers.

Bypass mode is also used to reset the FIFO when in FIFO mode.

For each channel only the first address is used. When new data is available, the old data is overwritten.

4.4.2 FIFO mode

In FIFO mode (*FIFO_CTRL_A (25h)* (FMODE [2:0])= 001) data from the X, Y and Z channels are stored in the FIFO until it is full, when 256 unread samples are stored in memory, data collecting is stopped.

To reset the FIFO content, Bypass mode should be written in the *FIFO_CTRL_A (25h)* register, setting the FMODE [2:0] bits to '000'. After this reset command, it is possible to restart FIFO mode, writing the value '001' in *FIFO_CTRL_A (25h)* (FMODE [2:0]).

The FIFO buffer can memorize 256 slots of X, Y and Z data.

4.4.3 Continuous mode

Continuous mode (*FIFO_CTRL_A (25h)* (FMODE[2:0] = 110) provides a continuous FIFO update: when 256 unread samples are stored in memory, as new data arrives the oldest data is discarded and overwritten by the newer.

A FIFO threshold flag *FIFO_CTRL_A (25h)* (FIFO_FTH) is asserted when the number of unread samples in FIFO is greater than or equal to *FIFO_THS_A (2Eh)* (FTH[7:0]).

It is possible to route *FIFO_CTRL_A (25h)*(FTH) to the INT1 pin by writing the INT1_FTH bit to '1' in register *CTRL4_A (23h)* or to the INT2 pin by writing the INT2_FTH bit to '1' in register *CTRL5_A (24h)*.

If an overrun occurs, the oldest sample in FIFO is overwritten and the FIFO_OVR flag in *FIFO_SRC_A (2Fh)* is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in *FIFO_SRC_A (2Fh)* and *FIFO_SAMPLES_A (30h)* (Diff[8:0]).

4.4.4 Continuous-to-FIFO mode

In Continuous-to-FIFO mode *FIFO_CTRL_A (25h)* (FMODE [2:0] = 011), FIFO operates in Continuous mode and FIFO mode starts upon an internal trigger event. When the FIFO is full, data collecting is stopped.

Figure 10. Continuous-to-FIFO mode

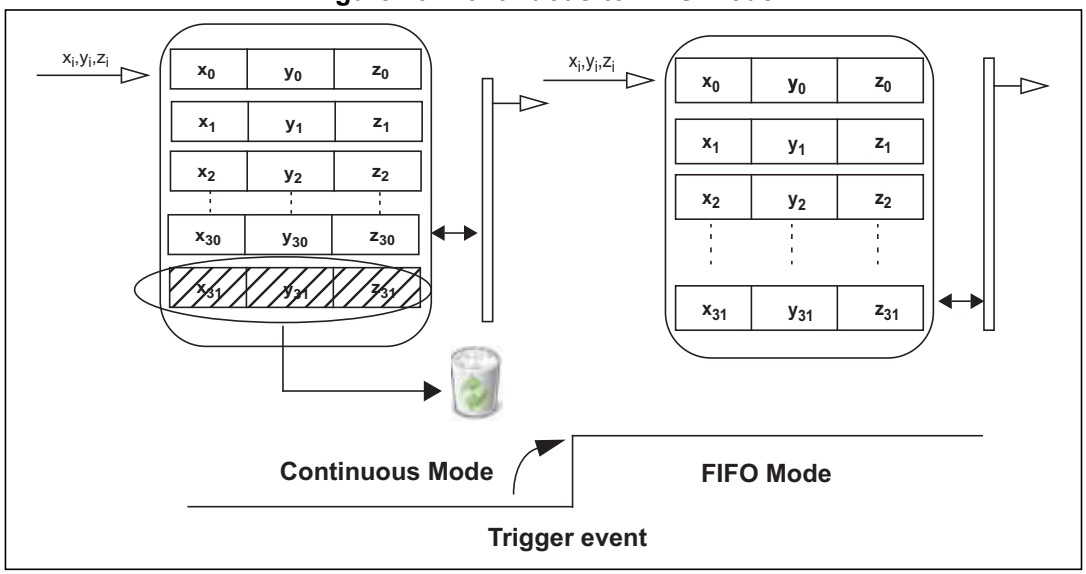
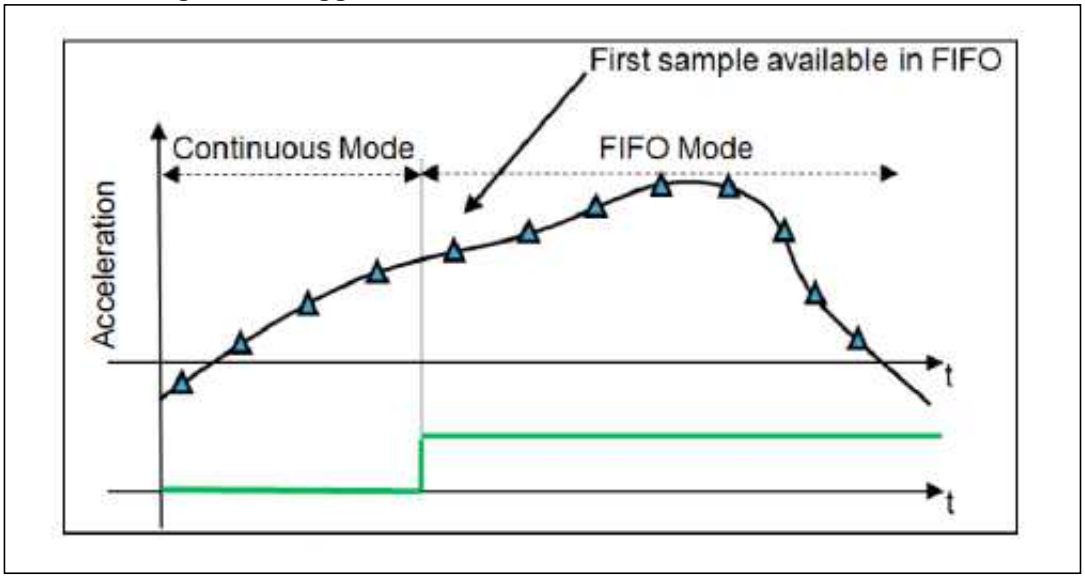


Figure 11. Trigger event to FIFO for Continuous-to-FIFO mode



4.4.5 Bypass-to-Continuous mode

In Bypass-to-Continuous mode (*FIFO_CTRL_A (25h)*(FMODE[2:0] = '100'), data measurement storage inside FIFO starts in Continuous mode upon an internal trigger event, then the sample that follows the trigger is available in FIFO.

Figure 12. Bypass-to-Continuous mode

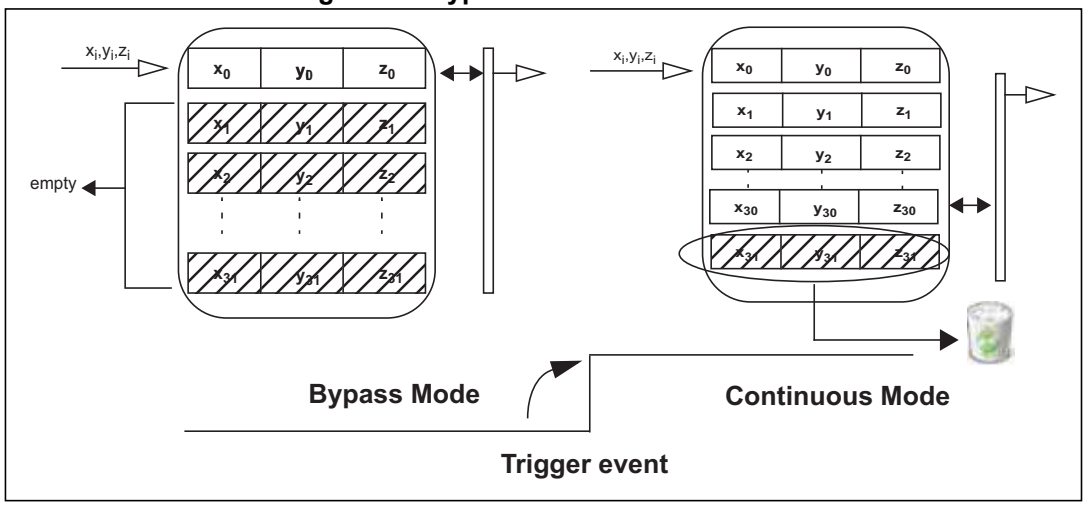
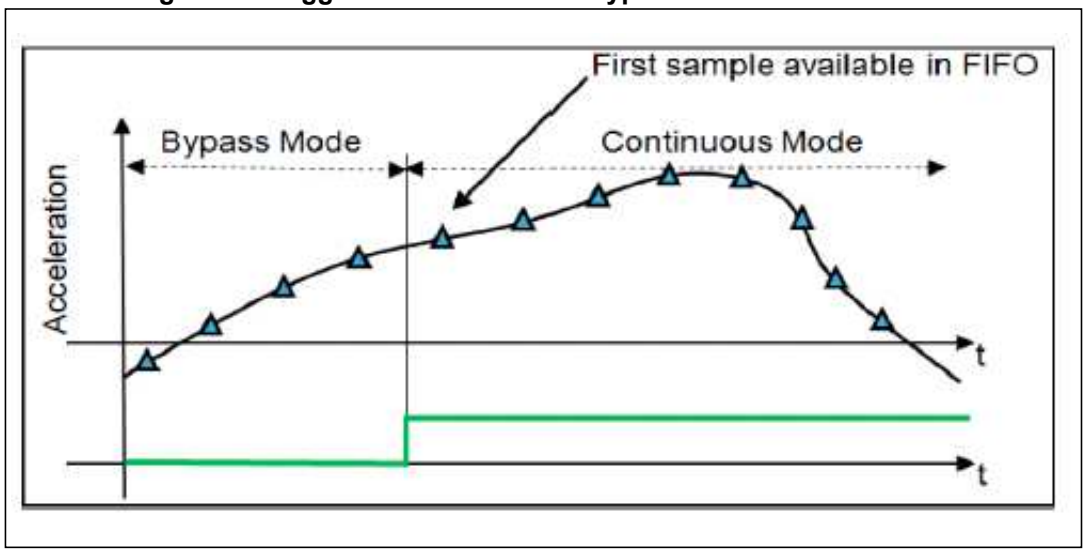


Figure 13. Trigger event to FIFO for Bypass-to-Continuous mode



4.4.6 Module-to-FIFO

When the MODULE_TO_FIFO bit in the *FIFO_CTRL_A (25h)* register is set to '1', the 14-bit magnitude of the vector of the current axes is sent as FIFO input instead of axes data. X-, Y- and Z-axis data are replaced with 3 times the adjacent data generated by the module routine, as shown in *Figure 14*, so a row of FIFO is written every 3 axes data ready.

The module routine must be previously enabled by writing to the *FUNC_CTRL_A (3Fh)* register.

The module data in FIFO can be read as output data in the registers 28h-2Dh.

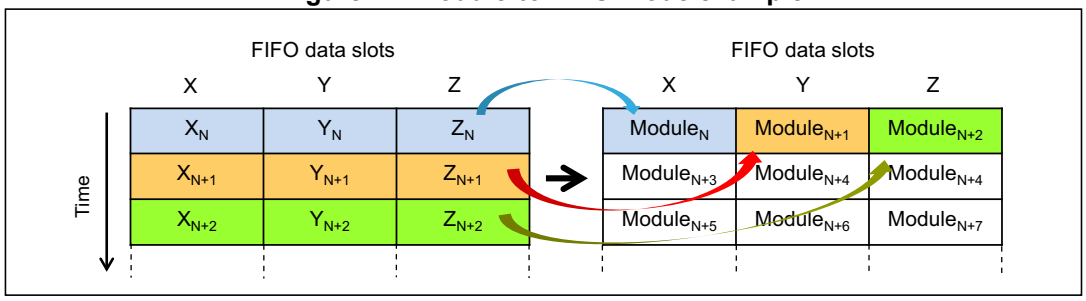
The ISM303DAC calculates the vector sum of the acceleration of the X-, Y-, Z-axis using the following formula:

module (14-bit) = $Sqrt(x^2+y^2+z^2)$

The implementation is based on an approximation of this formula (error below noise level).

As shown in *Figure 14*, when module-to-FIFO is enabled, each row of FIFO contains 3 values of the module, related to 3 consecutive ODR.

Figure 14. Module-to-FIFO mode example



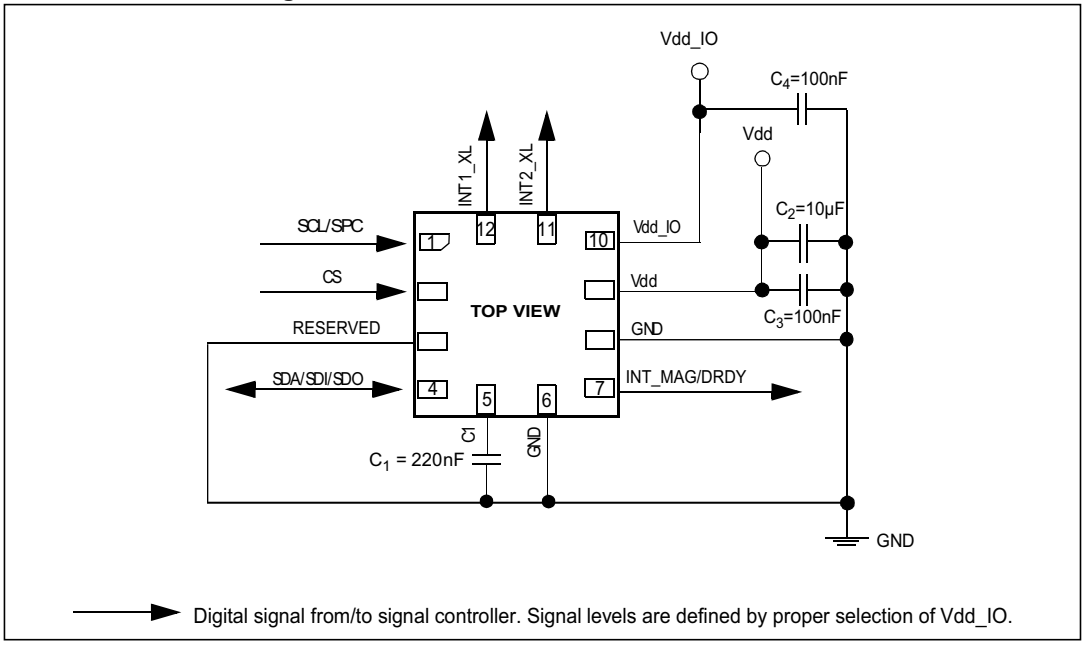
4.5 Factory calibration

The IC interface is factory calibrated for sensitivity (LA_So, M_GN), Zero-*g* level (LA_TyOff) and Zero-*gauss* level (M_TyOff).

The trim values are stored inside the device in nonvolatile memory. Anytime the device is turned on, the trim parameters are downloaded into the registers to be used during active operation. This allows using the device without further calibration.

5 Application hints

Figure 15. ISM303DAC electrical connections



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 9 of the device (common design practice).

It is possible to remove Vdd, maintaining Vdd_IO, without blocking the communication bus, in this condition the measurement chain is powered off.

The following recommendations apply to capacitor C1:

- It must be connected as close as possible to pins 5 and 6 since very high current pulses flow from C1 to pin 5 and 6. This avoid problems caused by inductive effects due to the length of the copper strips.
- It is highly recommended to use low ESR (max 200 mOhm)

The functionality of the device and the measured acceleration data are selectable and accessible through the I^2C or SPI interfaces. When using the I^2C, CS must be tied high (i.e. connected to Vdd_IO).

The functions, the threshold and the timing of the three interrupt pins (INT1_XL, INT2_XL, and INT_MAG/DRDY) can be completely programmed by the user through the I^2C/SPI interface.

Table 19. Pin status

Pin#	Name	Function	Status
1	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)	Default: input without pull-up
2	CS	I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)	Default: input without pull-up
3	Reserved	Reserved, connected to GND	
4	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)	Default: (SDA) input without pull-up
5	C1	Capacitor connection (C1 = 220 nF)	External cap, voltage forced by the device
6	GND	0 V	
7	INT_MAG/DRDY	Magnetometer interrupt/data-ready signal	Default: output high impedance
8	GND	0 V	
9	Vdd	Power supply	
10	Vdd_IO	Power supply for I/O pins	
11	INT2_XL	Accelerometer interrupt 2	Default: output forced to ground
12	INT1_XL	Accelerometer interrupt 1	Default: output forced to ground

Note: In order to program INT_MAG/DRDY as a push-pull output, write the INT_MAG bit to 1 in CFG_REG_C_M (62h).

5.1 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standards.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Land pattern and soldering recommendations are available at www.st.com.

5.2 High-current wiring effects

High current in wiring and printed circuit traces can be culprits in causing errors in magnetic field measurements for compassing.

Conductor-generated magnetic fields will add to the Earth’s magnetic field, leading to errors in compass heading computation.

Keep currents higher than 10 mA a few millimeters away from the sensor IC.

6 Digital interfaces

The registers embedded inside the ISM303DAC may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW-configured to operate in 3-wire interface mode.

The serial interfaces are mapped to the same pins. To select/exploit the I^2C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 20. Serial interface pin description

Pin name	Pin description
CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)

6.1 I^2C serial interface

The ISM303DAC I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 21. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free, both the lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with the normal mode.

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a high-to-low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the magnetometer block of the ISM303DAC behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represent the actual register address.

The I²C embedded inside the accelerometer block of the ISM303DAC behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent. Once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represent the actual register address while the IF_ADD_INC bit in *CTRL2_A (21h)* defines the increase in the address.

The slave address is completed with a Read/Write bit. If the bit was ‘1’ (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is ‘0’ (Write) the master will transmit to the slave with direction unchanged. *Table 26* explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 22. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 23. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 24. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 25. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low-to-high transition on the SDA line while the SCL line is high is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

Default address:

The accelerometer sensor slave address is 0011101b while magnetic sensor slave address is 0011110b.

The slave addresses are completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes. If the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 26* and *Table 27* explain how the SAD+Read/Write bit patterns are composed, listing all the possible configurations.

Linear acceleration sensor: the default (factory setting) 7-bit slave address is 0011101b.

Table 26. SAD+Read/Write patterns

Command	SAD[6:0]	R/W	SAD+R/W
Read	0011101	1	00111011
Write	0011101	0	00111010

Magnetic field sensor: the default (factory setting) 7-bit slave address is 0011110b.

Table 27. SAD + Read/Write patterns

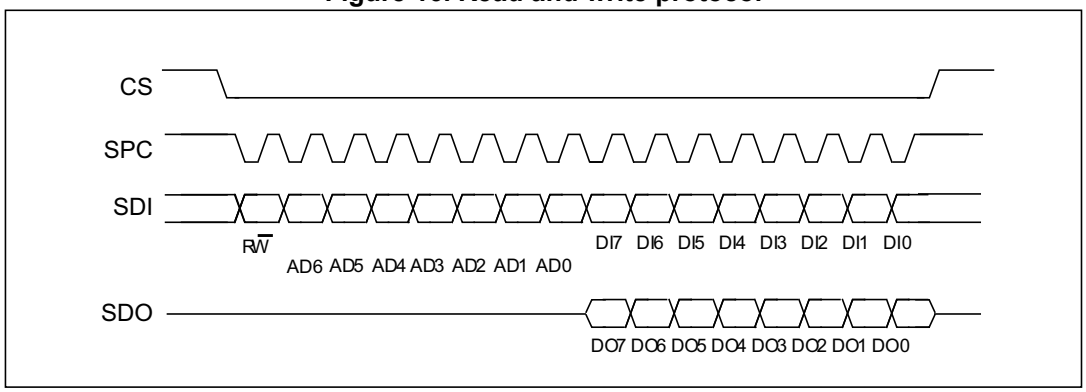
Command	SAD[6:0]	R/W	SAD + R/W
Read	0011110	1	00111101 (3Dh)
Write	0011110	0	00111100 (3Ch)

6.2 SPI bus interface

The ISM303DAC SPI is a bus slave. The SPI allows writing to and reading from the registers of the device.

The serial interface interacts with the application using 3 wires: **CS**, **SPC**, **SDI** and **SDO** (refer to *Table 20*).

Figure 16. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

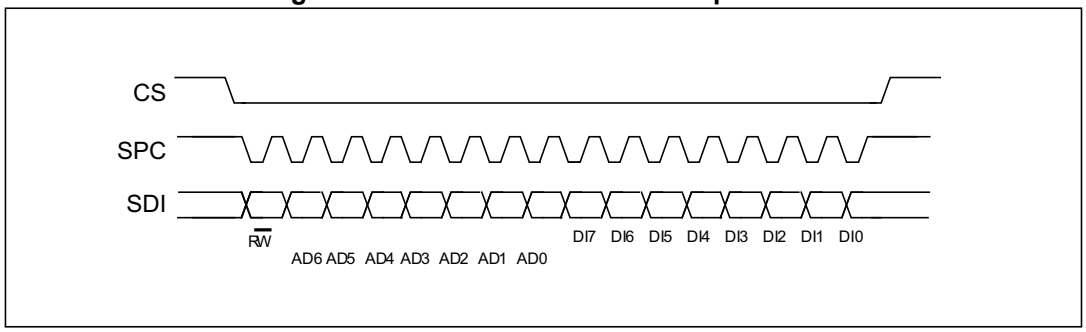
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands additional blocks of 8 clock periods will be added. For the accelerometer when the *CTRL2_A (21h)* (IF_ADD_INC) bit is '0', the address used to read/write data remains the same for every block. When the *CTRL2_A (21h)* (IF_ADD_INC) bit is '1', the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

6.2.1 Accelerometer SPI write

Figure 17. Accelerometer SPI write protocol



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

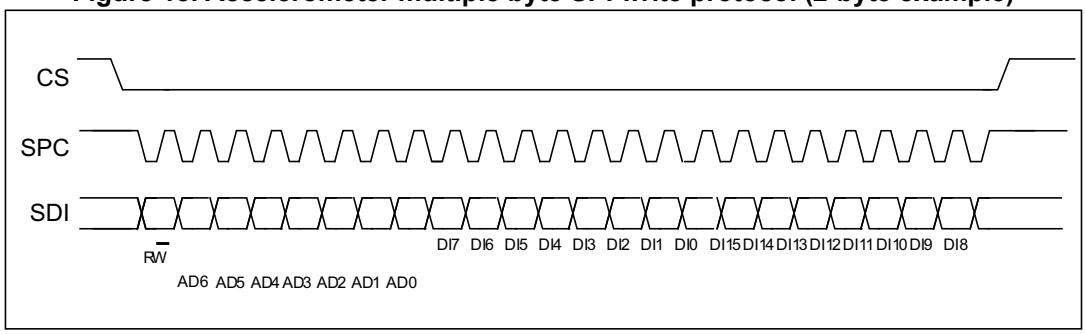
bit 1 -7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Additional data in multiple byte writes.

The accelerometer address auto increment is enabled by default (volatile bit IF_ADD_INC in *CTRL2_A (21h)* must be set to '0' to disable).

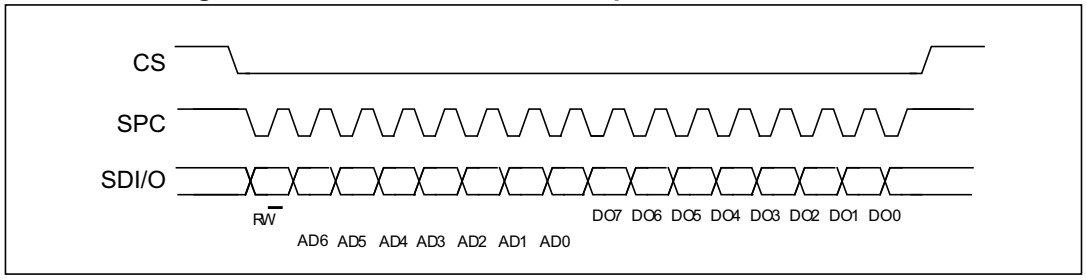
Figure 18. Accelerometer multiple byte SPI write protocol (2-byte example)



6.2.2 Accelerometer SPI read in 3-wire mode

3-wire mode is entered by setting the *CTRL2_A (21h)* (SPI_ENABLE) bit equal to '1' (SPI serial interface read enable).

Figure 19. Accelerometer SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

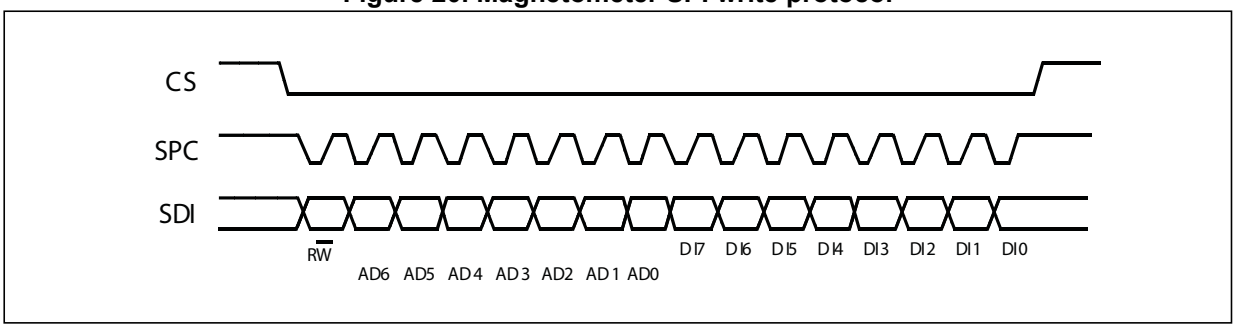
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

The accelerometer address auto increment is enabled by default (volatile bit IF_ADD_INC in *CTRL2_A (21h)* must be set to '0' to disable).

6.2.3 Magnetometer SPI write

Figure 20. Magnetometer SPI write protocol



The SPI write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

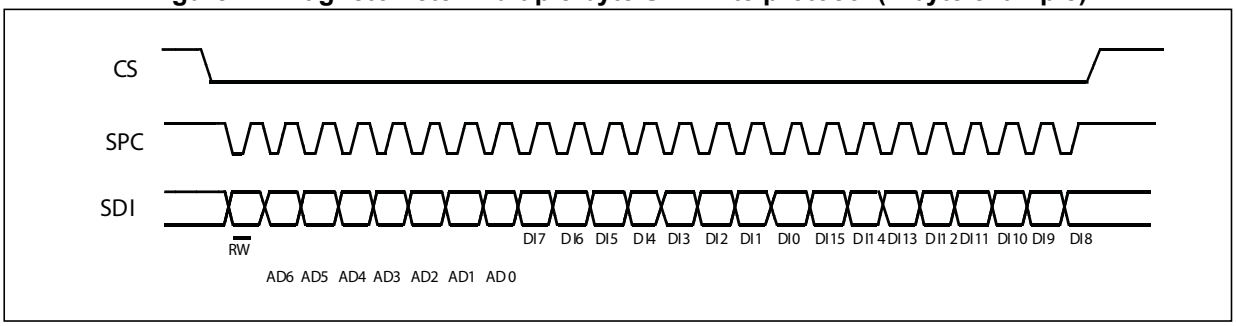
bit 0: WRITE bit. The value is 0.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

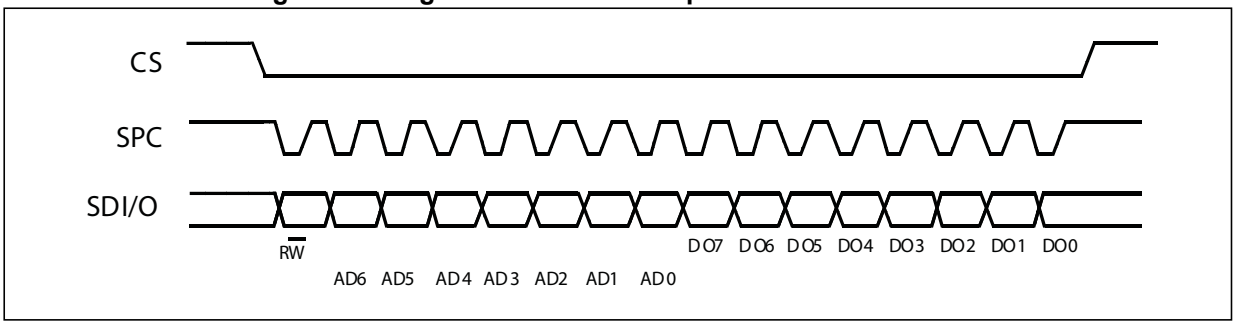
bit 16-... : data DI(...-8). Further data in multiple byte writes.

Figure 21. Magnetometer multiple byte SPI write protocol (2-byte example)



6.2.4 Magnetometer SPI write in 3-wire mode

Figure 22. Magnetometer SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: WRITE bit. The value is 0.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

The multiple read command is available in 3-wire mode.

7 Register mapping

The table given below provides a list of the 8-bit registers embedded in the device and the corresponding addresses. Registers 00h through 3Fh are dedicated to the accelerometer while registers 40h through 6Fh are dedicated to the magnetometer.

Table 28. Register map

Name	Type(1)	Register address		Default	Comment
		Hex	Binary		
RESERVED	-	00-0B		-	RESERVED
Module_8bit_A	R	0C	00001100	output	
RESERVED	-	0D-0E		-	RESERVED
WHO_AM_I_A	R	0F	00001111	01000011	Who I am ID
RESERVED	-	10-1F		-	RESERVED
CTRL1_A	R/W	20	00100000	00000000	Control registers
CTRL2_A	R/W	21	00100001	00000100	
CTRL3_A	R/W	22	00100010	00000000	
CTRL4_A	R/W	23	00100011	00000000	
CTRL5_A	R/W	24	00100100	00000000	
FIFO_CTRL_A	R/W	25	00100101	00000000	FIFO control reg
OUT_T_A	R	26	00100110	output	Temp sensor output
STATUS_A	R	27	00100111	output	Status data register
OUT_X_L_A	R	28	00101000	output	Output registers
OUT_X_H_A	R	29	00101001		
OUT_Y_L_A	R	2A	00101010		
OUT_Y_H_A	R	2B	00101011		
OUT_Z_L_A	R	2C	00101100		
OUT_Z_H_A	R	2D	00101101		
FIFO_THS_A	R/W	2E	00101110	00000000	FIFO registers
FIFO_SRC_A	R	2F	00101111	output	FIFO SRC
FIFO_SAMPLES_A	R/W	30	00110000	00000000	Unread samples stored in FIFO
TAP_6D_THS_A	R/W	31	00110001	00000000	TAP, 4D, 6D threshold
INT_DUR_A	R/W	32	00110010	00000000	Interrupt duration
WAKE_UP_THS_A	R/W	33	00110011	00000000	TAP/D-TAP selection, Inactivity EN, Wakeup threshold

Table 28. Register map (continued)

Name	Type(1)	Register address		Default	Comment
		Hex	Binary		
WAKE_UP_DUR_A	R/W	34	00110100	00000000	Wakeup duration
FREE_FALL_A	R/W	35	00110101	00000000	Free-fall config.
STATUS_DUP_A	R	36	00110110	output	Status register
WAKE_UP_SRC_A	R	37	00110111	output	Wakeup SRC
TAP_SRC_A	R	38	00111000	output	TAP SRC
6D_SRC_A	R	39	00111001	output	6D SRC
RESERVED		3A-3E			
FUNC_CTRL_A	R/W	3F	00000100	00000000	FUNCTION CTRL
RESERVED		40-44			
OFFSET_X_REG_L_M	R/W	45	01000101	00000000	Magnetometer hard-iron registers
OFFSET_X_REG_H_M	R/W	46	01000110	00000000	
OFFSET_Y_REG_L_M	R/W	47	01000111	00000000	
OFFSET_Y_REG_H_M	R/W	48	01001000	00000000	
OFFSET_Z_REG_L_M	R/W	49	01001001	00000000	
OFFSET_Z_REG_H_M	R/W	4A	01001010	00000000	
RESERVED		4B-4C			
WHO_AM_I_M	R	4F	01001111	01000000	Who I am ID
RESERVED		50-5F			
CFG_REG_A_M	R/W	60	01100000	00000011	Magnetometer configuration registers
CFG_REG_B_M	R/W	61	01100001	00000000	
CFG_REG_C_M	R/W	62	01100010	00000000	
INT_CRTL_REG_M	R/W	63	01100011	11100000	Magnetometer interrupt configuration registers
INT_SOURCE_REG_M	R	64	01100100		
INT_THS_L_REG_M	R/W	65	01100101	00000000	
INT_THS_H_REG_M	R/W	66	01100110	00000000	
STATUS_REG_M	R	67	01100111		
OUTX_L_REG_M	R	68	01101000	output	Magnetometer output registers
OUTX_H_REG_M	R	69	01101001	output	
OUTY_L_REG_M	R	6A	01101010	output	
OUTY_H_REG_M	R	6B	01101010	output	
OUTZ_L_REG_M	R	6C	01101100	output	
OUTZ_H_REG_M	R	6D	01101101	output	
RESERVED		6E-6F			

1. R = read-only register, RW = readable/writable register

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

8 Register description

8.1 Module_8bit_A (0Ch)

Module out value (r). This register is a read-only register.

Table 29. Module_8bit_A register

Module_7	Module_6	Module_5	Module_4	Module_3	Module_2	Module_1	Module_0

Table 30. Module_8bit_A register description

Module [7:0]	Module output value (8-bit). Default value: 0

8.2 WHO_AM_I_A (0Fh)

Who_AM_I register (r). This register is a read-only register. Its value is fixed at 43h.

Table 31. WHO_AM_I_A register default values

0	1	0	0	0	0	1	1

8.3 CTRL1_A (20h)

Control register 1 (r/w)

Table 32. CTRL1_A register

ODR3	ODR2	ODR1	ODR0	FS1	FS0	HF_ODR	BDU

Table 33. CTRL1_A register description

ODR [3:0]	Output data rate & power mode selection. Default value: 0000 (see *Table 34*)
FS [1:0]	Full-scale selection. Default value: 00 (00: ±2 *g*; 01: ±16 *g*; 10: ±4 *g*; 11: ±8 *g*)
HF_ODR	High-frequency ODR mode enable. Default value: 0
BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB read)

ODR [3:0] is used to set the power mode and ODR selection. The following table lists the bit settings for power-down mode and each available frequency.

Table 34. ODR register setting: power down (PD) and low power (LP)

ODR[3:0]	HF_ODR	ODR selection [Hz]	Bit resolution	Mode
0000	-	-	-	PD
1000	-	1	10	LP
1001	-	12.5	10	LP
1010	-	25	10	LP

Table 34. ODR register setting: power down (PD) and low power (LP) (continued)

ODR[3:0]	HF_ODR	ODR selection [Hz]	Bit resolution	Mode
1011	-	50	10	LP
1100	-	100	10	LP
1101	-	200	10	LP
1110	-	400	10	LP
1111	-	800	10	LP

Table 35. ODR register setting: high resolution (HR) and high frequencies (HF)

ODR[3:0]	HF_ODR	ODR selection [Hz]	Bit resolution	Mode
0001	-	12.5	14	HR
0010	-	25	14	HR
0011	-	50	14	HR
0100	-	100	14	HR
0101	0	200	14	HR
0110	0	400	14	HR
0111	0	800	14	HR
0101	1	1600	12	HF
0110	1	3200	12	HF
0111	1	6400	12	HF

The BDU bit is used to inhibit the update of the output registers until both upper and lower register parts are read. In default mode (BDU = ‘0’) the output register values are updated continuously. When the BDU is activated (BDU = ‘1’), the content of the output registers is not updated until both MSB and LSB are read which avoids reading values related to different sample times.

8.4 CTRL2_A (21h)

Control register 2 (r/w)

Table 36. CTRL2_A register

BOOT	SOFT_ RESET	0(1)	0(1)	FDS_ SLOPE	IF_ADD_ INC	I2C_ DISABLE	SPI_ ENABLE

1. This bit must be set to '0' for the correct operation of the device.

Table 37. CTRL2_A register description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
SOFT_RESET	Soft reset acts as reset for all control registers, then goes to 0. Default value: 0 (0: disabled; 1: enabled)
FDS_SLOPE	High-pass filter data selection on output register and FIFO. Default value: 0 (0: internal filter bypassed; 1: internal filter enabled on output register and FIFO)
IF_ADD_INC	Register address automatically incremented during multiple byte access with a serial interface (I^2C or SPI). Default value: 1 (0: disabled; 1: enabled)
I2C_DISABLE	Disable I^2C communication protocol. Default value: 0 (0: SPI and I^2C interfaces enabled; 1: I^2C mode disabled)
SPI_ENABLE	3-wire SPI interface read enable. Default value: 0 0: SPI read disabled 1: SPI read enabled

8.5 CTRL3_A (22h)

Control register 3 (r/w)

Table 38. CTRL3_A register

ST2	ST1	TAP_X_EN	TAP_Y_EN	TAP_Z_EN	LIR	H_LACTIVE	PP_OD

Table 39. CTRL3_A register description

ST [2:1]	Self-test enable. Default value: 00 (00: Self-test disabled; Other: see *Table 40*)
TAP_X_EN	Tap recognition on X direction enable. Default value: 0 (0: disabled; 1: enabled)
TAP_Y_EN	Tap recognition on Y direction enable. Default value: 0 (0: disabled; 1: enabled)
TAP_Z_EN	Tap recognition on Z direction enable. Default value: 0 (0: disabled; 1: enabled)
LIR	Latched Interrupt. Switches between latched ('1'-logic) and pulsed ('0'-logic) mode for function source signals and interrupts routed to pins (wakeup, tap, double-tap, tilt, pedometer, significant motion). Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
H_LACTIVE	Interrupt active high, low. Default value: 0 (0: active high; 1: active low)
PP_OD	Push-pull/open-drain selection on interrupt pad. Default value: 0 (0: push-pull; 1: open-drain)

Table 40. Self-test mode selection

ST2	ST1	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Negative sign self-test
1	1	Not allowed

8.6 CTRL4_A (23h)

Control register 4 (r/w): interrupt 1 configuration

Table 41. CTRL4_A register

0(1)	INT1_S_TAP	INT1_WU	INT1_FF	INT1_TAP	INT1_6D	INT1_FTH	INT1_DRDY

1. This bit must be set to '0' for correct device operation.

Table 42. CTRL4_A register description

INT1_S_TAP	Single-tap recognition is routed on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_WU	Wakeup recognition is routed on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_FF	Free-fall recognition is routed on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_TAP	Double-tap recognition is routed on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_6D	6D recognition is routed on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_FTH	FIFO threshold interrupt is routed on INT1 pad. Default value: 0 (0: disabled; 1: enabled)
INT1_DRDY	Data-Ready is routed on INT1 pad. Default value: 0 (0: disabled; 1: enabled)

8.7 CTRL5_A (24h)

Control register 5 (r/w): interrupt 2 configuration

Table 43. CTRL5_A register

DRDY_ PULSED	INT2_ BOOT	INT2_ ON_INT1	0(1)	0(1)	0(1)	INT2_ FTH	INT2_ DRDY

1. This bit must be set to '0' for correct device operation.

Table 44. CTRL5_A register description

DRDY_ PULSED	Data-ready interrupt mode selection: latched mode / pulsed mode. Default value: 0 (0: latched mode; 1: pulsed mode for data-ready)
INT2 _BOOT	Boot state routed on INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2 _ON INT1	All signals routed on INT2 are also routed on INT1. Default value: 0 (0: disabled; 1: enabled)
INT2_FTH	FIFO threshold interrupt is routed on INT2 pad. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY	Data-Ready is routed on INT2 pad. Default value: 0 (0: disabled; 1: enabled)

8.8 FIFO_CTRL_A (25h)

FIFO control register 5 (r/w).

Table 45. FIFO_CTRL_A register

FMODE2	FMODE1	FMODE0	0(1)	MODULE_ TO_FIFO	0(1)	0(1)	IF_CS_PU _ DIS

1. This bit must be set to '0' for correct device operation.

Table 46. FIFO_CTRL_A register description

FMODE [2:0]	FIFO mode selection bits. Default: 000. For further details refer to *Table 47.*
MODULE_TO_ FIFO	When set to '1'-logic, module routine result is send to FIFO instead of X,Y,Z acceleration data
IF_CS_PU_DIS	When '1'-logic disconnects pull-up in if_cs pad. Default: 0

When the FIFO has been enabled, data acquired has been stored at the accelerometer ODR and the trigger signal of FIFO writing is the accelerometer internal data-ready.

FIFO data can be stored in default configuration where inertial data as been stored as X, Y, Z data or in module configuration:

Default configuration: 256-level inertial data (14-bit stored data for X, Y, Z)

User-selectable: 768 module data (14-bit each module)

Table 47. FIFO mode selection

FMODE2	FMODE1	FMODE0	Mode
0	0	0	Bypass mode: FIFO turned off
0	0	1	FIFO mode: Stops collecting data when FIFO is full.
0	1	0	Reserved
0	1	1	Continuous-to-FIFO: Stream mode until trigger is deasserted, then FIFO mode
1	0	0	Bypass-to-Continuous: Bypass mode until trigger is deasserted, then FIFO mode
1	0	1	Reserved
1	1	0	Continuous mode: data If the FIFO is full, the new sample overwrites the older sample.
1	1	1	Reserved

8.9 OUT_T_A (26h)

Temperature output register (r).

Table 48. OUT_T_A register

TEMP7	TEMP6	TEMP5	TEMP4	TEMP3	TEMP2	TEMP1	TEMP0

Table 49. OUT_T_A register description

Temp [7:0]	Temperature sensor output data. The value is expressed as two's complement sign. Sensitivity = 1 °C/LSB 0 LSB represents T=25 °C ambient.

8.10 STATUS_A (27h)

Status register (r)

Table 50. STATUS_A register

FIFO_THS	WU_IA	SLEEP_ STATE	DOUBLE_ TAP	SINGLE_ TAP	6D_IA	FF_IA	DRDY

Table 51. STATUS_A register description

FIFO_THS	FIFO threshold status flag. (0: FIFO filling is lower than threshold level; 1: FIFO filling is equal to or higher than the threshold level.)
WU_IA	Wakeup event detection status. (0: WU event not detected; 1: Wakeup event detected)
SLEEP_ STATE	Sleep event status. (0: Sleep event not detected; 1: Sleep event detected)
DOUBLE_ TAP	Double-tap event status (0: Double-tap event not detected; 1: Double-tap event detected)
SINGLE_ TAP	Single-tap event status (0: Single-tap event not detected; 1: Single-tap event detected)
6D_IA	Source of change in position portrait/landscape/face-up/face-down. (0: no event detected; 1: a change in position detected)
FF_IA	Free-fall event detection status. (0: free-fall event not detected; 1: free-fall event detected)
DRDY	Data-ready status. (0: not ready; 1: X-, Y- and Z-axis new data available)

8.11 OUT_X_L_A (28h)

X-axis LSB output register (r)

Table 52. OUT_X_L_A register default values

X_L7	X_L6	X_L5(2)	X_L4(2)	X_L3(1)(2)	X_L2(1)(2)	0	0

1. If 12-bit mode is enabled, this bit is set to 0.
2. If 10-bit mode is enabled, this bit is set to 0.

The 8 least significant bits of linear acceleration sensor X-axis output. Together with the *OUT_X_H_A (29h)* register it forms the output value expressed as a 16-bit word in 2's complement.

8.12 OUT_X_H_A (29h)

X-axis MSB output register (r)

Table 53. OUT_X_H_A register default values

X_H7	X_H6	X_H5	X_H4	X_H3	X_H2	X_H1	X_H0

The 8 most significant bits of linear acceleration sensor X-axis output. Together with the *OUT_X_L_A (28h)* register it forms the output value expressed as a 16-bit word in 2's complement.

8.13 OUT_Y_L_A (2Ah)

Y-axis LSB output register (r)

Table 54. OUT_Y_L_A register default values

Y_L7	Y_L6	Y_L5(2)	Y_L4(2)	Y_L3(1)(2)	Y_L2(1)(2)	0	0

1. If 12-bit mode is enabled, this bit is set to 0.
2. If 10-bit mode is enabled, this bit is set to 0.

The 8 least significant bits of linear acceleration sensor Y-axis output. Together with the *OUT_Y_H_A (2Bh)* register it forms the output value expressed as a 16-bit word in 2's complement.

8.14 OUT_Y_H_A (2Bh)

Y-axis MSB output register (r)

Table 55. OUT_Y_H_A register default values

Y_H7	Y_H6	Y_H5	Y_H4	Y_H3	Y_H2	Y_H1	Y_H0

The 8 most significant bits of linear acceleration sensor Y-axis output. Together with the *OUT_Y_L_A (2Ah)* register it forms the output value expressed as a 16-bit word in 2's complement.

8.15 OUT_Z_L_A (2Ch)

Z-axis LSB output register (r)

Table 56. OUT_Z_L_A register default values

Z_L7	Z_L6	Z_L5(2)	Z_L4(2)	Z_L3(1)(2)	Z_L2(1)(2)	0	0

1. If 12-bit mode is enabled, this bit is set to 0.
2. If 10-bit mode is enabled, this bit is set to 0.

The 8 least significant bits of linear acceleration sensor Z-axis output. Together with the *OUT_Z_H_A (2Dh)* register it forms the output value expressed as a 16-bit word in 2's complement.

8.16 OUT_Z_H_A (2Dh)

Z-axis MSB output register (r)

Table 57. OUT_Z_H_A register default values

Z_H7	Z_H6	Z_H5	Z_H4	Z_H3	Z_H2	Z_H1	Z_H0

The 8 most significant bits of linear acceleration sensor Z-axis output. Together with the *OUT_Z_L_A (2Ch)* register it forms the output value expressed as a 16-bit word in 2's complement.

8.17 FIFO_THS_A (2Eh)

FIFO threshold level setting (r/w).

Table 58. FIFO_THS_A register

FTH7	FTH6	FTH5	FTH4	FTH3	FTH2	FTH1	FTH0

8.18 FIFO_SRC_A (2Fh)

FIFO_SRC register (r)

Table 59. FIFO_SRC_A register

FTH	FIFO OVR	DIFF8	-	-	-	-	-

Table 60. FIFO_SRC register description

FTH	FIFO threshold status. (0: FIFO filling is lower than FTH level; 1: FIFO filling is equal to or higher than threshold level)
OVR	FIFO overrun status. (0: FIFO is not completely filled; 1: FIFO is completely filled and at least one sample has been overwritten)
DIFF8	Concatenated with *FIFO_SAMPLES_A (30h)* register, it represents the number of unread samples stored in FIFO. (000000000 = FIFO empty; 100000000 = FIFO full, 256 unread samples).

8.19 FIFO_SAMPLES_A (30h)

FIFO_SAMPLES control register (r)

Table 61. FIFO_SAMPLES_A register

DIFF7	DIFF6	DIFF5	DIFF4	DIFF3	DIFF2	DIFF1	DIFF0

Table 62. FIFO_SAMPLES_A register description

DIFF [7:0]	Concatenated with DIFF8 bit in *FIFO_SRC_A (2Fh)* register, it represents the number of unread samples stored in FIFO. (000000000 = FIFO empty; 100000000 = FIFO full, 256 unread samples).

8.20 TAP_6D_THS_A (31h)

4D configuration enable and TAP threshold configuration (r/w)

Table 63. TAP_6D_THS_A register

4D_EN	6D_THS1	6D_THS0	TAP_ THS4	TAP_ THS3	TAP_ THS2	TAP_ THS1	TAP_ THS0

Table 64. TAP_6D_THS_A register description

4D_EN	4D detection portrait/landscape position enable. (0: no position detected; 1: portrait/landscape detection and face-up/face-down position enabled).
6D_THS [1:0]	Thresholds for 4D/6D function @ FS=2 *g* (refer to *Table 65*)
TAP_THS [4:0]	Threshold for TAP recognition @ FS=2 *g*

Table 65. 4D/6D threshold setting FS @ 2 *g*

6D_THS1	6D_THS0	Threshold decoding (degrees)
0	0	6 (80 degrees)
0	1	11 (70 degrees)
1	0	16 (60 degrees)
1	1	21 (50 degrees)

8.21 INT_DUR_A (32h)

Interrupt duration register (r/w)

Table 66. INT_DUR_A register

LAT3	LAT2	LAT1	LAT0	QUIET1	QUIET0	SHOCK1	SHOCK0

Table 67. INT_DUR_A register description

LAT [3:1]	Duration of maximum time gap for double-tap recognition. When double-tap recognition is enabled, this register expresses the maximum time between two successive detected taps to determine a double-tap event. 1 LSB = 32 TODR.
QUIET [1:0]	Expected quiet time after a tap detection: this register represents the time after the first detected tap in which there must not be any over-threshold event. 1 LSB = 4 TODR.
SHOCK [4:0]	Maximum duration of over-threshold event: this register represents the maximum time of an over-threshold signal detection to be recognized as a tap event. 1 LSB = 8 TODR

8.22 WAKE_UP_THS_A (33h)

Wakeup threshold register (r/w)

Table 68. WAKE_UP_THS_A register

SINGLE_ DOUBLE_ TAP	SLEEP_ ON	WU_ THS_ 5	WU_ THS_4	WU_ THS_3	WU_ THS 2	WU_ THS 1	WU_ THS 0

Table 69. WAKE_UP_THS_A register description

SINGLE_ DOUBLE_ TAP	Double/single-tap event detection: (0: double-tap event detection; 1: single-tap event detection)
SLEEP_ON	Sleep (inactivity) enable (0: sleep disabled; 1: sleep enabled)
WU_THS [5:0]	Wakeup threshold

8.23 WAKE_UP_DUR_A (34h)

Wakeup and sleep duration configuration register (r/w)

Table 70. WAKE_UP_DUR_A register

FF_DUR5	WU_DUR1	WU_DUR0	INT1_ FSS7	SLEEP_ DUR3	SLEEP_ DUR2	SLEEP_ DUR1	SLEEP_ DUR0

Table 71. WAKE_UP_DUR_A register description

FF DUR5	Free-fall duration. In conjunction with FF_DUR [4:0] bit in *FREE_FALL_A (35h)* register. 1 LSB = 1 TODR
WU_DUR [1:0]	Wakeup duration. 1 LSB = 1 TODR
INT1_FSS7	FF interrupt is routed on INT1 pad (0: disabled; 1: enabled)
SLEEP_DUR[5:0]	Duration to go in sleep mode. 1 LSB = 512 TODR

8.24 FREE_FALL_A (35h)

Free-fall duration and threshold configuration register (r/w)

Table 72. FREE_FALL_A register

FF_DUR4	FF_DUR3	FF_DUR2	FF_DUR1	FF_DUR0	FF_THS2	FF_THS1	FF_THS0

Table 73. FREE_FALL_A register description

FF_DUR [4:0]	Free-fall duration. In conjunction with FF_DUR5 bit in *WAKE_UP_DUR_A (34h)* register. 1 LSB = 1 TODR.
FF_THS [2:0]	Free-fall threshold @ FS = 2 *g* (refer to *Table 74*)

Table 74. FREE_FALL_A threshold decoding @ 2 *g* FS

FF_THS1	FF_THS1	FF_THS0	Threshold decoding (degrees)
0	0	0	5
0	0	1	7
0	1	0	8
0	1	1	10
1	0	0	11
1	0	1	13
1	1	0	15
1	1	1	16

8.25 STATUS_DUP_A (36h)

Event detection status register (r)

Table 75. STATUS_DUP_A register

OVR	WU_IA	SLEEP_ STATE	DOUBLE_ TAP	SINGLE_ TAP	6D_IA	FF_IA	DRDY

Table 76. STATUS_DUP_A register description

OVR	FIFO overrun status flag. (0: FIFO filling is not completely filled; 1: FIFO is completely filled and at least one sample has been overwritten)
WU_IA	Wakeup event detection status. (0: WU event not detected; 1: Wake up event detected)
SLEEP_ STATE	Sleep event status. (0: Sleep event not detected; 1: Sleep event detected)
DOUBLE_ TAP	Double-tap event status: (0: Double-tap event not detected; 1: Double-tap event detected)
SINGLE_ TAP	Single-tap event status: (0: Single-tap event not detected; 1: Single-tap event detected)
6D_IA	Source of change in position portrait/landscape/face-up/face-down. (0: no event detected; 1: a change in position is detected)
FF_IA	Free-fall event detection status. (0: free-fall event not detected; 1: free-fall event detected)
DRDY	Data-ready status. (0: not ready; 1: X-, Y- and Z-axis new data available)

8.26 WAKE_UP_SRC_A (37h)

Wakeup source register (r)

Table 77. WAKE_UP_SRC_A register

-	-	FF_IA	SLEEP STATE IA	WU_IA	X_WU	Y_WU	Z_WU

Table 78. WAKE_UP_SRC_A register description

FF_IA	Free-fall event detection status. (0: FF event not detected; 1: FF event detected)
SLEEP STATE IA	Sleep event status. (0: Sleep event not detected; 1: Sleep event detected)
WU_IA	Wakeup event detection status. (0: Wakeup event not detected; 1: Wakeup event is detected)
X_WU	Wakeup event detection status on X-axis. (0: Wakeup event on X not detected; 1: Wakeup event on X-axis is detected)
Y_WU	Wakeup event detection status on Y-axis. (0: Wakeup event on Y not detected; 1: Wake up event on Y-axis is detected)
Z_WU	Wakeup event detection status on Z-axis. (0: Wakeup event on Z not detected; 1: Wake up event on Z-axis is detected)

8.27 TAP_SRC_A (38h)

TAP source register (r)

Table 79. TAP_SRC_A register

-	TAP_IA	SINGLE TAP	DOUBLE TAP	TAP SIGN	X_TAP	Y_TAP	Z_TAP

Table 80. TAP_SRC_A register description

TAP_IA	TAP event status. (0: Tap event not detected; 1: Tap event detected)
SINGLE TAP	Single-tap event status. (0: Single-tap event not detected; 1: Single-tap event detected)
DOUBLE TAP	Double-tap event status. (0: Double-tap event not detected; 1: Double-tap event detected)
TAP_SIGN	Sign of acceleration detected by tap event. (0: positive sign of acceleration detected; 1: negative sign of acceleration detected).
X_TAP	Tap event detection status on X-axis. (0: Tap event on X not detected; 1: Tap event on X-axis is detected)
Y_TAP	Tap event detection status on Y-axis. (0: Tap event on Y not detected; 1: TAP event on Y-axis is detected)
Z_TAP	Tap event detection status on Z-axis. (0: Tap event on Z not detected; 1: Tap event on Z-axis is detected)

8.28 6D_SRC_A (39h)

6D source register (r)

Table 81. 6D_SRC_A register

-	6D_IA	ZH	ZL	YH	YL	XH	XL

Table 82. 6D_SRC_A register description

6D_IA	Source of change in position portrait/landscape/face-up/face-down. (0: no event detected; 1: a change in position is detected)
ZH	ZH overthreshold (0: ZH does not exceed the threshold; 1: ZH is over the threshold)
ZL	ZL overthreshold (0: ZL does not exceed the threshold; 1: ZL is over the threshold)
YH	YH overthreshold (0: YH does not exceed the threshold; 1: YH is over the threshold)
YL	YL overthreshold (0: YL does not exceed the threshold; 1: YL is over the threshold)
XH	XH overthreshold: (0: XH does not exceed the threshold; 1: XH is over the threshold)
XL	XL overthreshold (0: XL does not exceed the threshold; 1: XL is over the threshold)

8.29 FUNC_SRC_A (3Eh)

Functional source register (r)

Table 83. FUNC_SRC_A register

-	-	-	-	-	0	MODULE_ READY	-

Table 84. FUNC_SRC_A register description

MODULE_READY	Module status. (0: new module data not available, 1: new module data available)

8.30 FUNC_CTRL_A (3Fh)

Functional control register (r/w)

Table 85. FUNC_CTRL_A register

0(1)	0(1)	MODULE_ ON	0(1)	0(1)	0(1)	0(1)	0(1)

1. This bit must be set to '0' for the correct operation of the device.

Table 86. FUNC_CTRL_A register description

MODULE_ON	Module processing enable. Default value: 0 (0: disabled; 1: module)

8.31 OFFSET_X_REG_L_M (45h) and OFFSET_X_REG_H_M (46h)

These registers comprise a 16-bit register and represent X hard-iron offset in order to compensate environmental effects (data in two's complement). These values act on the magnetic output data value in order to delete the environmental offset.

8.32 OFFSET_Y_REG_L_M (47h) and OFFSET_Y_REG_H_M (48h)

These registers comprise a 16-bit register and represent Y hard-iron offset in order to compensate environmental effects (data in two's complement). These values act on the magnetic output data value in order to delete the environmental offset.

8.33 OFFSET_Z_REG_L_M (49h) and OFFSET_Z_REG_H_M (4Ah)

These registers comprise a 16-bit register and represent Z hard-iron offset in order to compensate environmental effects (data in two's complement). These values act on the magnetic output data value in order to delete the environmental offset.

8.34 WHO_AM_I_M (4Fh)

The identification register is used to identify the device (read-only register).

0	1	0	0	0	0	0	0

8.35 CFG_REG_A_M (60h)

The configuration register is used to configure the output data rate and the measurement configuration.

Table 87. CFG_REG_A_M register

COMP_ TEMP_EN	REBOOT	SOFT_RST	LP	ODR1	ODR0	MD1	MD0

Table 88. CFG_REG_A_M register description

COMP_ TEMP_EN(1)	Enable the magnetometer temperature compensation. Default value: 0 (0: temperature compensation disabled; 1: temperature compensation enabled)
REBOOT	Reboot magnetometer memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
SOFT_RST	When this bit is set, the configuration registers and user registers are reset. Flash registers keep their values.
LP	Low-power mode enable. Default: 0 0: high-resolution mode 1: low-power mode enabled
ODR[1:0]	Output data rate configuration (see *Table 89: Output data rate configuration*)
MD[1:0]	Mode select bit. These bits select the mode of operation of the device (see *Table 90: System mode*)

1. For proper operation, this bit must be set to '1'.

Table 89. Output data rate configuration

ODR1	ODR0	ODR (Hz)
0	0	10 (default)
0	1	20
1	0	50
1	1	100

Table 90. System mode

MD1	MD0	Mode
0	0	Continuous mode. In continuous mode the device continuously performs measurements and places the result in the data register. The data-ready signal is generated when a new data set is ready to be read. This signal can be available on the external pin by setting the INT_MAG bit in *CFG_REG_C_M (62h)*.
0	1	Single mode. When single mode is selected, the device performs a single measurement, sets DRDY high and returns to idle mode. Mode register return to idle mode bit values.
1	0	Idle mode. Device is placed in idle mode. I^2C and SPI active.
1	1	Idle mode. Device is placed in idle mode. I^2C and SPI active.

8.36 CFG_REG_B_M (61h)

Table 91. CFG_REG_B_M register

0	0	0	OFF_ CANC_ ONE_ SHOT	INT_on_ DataOFF	Set_FREQ	OFF_CANC	LPF

Table 92. CFG_REG_B_M register description

OFF_CANC_ ONE_SHOT	Enables offset cancellation in single measurement mode. The OFF_CANC bit must be set to 1 when enabling offset cancellation in single measurement mode. 0: offset cancellation in single measurement mode disabled; 1: offset cancellation in single measurement mode enabled.
INT_on_ DataOFF	If '1', the interrupt block recognition checks data after the hard-iron correction to discover the interrupt.
Set_FREQ	Selects the frequency of the set pulse. 0: set pulse is released every 63 ODR; 1: set pulse is released only at power-on after PD condition.
OFF_CANC	Enables offset cancellation.
LPF	Low-pass filter enable (see *Table 93*) 0: digital filter disabled; 1: digital filter enabled

Table 93. Digital low-pass filter

CFG_REG_B[LPF]	BW [Hz]
0 (disable)	ODR/2
1 (enable)	ODR/4

8.37 CFG_REG_C_M (62h)

Table 94. CFG_REG_C_M register

0	INT_MAG_PIN	I2C_DIS	BDU	BLE	0(1)	Self_test	INT_MAG

1. This bit must be set to '0' for the correct operation of the device.

Table 95. CFG_REG_C_M register description

INT_MAG_PIN	If '1', the INTERRUPT signal (INT bit inside *INT_SOURCE_REG_M (64h)* is driven on INT_MAG_PIN.
I2C_DIS	If '1', the I^2C interface is inhibited. Only the SPI interface can be used.
BDU	If enabled, reading of incorrect data is avoided when the user reads asynchronously. In fact if the read request arrives during an update of the output data, a latch is possible, reading incoherent high and low parts of the same register. Only one part is updated and the other one remains old.
BLE	If '1', an inversion of the low and high parts of the data occurs.
Self_test	If '1', the self-test is enabled.
INT_MAG	If '1', the DRDY pin is configured as a digital output.

8.38 INT_CTRL_REG_M (63h)

The interrupt control register is used to enable and to configure the interrupt recognition.

Table 96. INT_CRTL_REG_M register

XIEN	YIEN	ZIEN	0(1)	0(1)	IEA	IEL	IEN

1. This bit must be set to '0' for the correct operation of the device.

Table 97. INT_CTRL_REG_M register description

XIEN	Enables the interrupt recognition for the X-axis. Default: 0 1: enabled; 0: disabled.
YIEN	Enables the interrupt recognition for the Y-axis. Default: 0 1: enabled; 0: disabled.
ZIEN	Enables the interrupt recognition for the Z-axis. Default: 0 1: enabled; 0: disabled.
IEA	Controls the polarity of the INT bit (*INT_SOURCE_REG_M (64h)*) when an interrupt occurs. Default: 0 If IEA = 0, then INT = 0 signals an interrupt If IEA = 1, then INT = 1 signals an interrupt
IEL	Controls whether the INT bit (*INT_SOURCE_REG_M (64h)*) is latched or pulsed. Default: 0 If IEL = 0, then INT is pulsed. If IEL = 1, then INT is latched. Once latched, INT remains in the same state until *INT_SOURCE_REG_M (64h)* is read.
IEN	Interrupt enable. When set, enables the interrupt generation. The INT bit is in *INT_SOURCE_REG_M (64h)*. Default: 0

8.39 INT_SOURCE_REG_M (64h)

When interrupt latched is selected, reading this register resets all the bits in this register.

Table 98. INT_SOURCE_REG_M register

P_TH_S_X	P_TH_S_Y	P_TH_S_Z	N_TH_S_X	N_TH_S_Y	N_TH_S_Z	MROI	INT

Table 99. INT_SOURCE_REG_M register description

P_TH_S_X	X-axis value exceeds the threshold positive side
P_TH_S_Y	Y-axis value exceeds the threshold positive side
P_TH_S_Z	Z-axis value exceeds the threshold positive side
N_TH_S_X	X-axis value exceeds the threshold negative side
N_TH_S_Y	Y-axis value exceeds the threshold negative side
N_TH_S_Z	Z-axis value exceeds the threshold negative side
MROI	MROI flag generation is alway enabled.This flag is reset by reading *INT_SOURCE_REG_M (64h)*.
INT	This bit signals when the interrupt event occurs.

8.40 INT_THS_L_REG_M (65h)

This register contains the least significant bits of the threshold value chosen for the interrupt.

Table 100. INT_THS_L_REG_M register

TH7	THS6	TH5	TH4	TH3	TH2	TH1	TH0

Table 101. INT_THS_L_REG_M register description

TH[7:0]	Threshold value for the interrupt.

8.41 INT_THS_H_REG_M (66h)

This register contains the most significant bits of the threshold value chosen for the interrupt.

Table 102. INT_THS_H_REG_M register

TH15	THS14	TH13	TH12	TH11	TH10	TH9	TH8

Table 103. INT_THS_H_REG_M register description

TH[15:8]	Threshold value for the interrupt.

These registers set the threshold value for the output to generate the interrupt (INT bit in *INT_SOURCE_REG_M (64h)*). This threshold is common to all three (axes) output values and is unsigned unipolar. The threshold value is correlated to the current gain and it is unsigned because the threshold is considered as an absolute value but crossing the threshold is detected for both positive and negative sides.

8.42 STATUS_REG_M (67h)

The status register is an 8-bit read-only register. This register is used to indicate device status. SR0 through SR7 indicate bit locations, with SR denoting the bits that are in the status register. SR7 denotes the first bit of the data stream.

Table 104. STATUS_REG_M register

Zyxor	zor	yor	xor	Zyxda	zda	yda	xda

Table 105. STATUS_REG_M register description

Zyxor	X-, Y- and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous set).
zor	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data).
yor	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data).
xor	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data).
Zyxda	X-, Y- and Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available).
zda	Z-axis new data available. Default value: 0 (0: a new data for the Z-axis is not yet available; 1: a new data for the Z-axis is available)
yda	Y-axis new data available. Default value: 0 (0: a new data for the Y-axis is not yet available; 1: a new data for the Y-axis is available)
xda	X-axis new data available. Default value: 0 (0: a new data for the X-axis is not yet available; 1: a new data for the X-axis is available)

8.43 OUTX_L_REG_M, OUTX_H_REG_M (68h - 69h)

The data output X registers are two 8-bit registers, data output ch1 MSB register (69h) and output X LSB register (68h).

The output data represents the raw magnetic data only if OFFSET_X_REG is equal to zero, otherwise hard-iron calibration is included.

Table 106. OUTX_L_REG_M register

0	0	0	0	0	0	0	0

Table 107. OUTX_H_REG_M register

0	0	0	0	0	0	0	0

The value of the magnetic field is expressed in two’s complement. This register contains the X component of the magnetic data.

8.44 OUTY_L_REG_M, OUTY_H_REG_M (6Ah - 6Bh)

The data output Y registers are two 8-bit registers, data output ch1 MSB register (6Bh) and output Y LSB register (6Ah).

The output data represents the raw magnetic data only if OFFSET_Y_REG is equal to zero, otherwise hard-iron calibration is included.

Table 108. OUTY_L_REG_M register

0	0	0	0	0	0	0	0

Table 109. OUTY_H_REG_M register

0	0	0	0	0	0	0	0

The value of the magnetic field is expressed in two's complement. This register contains the Y component of the magnetic data.

8.45 OUTZ_L_REG_M, OUTZ_H_REG_M (6Ch - 6Dh)

The data output Z registers are two 8-bit registers, data output ch1 MSB register (6Bh) and output Z LSB register (6Ah).

The output data represents the raw magnetic data only if OFFSET_Z_REG is equal to zero, otherwise hard-iron calibration is included.

Table 110. OUTZ_L_REG_M register

0	0	0	0	0	0	0	0

Table 111. OUTZ_H_REG_M register

0	0	0	0	0	0	0	0

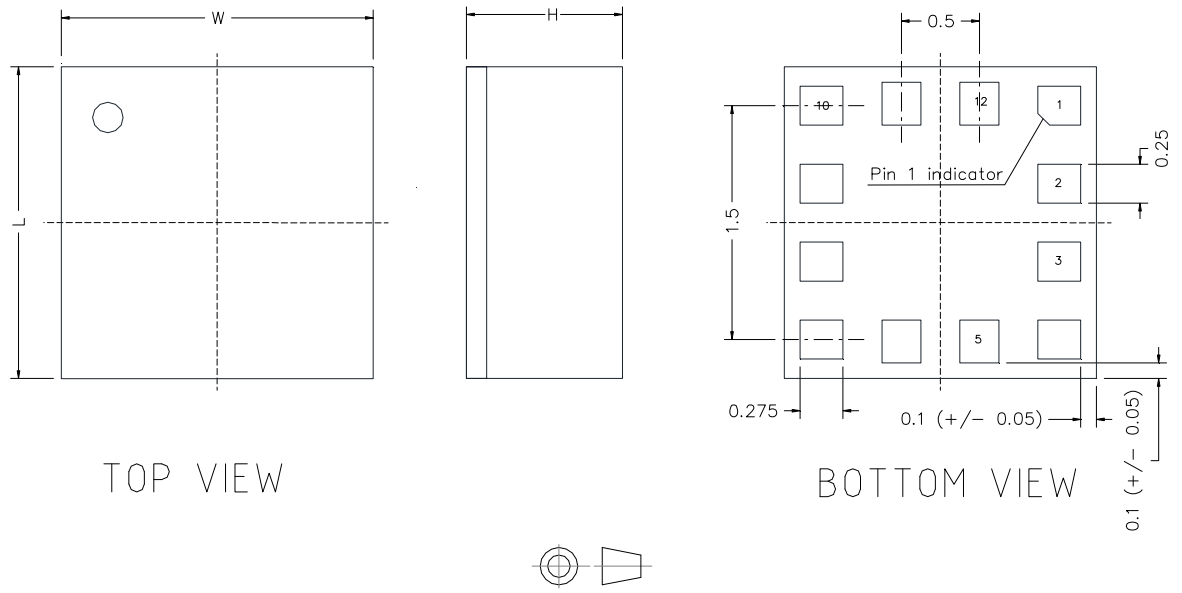
The value of the magnetic field is expressed in two's complement. This register contains the Z component of the magnetic data.

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

9.1 LGA-12 package information

Figure 23. LGA-12 2x2x1 mm package outline and mechanical data



Dimensions are in millimeter unless otherwise specified
General Tolerance is +/-0.1mm unless otherwise specified

OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2.00	±0.1
Width [W]	2.00	±0.1
Height [H]	1.0	MAX

8487206_5

9.2 LGA-12 packing information

Figure 24. Carrier tape information for LGA-12 package

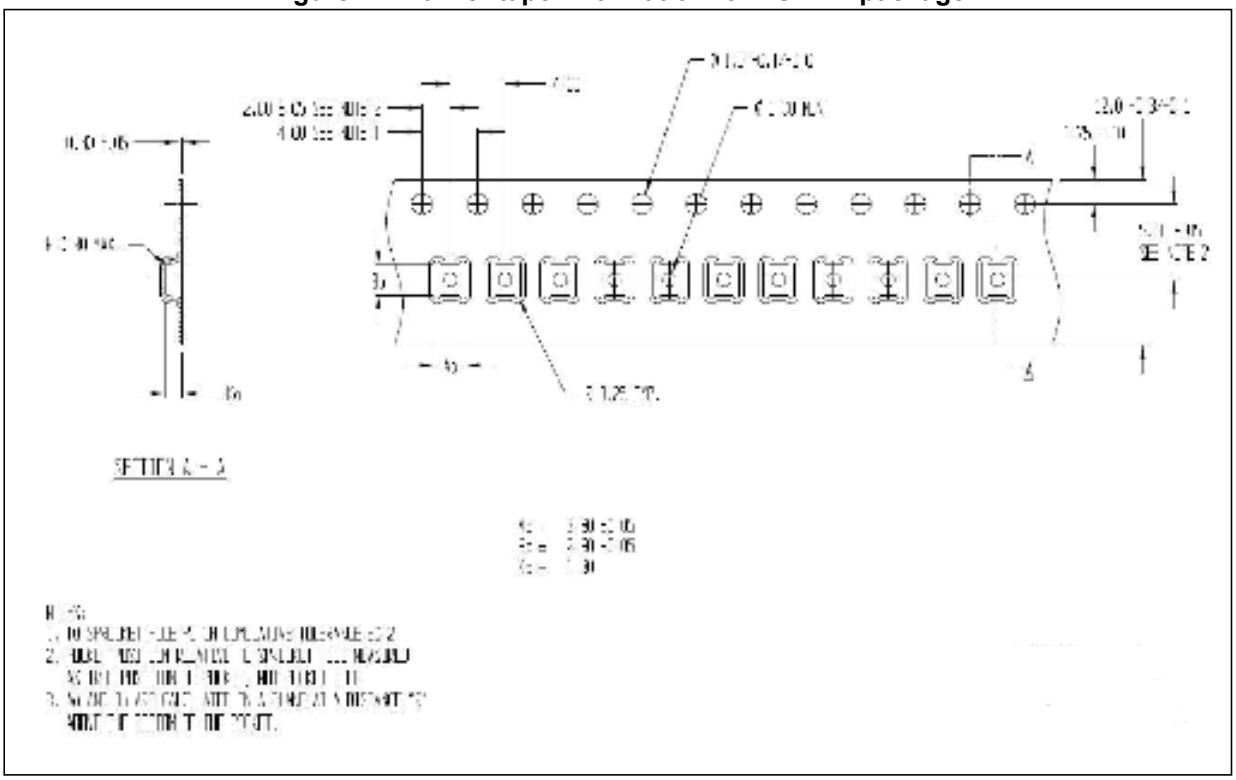


Figure 25. LGA-12 package orientation in carrier tape

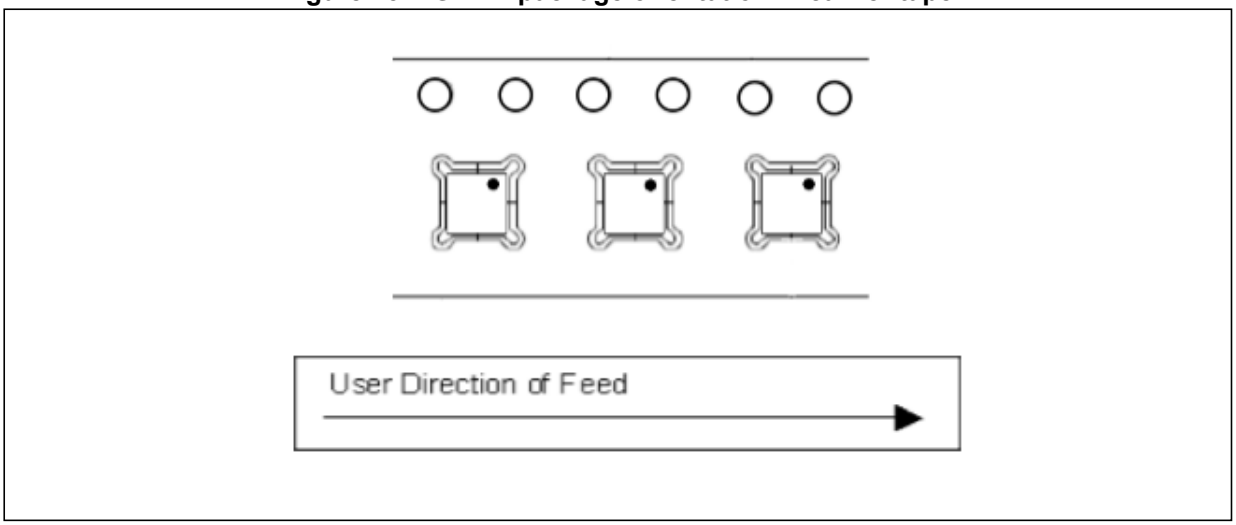


Figure 26. Reel information for carrier tape of LGA-12 package

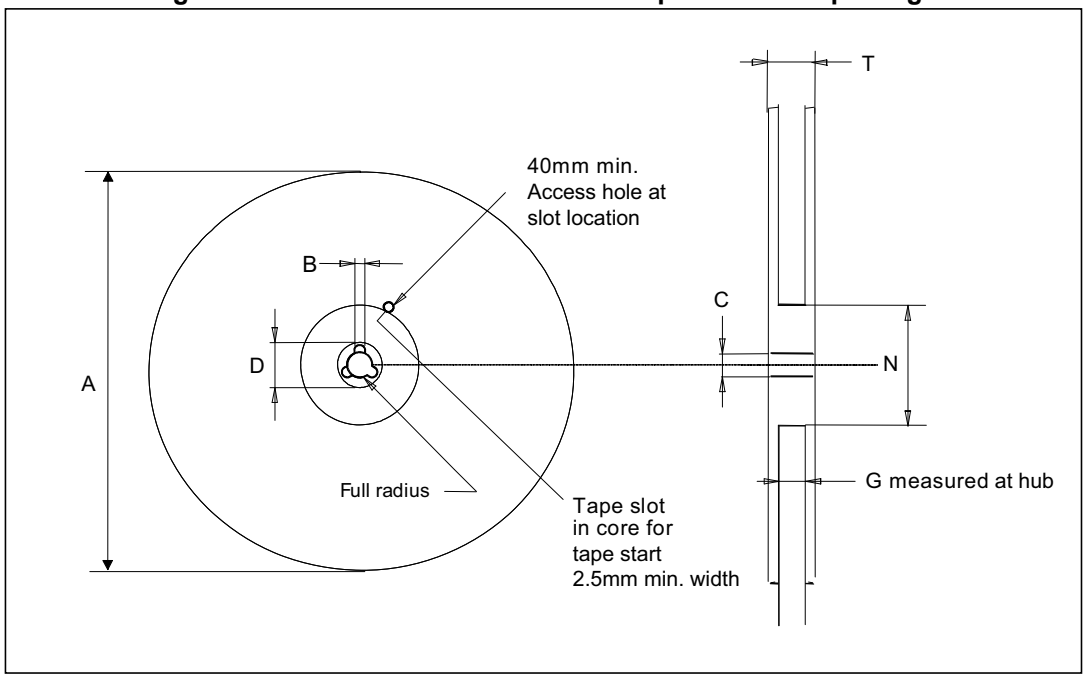


Table 112. Reel dimensions for carrier tape of LGA-12 package

Reel dimensions (mm)	
A (max)	330
B (min)	1.5
C	13 ±0.25
D (min)	20.2
N (min)	60
G	12.4 +2/-0
T (max)	18.4

10 Revision history

Table 113. Document revision history

Date	Revision	Changes
16-Oct-2017	1	Initial release
31-Oct-2017	2	Document status promoted to “Datasheet - production data”

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