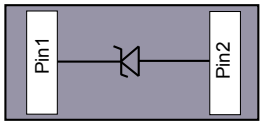
ESDA8P30-1T2

Datasheet

Small transient voltage suppressor



SOD882T package



Pin configuration

Features

- Low clamping voltage
- Peak pulse power:
  - 300 W (8/20 µs)
- Stand-off voltage 6.3 V
- Unidirectional diode
- Low leakage current:
  - 0.3 µA at 25 °C
- Complies with the following standards: IEC 61000-4-2 level 4
  - ± 30 kV (air discharge)
  - ± 30 kV (contact discharge)

Application

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phones, tablets, portable multimedia
- USB V_{bus} protection
- Power supply protection
- Battery protection

Product status link
ESDA8P30-1T2

Description

The ESDA8P30-1T2 is a unidirectional single line TVS diode designed to protect the power line against EOS and ESD transients.

The device is ideal for applications where high power TVS and board space saving are required.

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{pp}	Peak pulse voltage	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge	>30 >30	kV
P_{pp}	Peak pulse power (8/20 µs)		300	W
I_{pp}	Peak pulse current (8/20 µs)		30	A
T_{op}	Operating junction temperature range		-55 to 150	°C
T_{stg}	Storage junction temperature range		-55 to 150	°C

Figure 1. Electrical characteristics (definitions)

Symbol		Parameter
V_{BR}	=	Breakdown voltage
V_{CL}	=	Clamping voltage
I_{RM}	=	Leakage current @V_{RM}
V_{RM}	=	Stand-off voltage
I_{PP}	=	Peak pulse current
R_D	=	Dynamic resistance
I_R	=	Breakdown current

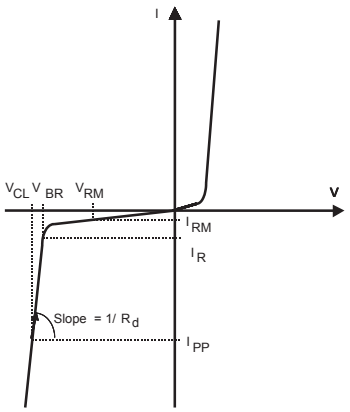


Table 2. Electrical characteristics (values) (T_{amb} = 25° C)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6.9	7.3	7.8	V
I_{RM}	V_{RM} = 6.3 V			300	nA
V_{CL}	I_{PP} = 20 A 8/20µs			11	V
	I_{PP} = 30 A 8/20µs			12	
R_D	8/20µs		0.12		Ω
C_{LINE}	V_{LINE} = 0 V, F = 1 MHz, V_{OSC} = 30 mV		170		pF

1.1 Characteristics (curves)

Figure 2. Peak pulse power dissipation versus initial junction temperature (typical value)

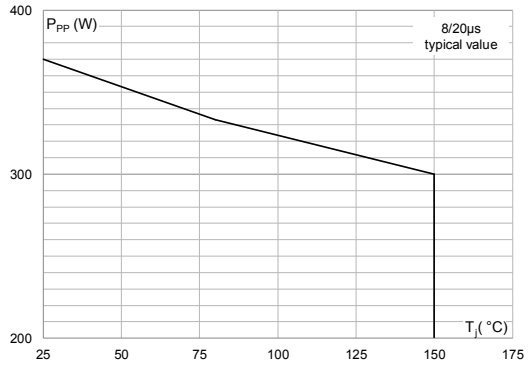


Figure 3. Peak pulse power versus exponential pulse duration (maximum values)

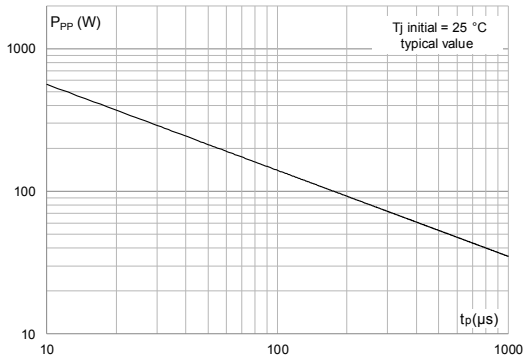


Figure 4. Peak power dissipation versus initial temperature (typical value)

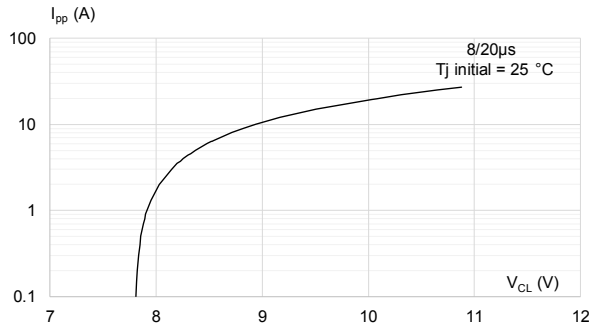


Figure 5. Leakage current versus junction temperature (typical value)

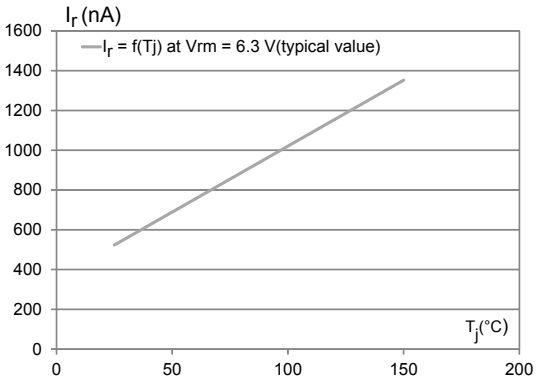


Figure 6. ESD response to IEC 61000-4-2 (+8kV contact discharge)

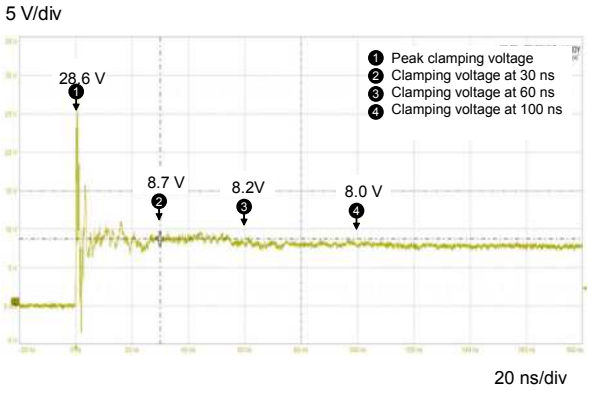
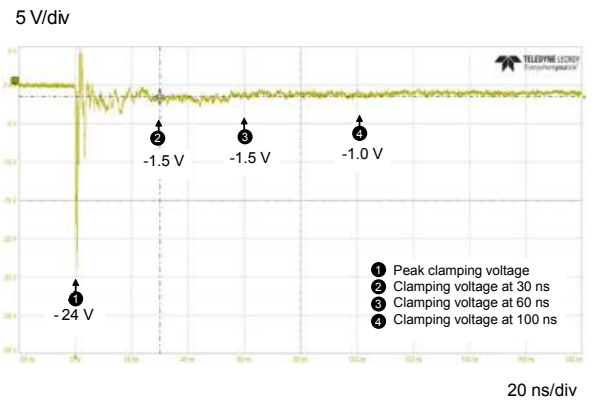


Figure 7. ESD response to IEC 61000-4-2 (-8kV contact discharge)



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 SOD882T package information

Figure 8. SOD882T package outline

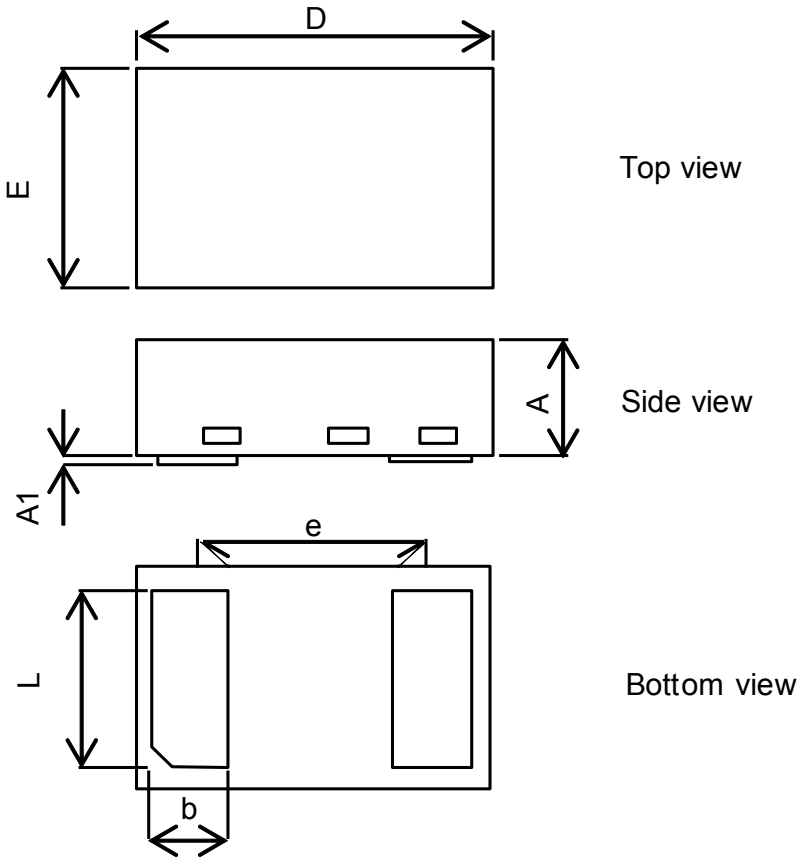


Table 3. **SOD882T package mechanical data**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.30		0.40
A1	0.00	0.02	0.05
L	0.45	0.50	0.55
D		1.00	
E		0.60	
e		0.65	
b	0.20	0.25	0.30

Figure 9. **SOD882T recommended footprint**

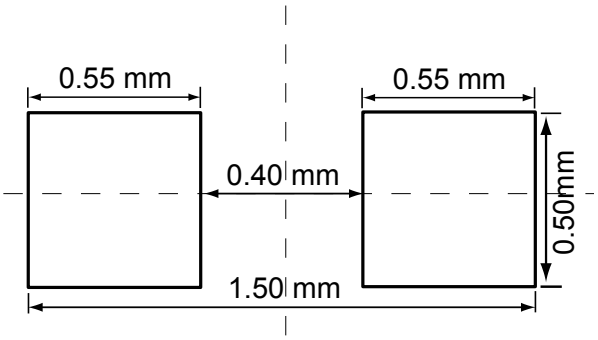
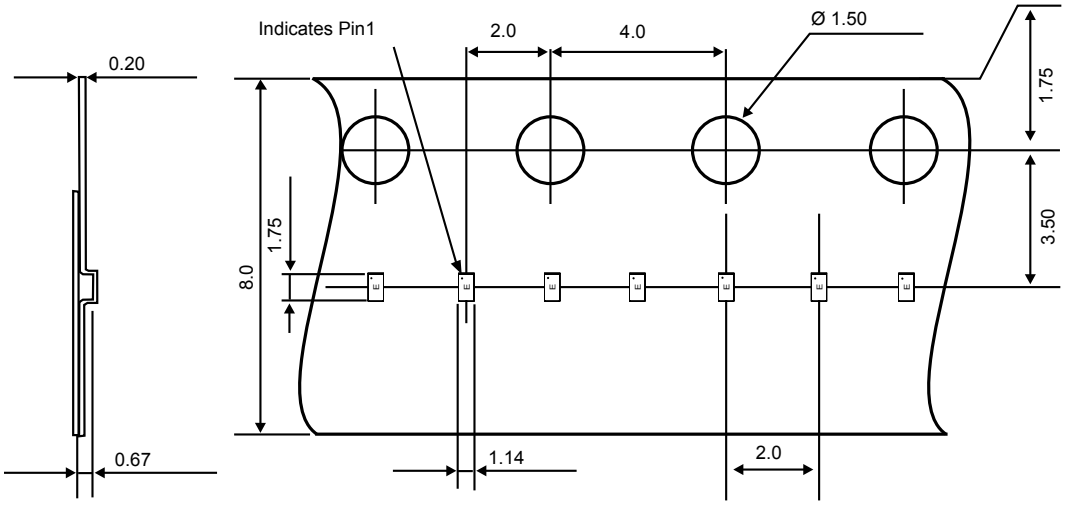


Figure 10. **Marking**



Figure 11. Tape and reel specification

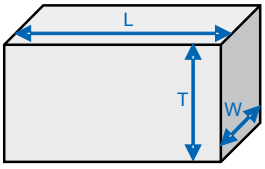


3 Recommendation on PCB assembly

3.1 Stencil opening design

1. General recommendation on stencil opening design
   a. Stencil opening dimensions: L (Length), W (Width), T (Thickness).

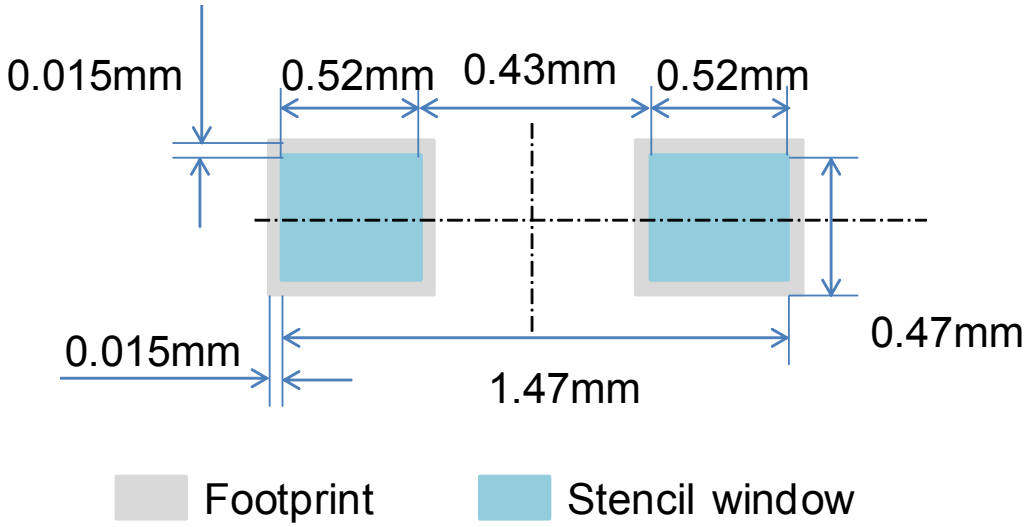
Figure 12. Stencil opening recommendation



   b. General design rule
      - Stencil thickness (T) = 75 ~ 125 µm
      - $\frac{W}{T} \geq 1.5$
      - $\frac{L \times W}{2T(L+W)} \geq 0.66$

1. Reference design
   a. Stencil opening thickness: 100 µm
   b. Stencil opening for leads: Opening to footprint ratio is 90%

Figure 13. Recommended stencil window position in mm



3.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-45 µm.

3.3 Placement

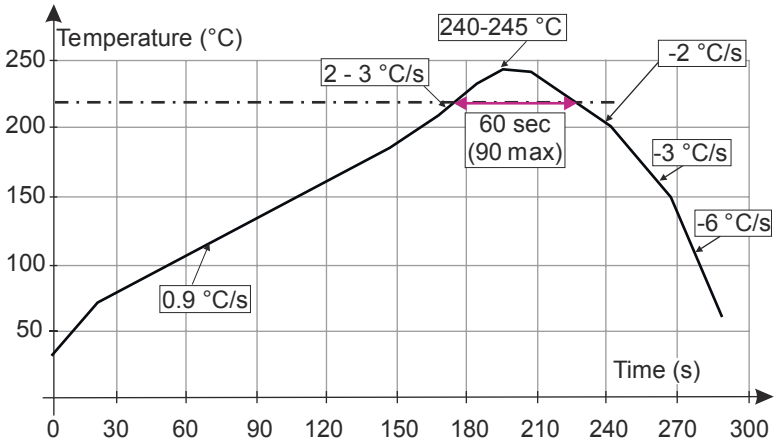
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.5 Reflow profile

Figure 14. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

4 Ordering information

Figure 15. Ordering information scheme

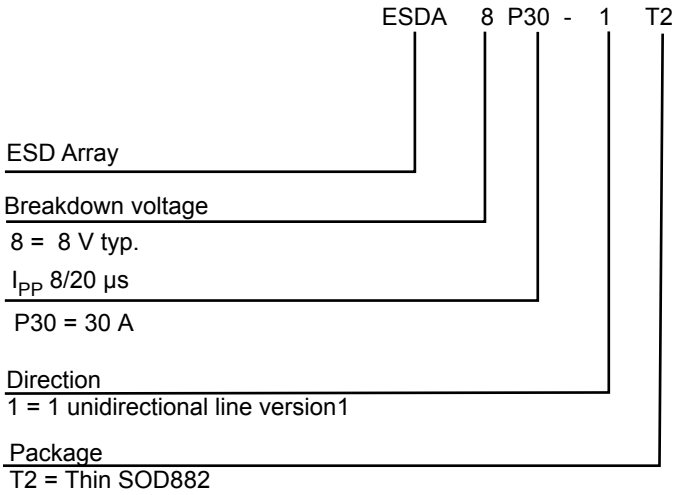


Table 4. Ordering information

Order code	Marking	Weight	Base qty.	Delivery mode
ESDA8P30-1T2	E	0.76 mg	12000	Tape and reel

1. *The marking can be rotated by multiples of 90° to differentiate assembly location.*

Revision history

Table 5. **Document revision history**

Date	Revision	Changes
03-Apr-2018	1	First issue.
24-Aug-2018	2	Updated Table 2.
18-Oct-2018	8	Updated Figure 10. Marking.

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