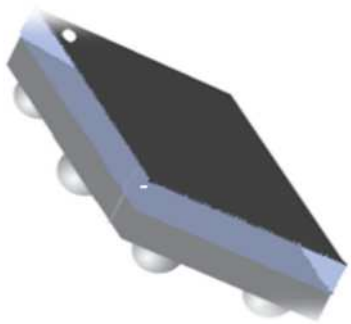
# BALFLB-WL-09D3

Datasheet

## 50 Ω nominal input / conjugate match balun to QFN-2L STM32WL in high power mode, 470-510 MHz with integrated harmonic filter



Chip scale package on glass 8 bumps

| Product status link |
| --- |
| BALFLB-WL-09D3 |

## Features

- QFN STM32WL sub-GHz wireless microcontrollers impedance matched balun and Tx harmonics filter
- Optimized for QFN STM32WL sub-GHz wireless microcontrollers in high power mode and dedicated to 2-layer PCB
- 50 Ω nominal input / conjugate matched balun to QFN STM32WL
- 50 Ω nominal impedance on antenna side Tx and Rx
- Deep Tx rejection harmonic filter
- Low insertion loss
- Small footprint
- Low profile ≤ 630 µm after reflow
- High RF performance
- RF BOM and area reduction
- ECOPACK2 compliant component

## Applications

- STM32WL sub-GHz wireless microcontrollers
- LPWAN-compliant radio solution, enabling the following modulations: LoRa®, (G)FSK, (G)MSK, and BPSK

## Description

STMicroelectronics BALFLB-WL-09D3 is an ultra-miniature balun. This device integrates a matching network, balun, and harmonics filter. Matching impedance has been customized for the STM32WL sub-GHz wireless microcontrollers.

It is using STMicroelectronics IPD technology on a nonconductive glass substrate, which optimizes RF performances.

# 1 Characteristics

**Table 1. Absolute maximum ratings ($T_{amb}$ = 25 °C)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $P_{IN}$ | Input power $RF_{IN}$ | 27 | dBm |
| $V_{ESD}$ | ESD ratings human body model (JESD22-A114), all I/O one at a time while others connected to GND | 2000 | V |
| | ESD ratings machine model, all I/O | 200 | |
| $T_{OP}$ | Operating temperature | -40 to +105 | °C |

**Table 2. Impedances ($T_{amb}$ = 25 °C)**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $Z_{RX}$ | Nominal differential Rx balun impedance | - | Matched to STM32WL | - | Ω |
| $Z_{TX}$ | Nominal Tx filter impedance | - | Matched to STM32WL | - | |
| $Z_{RX-ANT}$ | Nominal Rx balun antenna impedance | - | 50 | - | |
| $Z_{TX-ANT}$ | Nominal Tx filter antenna impedance | - | 50 | - | |

**Table 3. Electrical characteristics and RF performances ($T_{amb}$ = 25 °C)**

| Symbol | Parameter | Test condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| f | Frequency range | | 470 | 490 | 510 | MHz |
| $IL_{RX}$ | Rx balun insertion loss differential mode $\|S_{DS}\|$ without mismatch loss | | | 1.90 | 2.15 | dB |
| $IL_{TX}$ | HP Tx filter insertion loss $\|S_{21}\|$ without mismatch loss | | | 1.65 | 2.00 | dB |
| $RL_{RX-ANT}$ | Rx balun input return loss differential mode $\|S_{DD}\|$ on antenna | | 14 | 18 | | dB |
| $RL_{TX-ANT}$ | Tx filter output return loss $\|S_{11}\|$ on antenna | | 16 | 18 | | dB |
| $\phi_{imb}$ | RX balun phase imbalance | | -2.8 | | 2.8 | ° |
| $A_{imb}$ | RX balun amplitude imbalance | | -1.1 | | 1.1 | dB |
| $Att_{TX}$ | Tx filter harmonic rejection levels $\|S_{21}\|$ | Attenuation at 2fo | 44 | 48 | | dB |
| | | Attenuation at 3fo | 47 | 53 | | |
| | | Attenuation at 4fo | 42 | 45 | | |
| | | Attenuation at 5fo | 44 | 46 | | |
| | | Attenuation at 6fo | 48 | 52 | | |
| | | Attenuation at 7fo | 37 | 44 | | |
| | | Attenuation at 8fo | 31 | 36 | | |
| | | Attenuation at 9fo | 25 | 31 | | |
| | | Attenuation at 10fo | 22 | 27 | | |

## 1.1 RF measurements (Rx balun)

**Figure 1. Insertion loss (dB)**

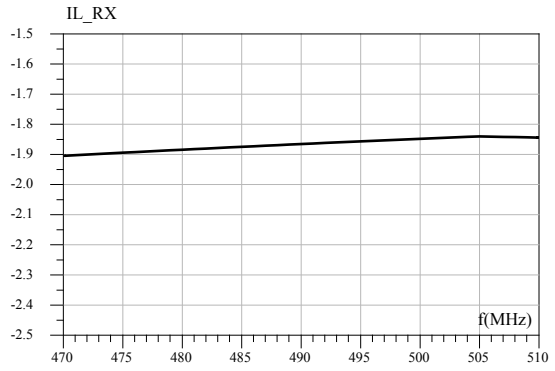



**Figure 2. Return loss on antenna (dB)**

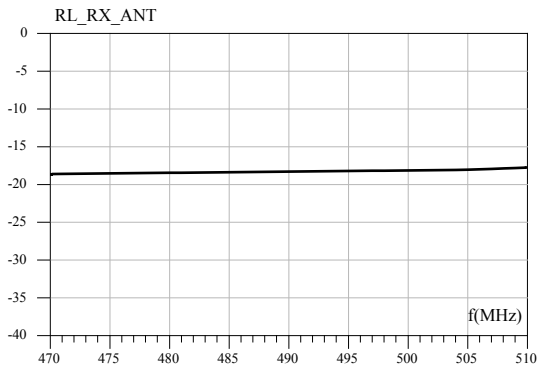



**Figure 3. Amplitude imbalance (dB)**

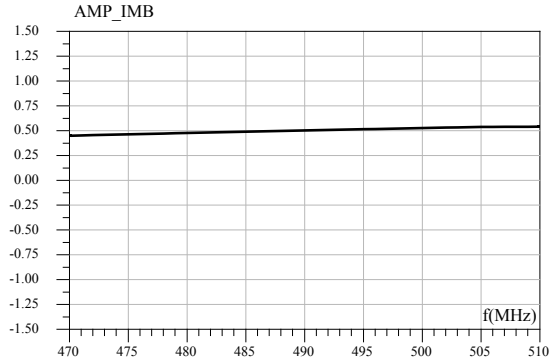
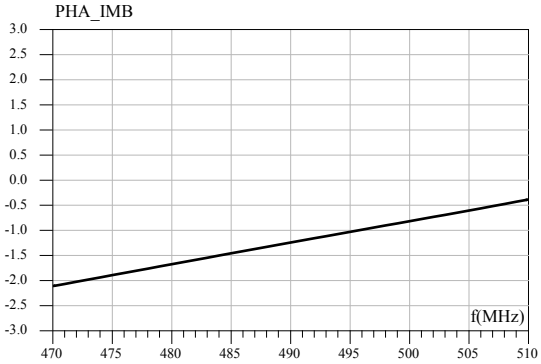



**Figure 4. Phase imbalance (°)**



## 1.2 RF measurements (Tx filter)

**Figure 5. Transmission wide band with harmonics attenuation (dB)**

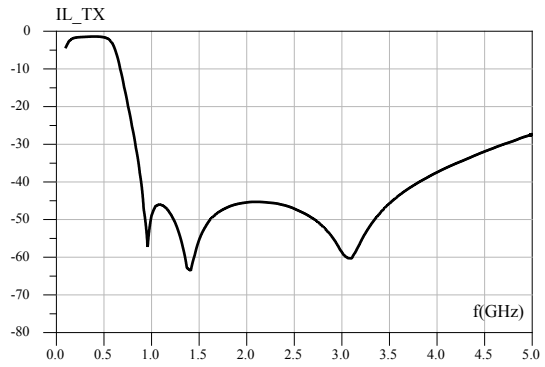



**Figure 6. Insertion loss (dB)**

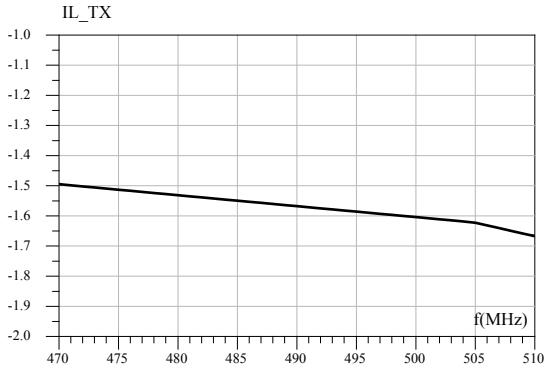
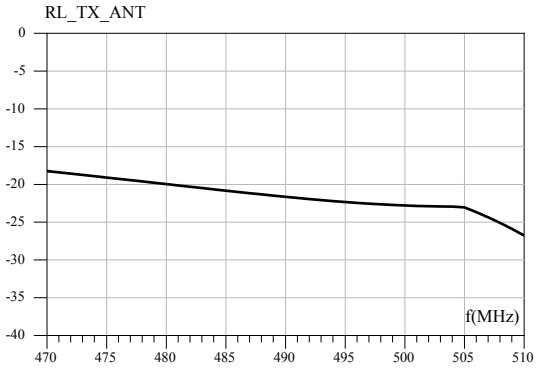



**Figure 7. Return loss on antenna (dB)**



# 2 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 2.1 CSPG package information

**Figure 8. CSPG 8 bumps package outline (bottom view - bumps up)**

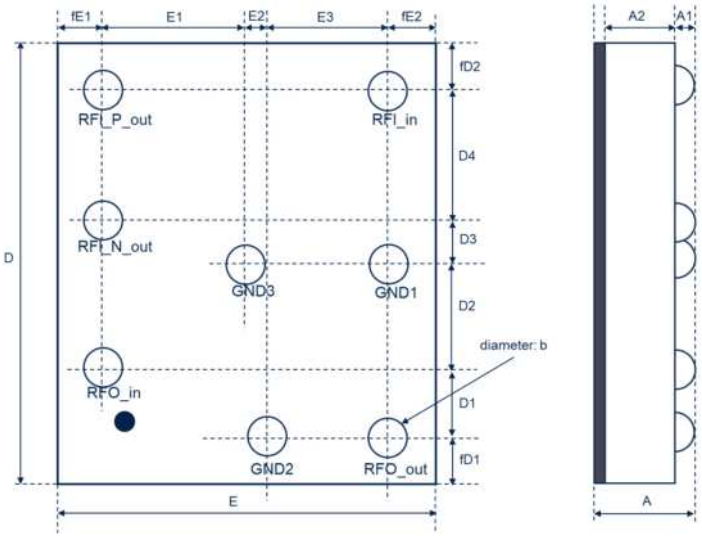



**Table 4. CSPG 8 bumps mechanical data**

| Ref. | Dimensions | | |
|---|---|---|---|
| | Millimeters | | |
| | Min. | Typ. | Max. |
| A | 0.580 | 0.630 | 0.680 |
| A1 | 0.180 | 0.205 | 0.230 |
| A2 | 0.380 | 0.400 | 0.420 |
| b | 0.230 | 0.255 | 0.280 |
| D | 2.100 | 2.150 | 2.200 |
| D1 | | 0.340 | |
| D2 | | 0.500 | |
| D3 | | 0.210 | |
| D4 | | 0.630 | |
| E | 1.800 | 1.850 | 1.900 |
| E1 | | 0.690 | |
| E2 | | 0.085 | |
| E3 | | 0.605 | |
| fD1 | | 0.235 | |
| fD2 | | 0.235 | |
| fE1 | | 0.235 | |
| fE2 | | 0.235 | |

## 2.2 CSPG 8 bumps packing information

**Figure 9. Marking**




**Figure 10. Top view**

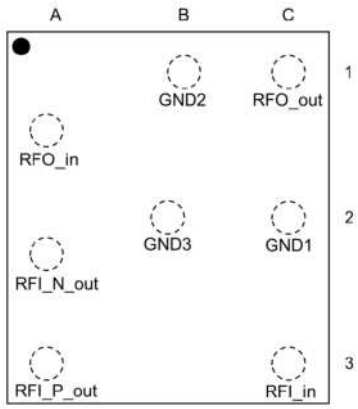
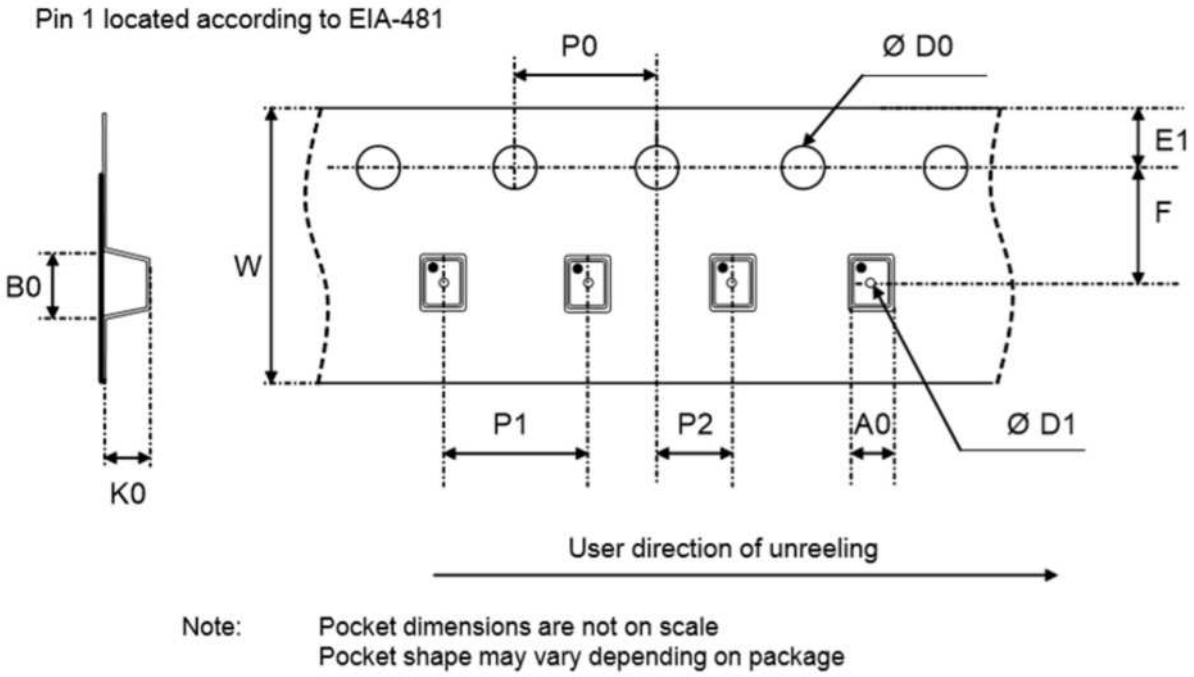



**Table 5. Pads description top view (pads down)**

| Pad ref. | Pad name | Description |
|---|---|---|
| A1 | RFO_in | Tx filter input |
| A2 | RFI_N_out | Differential-N Rx balun output |
| A3 | RFI_P_out | Differential-P Rx balun output |
| B1 | GND2 | Ground #2 |
| B2 | GND3 | Ground #3 |
| C1 | RFO_out | Tx filter output |
| C2 | GND1 | Ground #1 |
| C3 | RFI_in | Single ended Rx balun input |

Figure 11. **Tape and reel outline**




Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Table 6. **Tape and reel mechanical data**

| Ref | Dimensions | | |
|---|---|---|---|
| | Millimeters | | |
| | Min | Typ | Max |
| A0 | 1.89 | 1.94 | 1.99 |
| B0 | 2.19 | 2.24 | 2.29 |
| Ø D0 | 1.40 | 1.50 | 1.60 |
| Ø D1 | 0.95 | 1.00 | 1.05 |
| E1 | 1.65 | 1.75 | 1.85 |
| F | 3.45 | 3.50 | 3.55 |
| K0 | 0.70 | 0.75 | 0.80 |
| P0 | 3.90 | 4.00 | 4.10 |
| P1 | 3.90 | 4.00 | 4.10 |
| P2 | 1.95 | 2.00 | 2.05 |
| W | 7.90 | 8.00 | 8.30 |

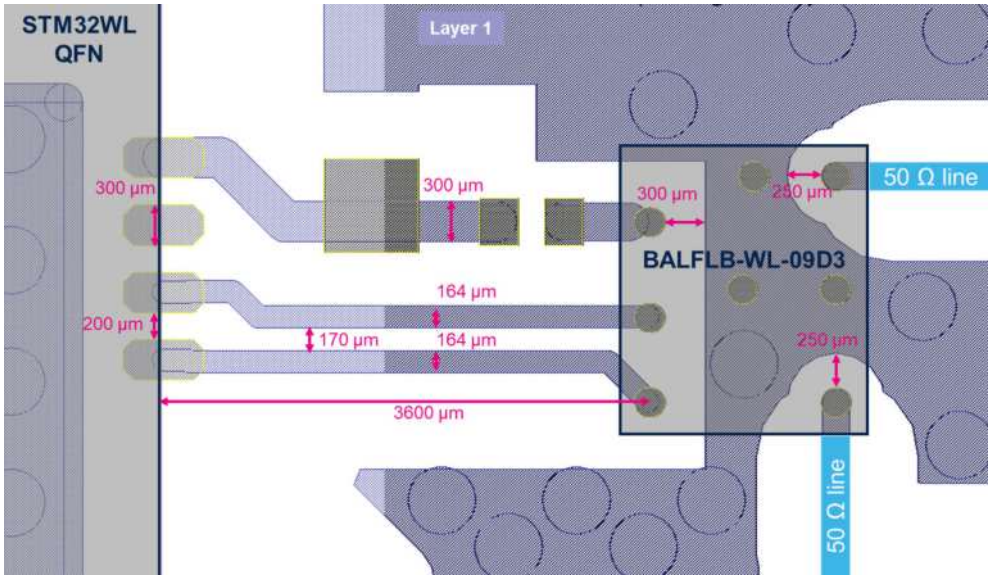
*Note: More packing information is available in the application note:*

- *AN2348 Flip-Chip: "Package description and recommendations for use"*

# 3 PCB assembly recommendations

## 3.1 Land pattern

Figure 12. **QFN-2L PCB land pattern recommendation**




The land pattern on layer 1 must be respected as described in Figure 12.

The ground plane on layer 1 is mandatory under the BALF, with its shape and definition optimized to achieve the best possible equipotentiality.

The density of vias and drills must be maximized near the BALF area to ensure optimal RF performance.

The layout around the IPD must be followed as closely as possible.

Table 7. **Characteristic impedances of RF transmission lines for a QFN package with a 2-layer PCB in high power mode**

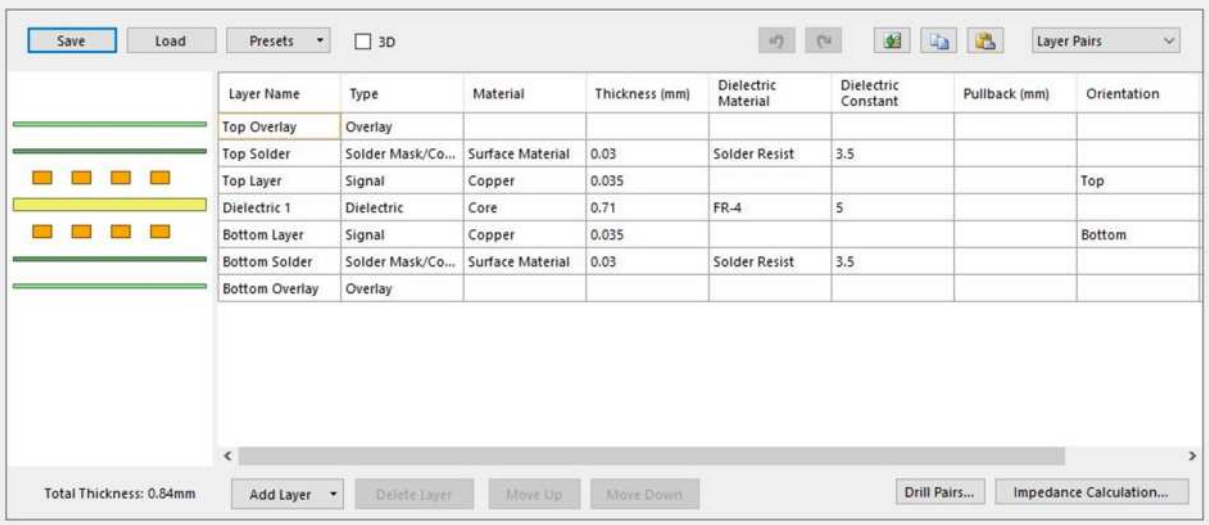
| RF transmission line | Type | Value | Unit | Description |
|---|---|---|---|---|
| RFO_out Antenna | $Z_0$ | 50 | Ω | Line between the BALF RFO_out pin and the Tx antenna |
| RFI_in Antenna | $Z_0$ | 50 | Ω | Line between the BALF RFI_in pin and the Rx antenna |
| RFO_HP | $Z_0$ | 92 | Ω | Line between the BALF RFO pin and the STM32 RFO_HP pin |
| RFI_out | $Z_0$ | 92 | Ω | Differential lines between the BALF RFI_x_out pins and the STM32 RFI_x_out pins |
| | $Z_{odd}$ | 55 | Ω | |
| | $Z_{even}$ | 154 | Ω | |

The characteristic impedances and lengths of the transmission lines must also be followed as precisely as possible.

Moreover, the physical dimensions of the lines must be adjusted according to the specific PCB stack-up, if it differs from the one presented in the datasheet, to maintain the expected characteristic impedance values.

The dimensions of the lines were calculated considering the ground plane on layer 2.

Figure 13. **Stack-up recommendation for a QFN-2L PCB**

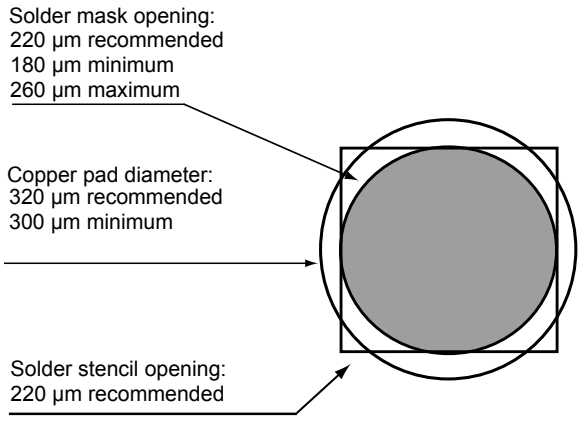



The PCB stack-up presented above is the one used to validate the product. The PCB dimensions should closely follow the recommendations, particularly the thickness of the dielectric between layer 1 and layer 2, which must remain within ±30 % of the specified values (that is, between 500 and 900 µm for a 2-layer PCB dedicated to the QFN package).

Other dimensions may vary without significantly impacting the overall functionality of the product.

## 3.2 Stencil opening design

Figure 14. **Footprint - 3 mils stencil - solder mask defined**




## 3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-38 µm.

## 3.4 Placement

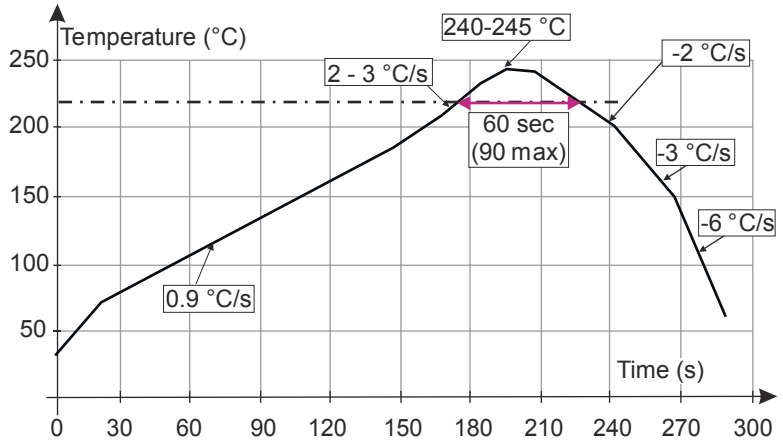
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

## 3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

## 3.6 Reflow profile

**Figure 15. ST ECOPACK® recommended soldering reflow profile for PCB mounting**




*Note: Minimize air convection currents in the reflow oven to avoid component movement.*

*Note: More information is available in the application note:*

- *AN2348 Flip-Chip: "Package description and recommendations for use"*

# 4 Ordering information

Table 8. **Ordering information**

| Order code | Marking | Package | Weight | Base qty. | Delivery mode |
|---|---|---|---|---|---|
| BALFLB-WL-09D3 | W9 | CSPG | 3.9 mg | 5000 | Tape and reel |

## Revision history

Table 9. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 14-Oct-2022 | 1 | Initial release. |
| 21-Dec-2022 | 2 | Updated *Table 1. Absolute maximum ratings ($T_{amb}$ = 25 °C)*. |
| 15-Jul-2025 | 3 | Updated Section 3.1: Land pattern, and Section 3.2: Stencil opening design. |

**IMPORTANT NOTICE – READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2025 STMicroelectronics – All rights reserved