Enpirion® Power Datasheet

EN5366QI 6A PowerSoC
Voltage Mode Synchronous Buck PWM DC-DC Converter with Integrated Inductor
External Output Voltage Programming

Not Recommended For New Designs

Description

This Altera Enpirion solution is a Power System on a chip (PowerSoC). It is specifically designed to meet the precise voltage and fast transient requirements of present and future high-performance, low-power processor, DSP, FPGA, ASIC, memory boards and system level applications in a distributed power architecture. Advanced circuit techniques, ultra high switching frequency, and very advanced, high-density, integrated circuit and proprietary inductor technology deliver high-quality, ultra compact, non-isolated DC-DC conversion. Operating this converter requires as few as three external components that include small value input and output ceramic capacitors and a soft-start capacitor.

The Altera Enpirion integrated inductor solution significantly helps in low noise system design and productivity by offering greatly simplified board design, layout and manufacturing requirements.

All Altera Enpirion products are RoHS compliant and lead-free manufacturing environment compatible.

Typical Application Circuit

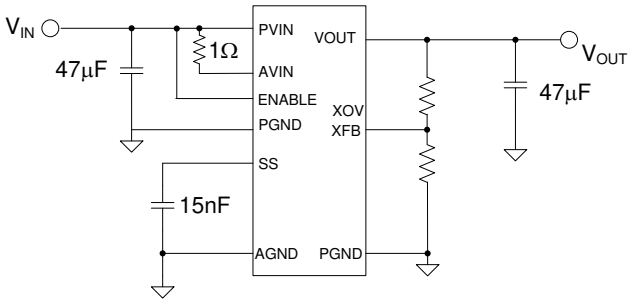


Figure 1. Simple Schematic

Features

- Integrated INDUCTOR, MOSFETS, Controller
- Footprint 1/3rd that of competing solutions.
- Low Part Count: only 3 MLCC Capacitors.
- Up to 20W continuous output power.
- Low output impedance optimized for ≤ 90 nm
- Master/slave configuration for paralleling.
- 5MHz operating frequency.
- High efficiency, up to 93%.
- Wide input voltage range of 2.375V to 5.5V.
- External resistor divider output voltage select.
- Output enable pin and Power OK signal.
- Programmable soft-start time.
- Optimized for low noise/EMI design.
- Under-Voltage Lockout, Thermal Shutdown, Output Overvoltage, Over Current, and Short Circuit Protection
- RoHS compliant, MSL level 3, 260C reflow.

Applications

- Point of load regulation for low-power processors, network processors, DSPs, FPGAs, and ASICs
- ≤ 90 nm advanced process loads
- Notebook computers, servers, workstations
- Broadband, networking, LAN/WAN, optical
- Low voltage, distributed power architectures with 2.5V, 3.3V or 5V rails
- DSL, STB, DVR, DTV, Industrial PC
- Ripple sensitive applications

Ordering Information

Part Number	Temp Rating (°C)	Package
EN5366QI	-40 to +85	58-pin QFN T&R
EN5366QI-E	QFN Evaluation Board	

*Optimized PCB Layout file downloadable from www.altera.com/enpirion to assure first pass design success.

Pin Configuration

Below is a top view diagram of the EN5366Q package.

NOTE: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

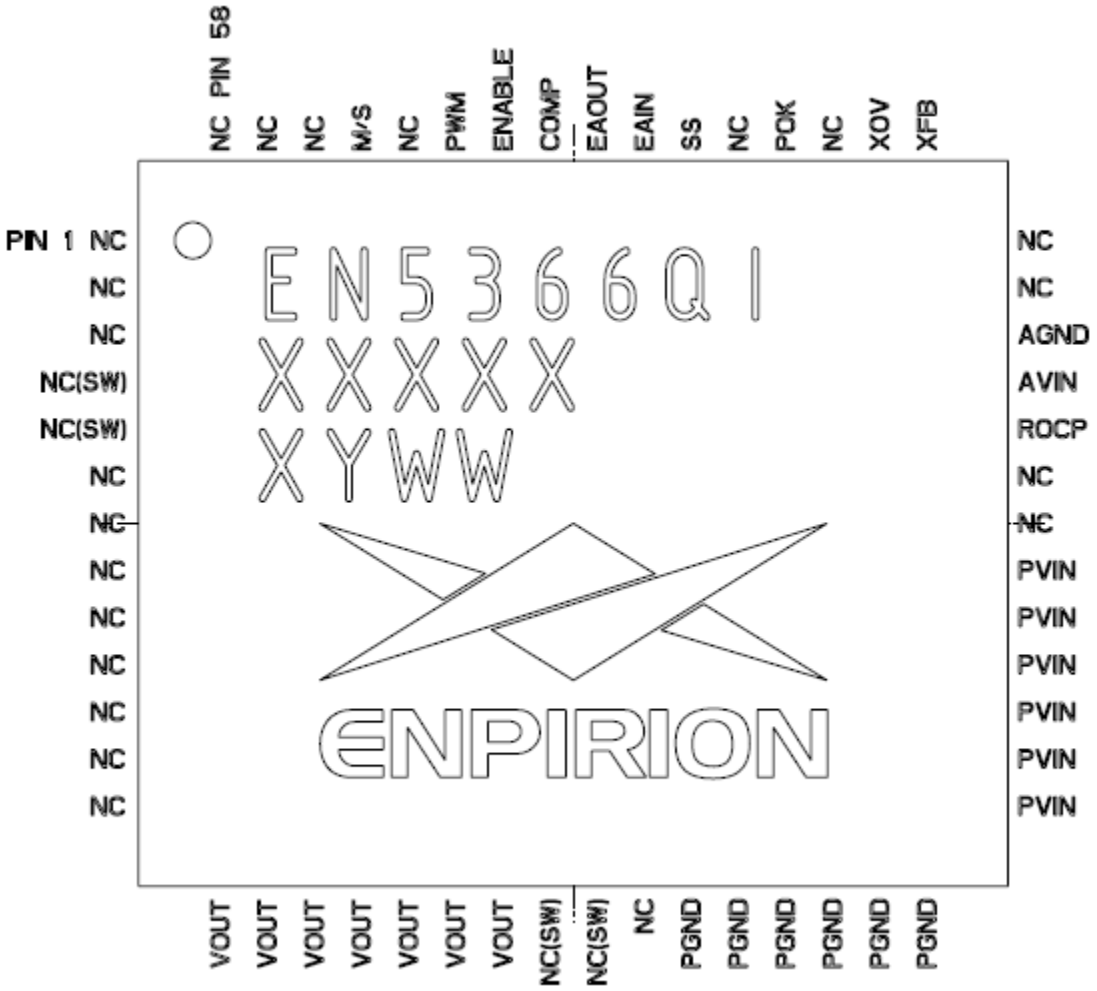


Figure 2. Pin Diagram, top view.

Pin Descriptions

PIN	NAME	FUNCTION
1-3	NC	NO CONNECT: These pins should not be electrically connected to each other or to any external signal, voltage, or ground. One or more of these pins may be connected internally.
4-5	NC(SW)	NO CONNECT – These pins are internally connected to the common drain output of the internal MOSFETs. NC(SW) pins are not to be electrically connected to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.
6-13	NC	NO CONNECT: These pins should not be electrically connected to each other or to any external signal, voltage, or ground. One or more of these pins may be connected internally.
14-20	VOUT	Regulated converter output. Decouple with output filter capacitor to PGND. Refer to layout section for specific layout requirements
21-22	NC(SW)	NO CONNECT – These pins are internally connected to the common drain output of the internal MOSFETs. NC(SW) pins are not to be electrically connected to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.
23	NC	NO CONNECT: These pins should not be electrically connected to each other or to any external signal, voltage, or ground. One or more of these pins may be connected internally.
24-29	PGND	Output power ground. Refer to layout section for specific layout requirements.
30-35	PVIN	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND. Refer to layout section for specific layout requirements
36-37	NC	NO CONNECT: These pins should not be electrically connected to each other or to any external signal, voltage, or ground. One or more of these pins may be connected internally.
38	ROCP	Optional Over Current Protection adjust pin. Used for diagnostic purposes only. Place 10kΩ resistor between this pin and AGND (pin 40) to raise the over current trip point to approximately 200% of maximum rated current.
39	AVIN	Analog voltage input for the controller circuits. Connect this pin to PVIN using a 1 Ohm resistor.
40	AGND	Analog ground for the controller circuits.
41-42	NC	NO CONNECT: These pins should not be electrically connected to each other or to any external signal, voltage, or ground. One or more of these pins may be connected internally.
43	XFB	Feedback pin for external voltage divider network.
44	XOV	Over voltage programming feedback pin.
45	NC	NO CONNECT: This pin should not be electrically connected to any other NC pin, or to any external signal, voltage, or ground. This pin may be connected internally.
46	POK	Power OK is an open drain transistor for power system state indication. POK is a logic high when VOUT is with -10% to +20% of VOUT nominal. Size pull-up resistor to limit current to 4mA when POK is low.
47	NC	NO CONNECT: These pins should not be electrically connected to each other or to any external signal, voltage, or ground. One or more of these pins may be connected internally.
48	SS	Soft-Start node. The soft-start capacitor is connected between this pin and AGND. The value of this capacitor determines the startup timing.
49	EAIN	Optional Error Amplifier input. Allows for customization of the control loop.
50	EAOUT	Optional Error Amplifier output. Allows for customization of the control loop.
51	COMP	Optional Error Amplifier Buffer output. Allows for customization of the control loop.

PIN	NAME	FUNCTION
52	ENABLE	Input Enable. Applying a logic high, enables the output and initiates a soft-start. Applying a logic low disables the output.
53	PWM	PWM input/output. Used for optional master/slave configuration. When M/S pin is asserted “low”, PWM will output the gate-drive PWM waveform. When the M/S pin is asserted “high”, the PWM pin is configured as an input for PWM signal from the “master” device. PWM pin can drive up to 3 slave devices. NOTE: Leave this pin open when not using parallel mode.
54	NC	NO CONNECT: These pins should not be electrically connected to each other or to any external signal, voltage, or ground. One or more of these pins may be connected internally.
55	M/S	Optional Master/Slave select pin. Asserting pin “low” places device in Master Mode for current sharing. PWM pin (53) will output PWM drive signal. Asserting pin “high” will place the device in Slave Mode. PWM pin (53) will be configured to input (receive) PWM drive signal from “Master” device. NOTE: Leave this pin open when not using parallel mode.
56-58	NC	NO CONNECT: These pins should not be electrically connected to each other or to any external signal, voltage, or ground. One or more of these pins may be connected internally.

Block Diagram

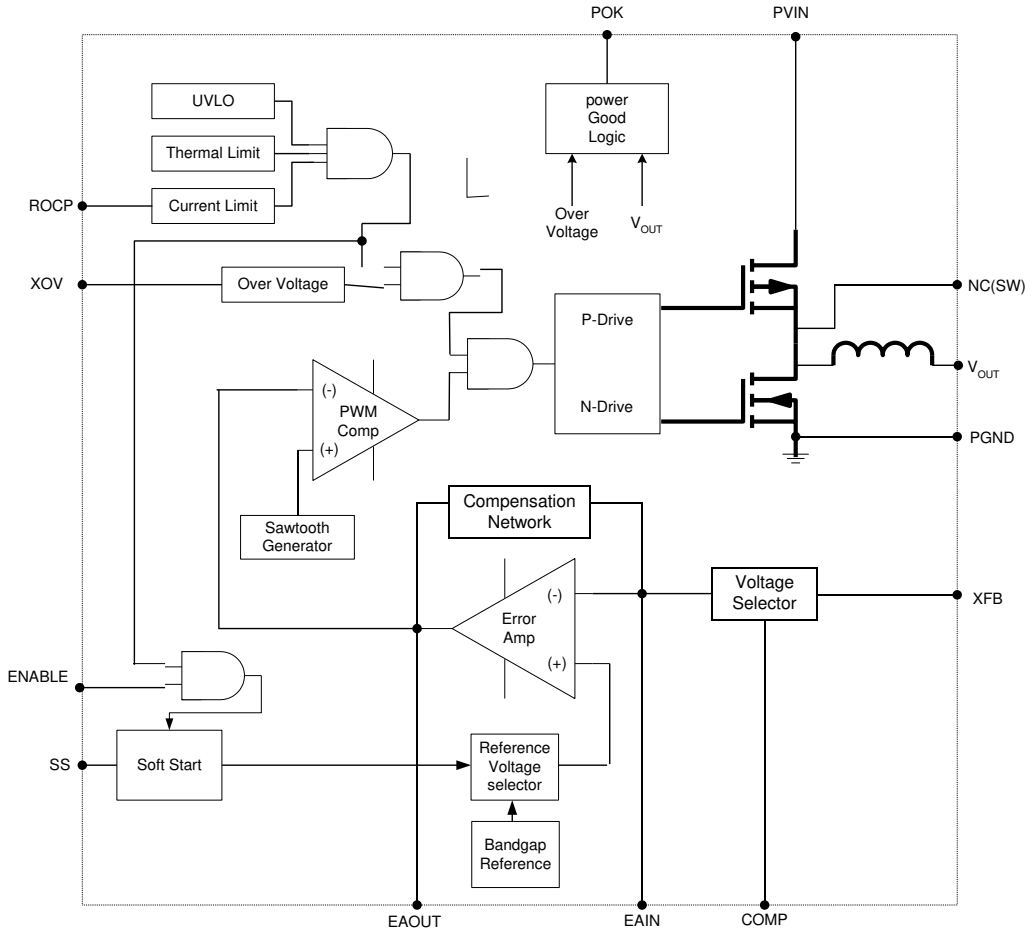


Figure 3. System block diagram.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond recommended operating conditions is not implied. Stress beyond absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Supply Voltage	V_{IN}	-0.5	7.0	V
Voltages on: ENABLE,		-0.5	V_{IN}	V
Voltage on XFB, XOV		-0.5	2.5	V
Voltages on: EAIN, EAOUT, COMP		-0.5	2.5	V
Voltages on: SS, PWM		-0.5	3.0	V
Voltages on: POK		-0.5	V_{IN} + 0.3	V
Storage Temperature Range	T_{STG}	-65	150	°C
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating (based on Human Body Model)			2000	V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.375	5.5	V
Output Voltage Range	V_{OUT}	0.75	3.3	V
Operating Ambient Temperature	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Ambient (0 LFM) **(Note 1)**	θ_{JA}	20	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	1.5	°C/W
Thermal Overload Trip Point	$T_{J\text{-}TP}$	+150	°C
Thermal Overload Trip Point Hysteresis		20	°C

NOTES:

1. Based on a four-layer board and proper thermal design in line with JEDEC EIJ/JESD 51 Standards.

Electrical Characteristics

NOTE: V_{IN}=5.5V over operating temperature range unless otherwise noted.
Typical values are at T_A = 25°C.

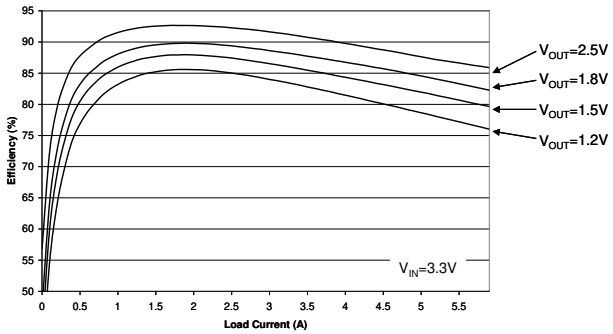
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}		2.375		5.5	V
Output Regulation						
Feedback Pin Voltage	V_{OUT}	2.375V ≤ VIN ≤ 5.5V, I_{LOAD} = 1A; T_A = 25°C	0.735	0.750	0.765	V
Feedback Pin Voltage	V_{OUT}	2.375V ≤ V_{IN} ≤ 5.5V, 0A ≤ I_{LOAD} ≤ 6A -40 ºC ≤ T_A ≤ +85 ºC	0.725	0.750	0.773	V
Transient Response (I_{OUT} = 0% to 100% or 100% to 0% of Rated Load)						
Peak Deviation	ΔV_{OUT}	V_{IN} = 5V, 1.2V < V_{OUT} < 3.3V C_{OUT}=50uF		3		%
Under Voltage Lockout						
Under Voltage Lock out threshold	V_{UVLO}	V_{IN} Increasing V_{IN} Decreasing		2.2 2.1		V
Switching Frequency						
Switching Frequency	F_{SWITCH}			5		MHz
Load Characteristics						
Maximum Continuous Output Current	I_{OUT}	**(Note 2)**	6			A
Current Limit Threshold	I_{OCP_TH}			9		A
Supply Current						
Shut-Down Supply Current	I_S	ENABLE=0V		50		µA
Enable Operation						
Disable Threshold	$V_{DISABLE}$	Max voltage to ensure the converter is disabled			0.8	V
Enable Threshold	V_{ENABLE}	2.375V ≤ V_{IN} ≤ 5.5V	1.8			V
Enable Pin Current	I_{EN}	V_{IN} = 5.5V		50		µA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Select Operation						
Logic Low Threshold	V_{SX-Low}	Threshold voltage for Logic Low			0.8	V
Logic High Threshold	$V_{SX-High}$	Threshold voltage for Logic High (internally pulled high; can be left floating to achieve logic high)	1.8		V_{IN}	V
V_{Sx} Pin Current	I_{VSX}	VIN = 5.5V V_{Sx} = GND V_{Sx} = V_{IN} V_{Sx} = Open		50 0 0		µA
Power OK Operation (Open Drain)						
POK threshold High		Percentage of V_{OUT} Nominal		120		%
POK threshold low		Percentage of V_{OUT} Nominal		90		%
POK Low Voltage		I_{POK} = 4 mA (Max sink Current)			0.4	V
POK High Voltage					V_{IN}	%
Output Rise Time						
V_{OUT} Rise Time Accuracy	ΔT_{RISE}	T_{RISE} = C_{ss}* 75KΩ; 10nF ≤ C_{SS} ≤30nF **(Note 3)**	-25		+25	%
Parallel Operation						
Current Balance	ΔI_{OUT}	With 2 – 4 converters in parallel, the difference between any 2 parts. ΔV_{IN} < 50mV; R_{TRACE} < 10mΩ.		+/-10		%

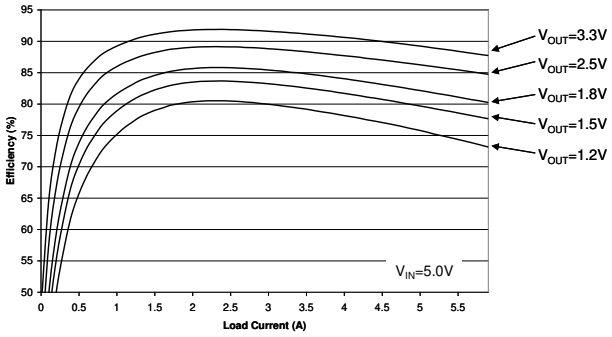
NOTES:

2. Maximum output current may need to be de-rated, based on operating condition, to meet T_J requirements.
3. Parameter not production tested but is guaranteed by design. Rise time begins when AVIN > V_{UVLO} and Enable=HIGH.

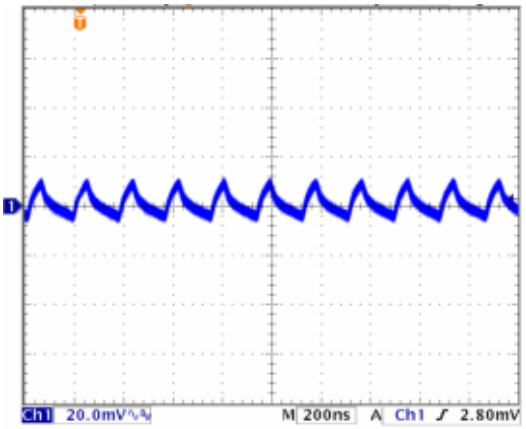
Typical Performance Characteristics



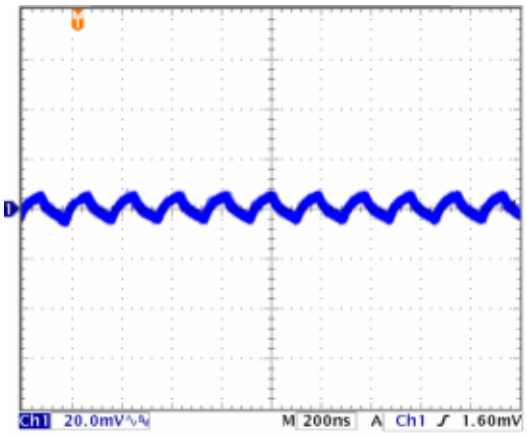
Efficiency vs. Load, V_{IN} = 3.3V.; Load = 0-6A.



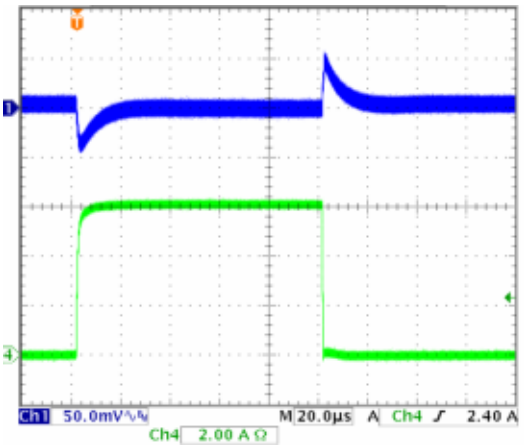
Efficiency vs. Load, V_{IN} = 5.0V.; Load = 0-6A.



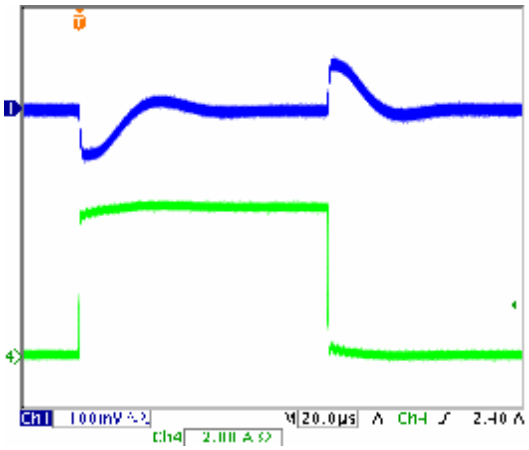
Ripple Voltage, 5.0V_{IN}/1.2V_{OUT}, I_{OUT}=6A, C_{OUT} = 3x22uF.



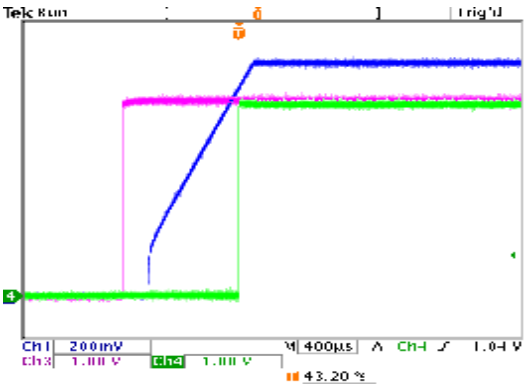
Ripple Voltage, 3.3V_{IN}/1.2V_{OUT}, I_{OUT}=6A, C_{OUT} = 3x22uF.



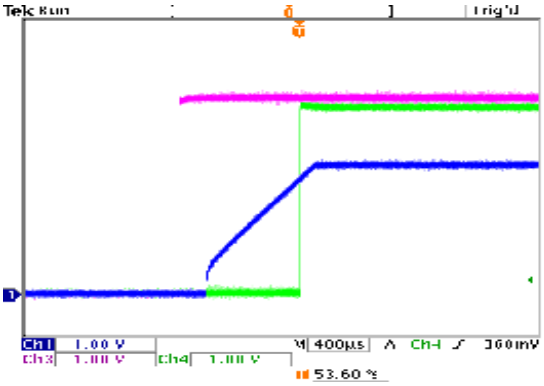
Transient Response 5.5V_{IN}/1.2V_{OUT}, 0-6A, 10A/uS. C_{OUT}=50uF.



Transient Response 5.5V_{IN}/3.3V_{OUT}, 0-6A, 10A/uS. C_{OUT}=50uF



Start up waveforms V_{IN}=5.0V, V_{OUT}=1.2V, C_{SS}=15nF, Ch 1 = V_{OUT}, Ch 3 = ENABLE, Ch 4 = POK.



Start up waveforms V_{IN}=5.0V, V_{OUT}=3.3V, C_{SS}=15nF, Ch 1 = V_{OUT}, Ch 3 = ENABLE, Ch 4 = POK.

Theory of Operation

Synchronous Buck Converter

The EN5366 is a synchronous, programmable power supply with integrated power MOSFET switches and integrated inductor. The nominal input voltage range is 2.4-5.5V. The output voltage is programmed using an external resistor divider network. The feedback control loop is a type III voltage-mode and the part uses a low-noise PWM topology. Up to 6A of continuous output current can be drawn from this converter. The 5MHz operating frequency enables the use of small-size input and output capacitors.

The power supply has the following protection features:

- Programmable over-current protection (to protect the IC from excessive load current).
- Short Circuit protection.
- Thermal shutdown with hysteresis.
- Programmable over-voltage protection.
- Under-voltage lockout circuit to disable the converter output when the input voltage is less than approximately 2.2V

Additional features include:

- Soft-start circuit, to limit the in-rush current when the converter is powered up.
- Power good circuit (POK) indicating whether the output voltage is between 90% of nominal V_{OUT} and the OVP trip point.

Output Voltage Programming

The EN5366 output voltage is programmed using a simple resistor divider network. Figure 4 shows the resistor divider configuration.

The EN5366 output voltage and over voltage thresholds are determined by the voltages presented at the XFB and XOV pins respectively. These voltages are set by way of resistor dividers between V_{OUT} and AGND with the midpoint going to XFB and XOV.

It is recommended that Rb1 and Rb2 resistor values be ~2kΩ. Use the following equation to set the resistor Ra1 for the desired output voltage:

$$Ra1 = \frac{(Vout - 0.75V) * Rb1}{0.75V}$$

If over-voltage protection is desired, use the following equation to set the resistor Ra2 for the desired OVP trip-point:

$$Ra2 = \frac{(OVPtrip - 0.90V) * Rb2}{0.90V}$$

By design, if both resistor dividers are the same, the OV trip-point will be 20% above the nominal output voltage.

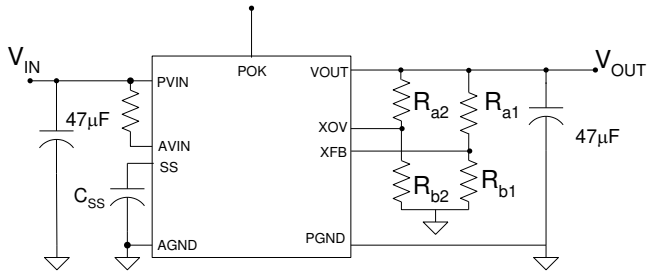


Figure 4. V_{OUT} and OVP resistor divider networks.

Input Capacitor Selection

The EN5366QI requires about 40-50uF of input capacitance. Low ESR ceramic capacitors are required with X5R or X7R dielectric formulation. Y5V or equivalent dielectric formulations must not be used as they lose capacitance with frequency, temperature and bias voltage.

In some applications, lower value ceramic capacitors maybe needed in parallel with the larger capacitors in order to provide high frequency decoupling.

Recommended Input Capacitors.

Description	MFG	P/N
22uF, 10V, X5R, 1206 (2 capacitors needed)	Murata	GRM31CR61A226ME19L
	Taiyo Yuden	LMK316BJ226ML-T

47uF, 10V, X5R, 1210 (1 capacitor needed)	Murata Taiyo Yuden	GRM32ER61A476KE20L LMK325BJ476MM-T

Output Capacitor Selection

The EN5366QI has been optimized for use with approximately 50µF of output capacitance. Low ESR ceramic capacitors are required with X5R or X7R dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose capacitance with frequency, temperature and bias voltage.

Recommended Output Capacitors.

Description	MFG	P/N
22uF, 6.3V, 10% X5R, 1206 (3 capacitors needed)	Murata Taiyo Yuden	GRM31CR60J226KE19L JMK316BJ226KL-T
47uF, 10V, 10% X5R, 1210	Murata	GRM32ER61A476KE20L
47uF, 6.3V, 10% X5R, 1210 (1 capacitor needed)	AVX	12106D476KAT2

Output ripple voltage is primarily determined by the aggregate output capacitor impedance. At the 5MHz switching frequency output impedance, denoted as Z, is comprised mainly of effective series resistance, ESR, and effective series inductance, ESL:

Z = ESR + ESL.

Placing output capacitors in parallel reduces the impedance and will hence result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + ... + \frac{1}{Z_n}$$

Typical ripple versus capacitor arrangement is given below:

Output Ripple vs Capacitor Configuration.

Output Capacitor Configuration	Typical Output Ripple (mVp-p) (as measured on EN5366QI Evaluation Board)
1 x 47uF	30
3 x 22 uF	15

Compensation

The EN5366 is internally compensated through the use of a type 3 compensation network and is optimized for use with about 50µF of output capacitance and will provide excellent loop bandwidth and transient performance for most applications. Voltage mode operation provides high noise immunity at light load. Further, Voltage mode control provides superior impedance matching to sub 90nm loads.

In some cases modifications to the compensation may be required. The EN5366QI provides the capability to modify the control loop to allow for customization for a given application. For more information, contact Altera Power Applications support.

Enable Operation

The ENABLE pin provides a means to shut down the device, or enable normal operation. A logic low will disable the converter and cause it to shut down. A logic high will enable the converter into normal operation. When the ENABLE pin is asserted high, the device will undergo a normal soft start.

Soft-Start Operation

The SS pin in conjunction with a small capacitor between this pin and AGND provides the soft start function to limit the in-rush current during start-up. During start-up of the converter the reference voltage to the error amplifier is gradually increased to its final level by an internal current source of typically 10uA charging the soft start capacitor. The typical soft-start time for the output to reach regulation voltage, from when AVIN > V_{UVLO} and Enable crosses its logic high threshold, is given by:

$$T_{SS} = C_{SS} * 75K\Omega \text{ (seconds)}$$

Where the soft-start time T_{SS} is in seconds and the soft-start capacitance C_{SS} is in Farads. Typically, a capacitor of around 15nF is recommended.

During the soft-start cycle, when the soft-start capacitor reaches 0.75V, the output has reached its programmed regulation range. Note that the soft-start current source will continue to operate, and during normal operation, the soft-start capacitor will charge up to a final value of 2.5V.

POK Operation

The POK signal is an open drain signal from the converter indicating the output voltage is within the specified range. The POK signal will be a logic high when the output voltage is within 90% - 120% of the programmed output voltage. If the output voltage goes outside of this range, the POK signal will be a logic low until the output voltage has returned to within this range. In the event of an over-voltage condition the POK signal will go low and will remain in this condition until the output voltage has dropped to 95% of the programmed output voltage before returning to the high state.

The internal POK FET is designed to tolerate up to 4mA. The pull-up resistor value should be chosen to limit the current from exceeding this value when POK is logic low.

Over-Current Protection

The current limit function is achieved by sensing the current flowing through a sense P-MOSFET. When the sensed current exceeds the current limit, both NFET and PFET switches are turned off. If the over-current condition is removed, the over-current protection circuit will re-enable the PWM operation. If the over-current condition persists, the circuit will continue to protect the load.

The OCP trip point is nominally set to 150% of maximum rated load. For diagnostic purposes, it is possible to increase the OCP trip point to approximately 200% of the maximum rated load by connecting a 10kΩ resistor between the ROCP pin (pin 38) and AGND (pin 39). This is intended for troubleshooting purposes only and the specification is not guaranteed.

Over-Voltage Protection

When the output voltage exceeds 120% of the programmed output voltage, the PWM operation stops, the lower N-MOSFET is turned on and the POK signal goes low. When the output voltage drops below 95% of the programmed output voltage, normal PWM operation resumes and POK returns to its high state.

Thermal Overload Protection

Thermal shutdown will disable operation when the Junction temperature exceeds approximately 150ºC. Once the junction temperature drops by approx 20ºC, the converter will re-start with a normal soft-start.

Input Under-Voltage Lock-Out

Circuitry is provided to ensure that when the input voltage is below the required voltage level (V_{UVLO}) for normal operation, the converter will not start-up. Circuits for hysteresis and input de-glitch are included to ensure high noise immunity and to prevent false tripping.

Parallel Device Operation

The EN5366QI is capable of paralleling up to a total of four converters to provide up to 24A of continuous current. Please consult Paralleling Circuit Design with EN5365/66 for more details and recommendations.

Power-Up/Down Sequencing

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. The PVIN should never be powered when AVIN is off. During power down, the AVIN should not be powered down before the PVIN. Tying PVIN and AVIN or all three pins (AVIN, PVIN, ENABLE) together during power up or power down meets these requirements.

Pre-Bias Start-up

The EN5366QI does not support startup into a pre-biased condition. Be sure the output capacitors are not charged or the output of the EN5366QI is not pre-biased when the EN5366QI is first enabled.

Layout Recommendations

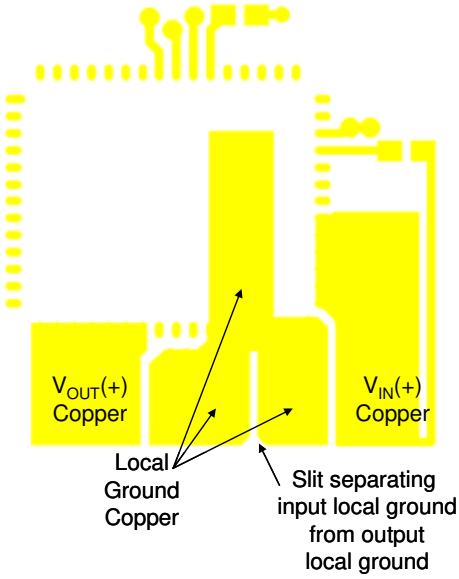


Figure 5. Layout of power and ground copper.

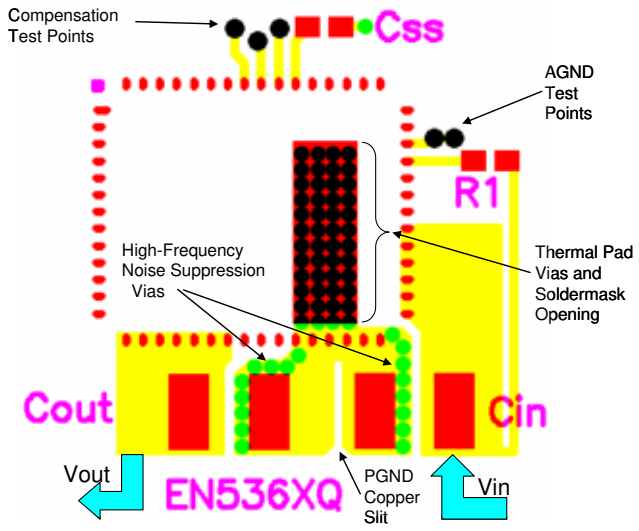


Figure 6. Use of thermal & noise suppression vias.

Recommendation 1: Input and output filter capacitors should be placed as close to the EN5366QI package as possible to reduce EMI from input and output loop currents. This reduces the physical area of the Input and Output AC current loops.

Recommendation 2: Place a slit in the input/output capacitor ground copper starting just below the common connection point of the device GND pins as shown in figures 5 and 6.

Recommendation 3: The large thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be less than 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.26mm. This connection provides the path for heat dissipation from the converter. Please see figures 6, 7, and 8.

Recommendation 4: Multiple small vias should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane as shown in figure 6. These vias can be the same size as the thermal vias discussed in recommendation 3.

Recommendation 5: The system ground plane referred to in recommendations 3 and 4 should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors shown in figure 6.

Recommendation 6: As with any switch-mode DC/DC converter, do not run sensitive signal or control lines underneath the converter package.

Please refer to the Gerber files and summarized layout notes available at www.altera.com/enpirion for more layout details.

NOTE: Figures 5 and 6 show only the critical components and traces for a minimum footprint layout. ENABLE, Vout-programming, and other small signal pins need to be connected and routed according to the specific application.

Design Considerations for Lead-Frame Based Modules

Exposed Metal on Bottom Of Package

Lead frame offers many advantages in thermal performance, in reduced electrical lead resistance, , and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package.

Only the large thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN5366QI should be clear of any metal except for the large thermal pad. The “grayed-out” area in Figure 7 represents the area that should be clear of any metal (traces, vias, or planes), on the top layer of the PCB.

Figure 8 demonstrates the recommended PCB footprint for the EN5366QI. Figure 9 shows the shape and location of the exposed metal pads as well as the mechanical dimension of the large thermal pad and the pins.

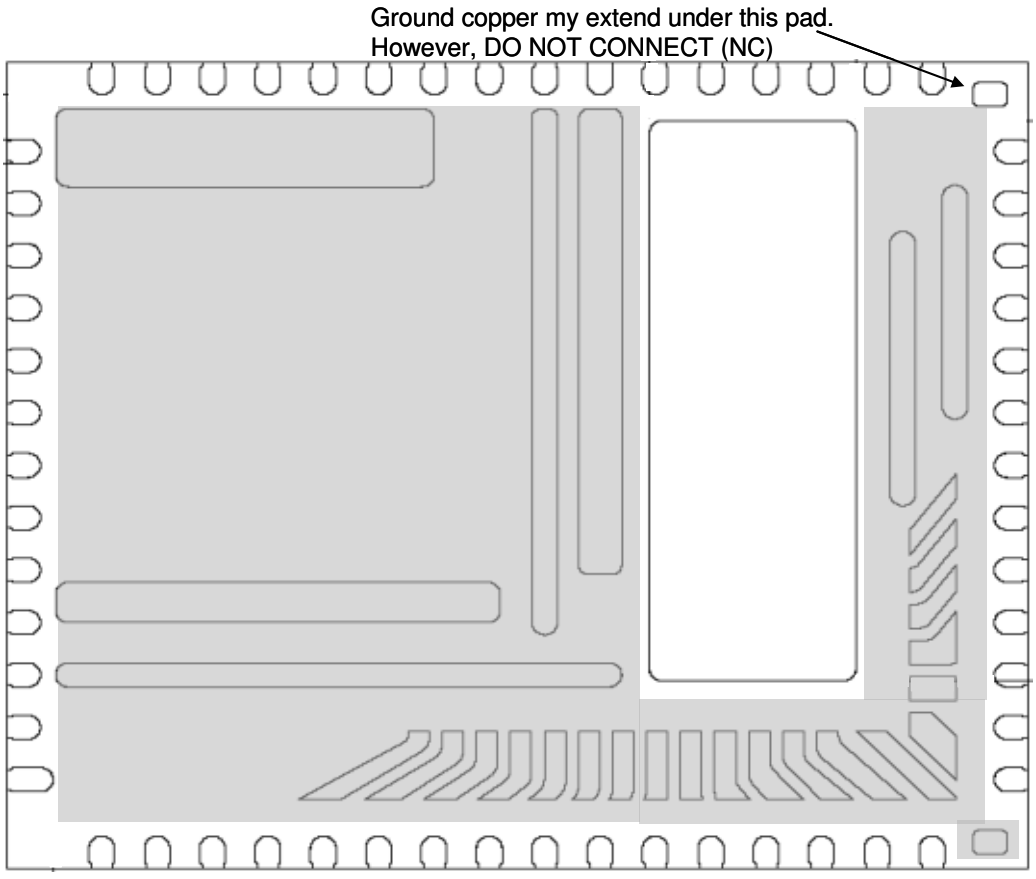


Figure 7. Lead-Frame exposed metal. Grey area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

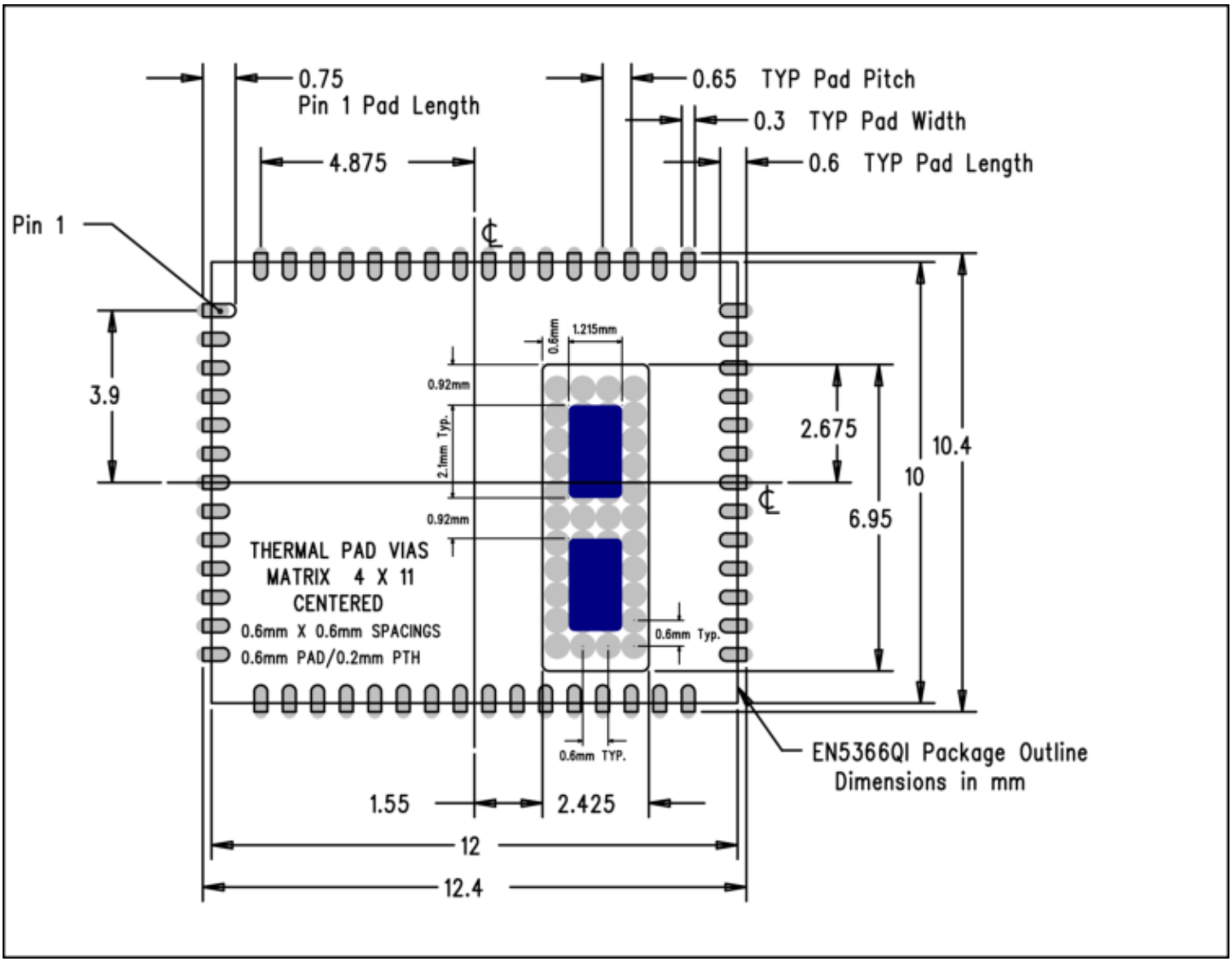


Figure 8: EN5366QI PCB Footprint (Top View)

The solder stencil aperture for the thermal pad is shown in blue and is based on Enpirion power product manufacturing specifications.

Package Dimensions

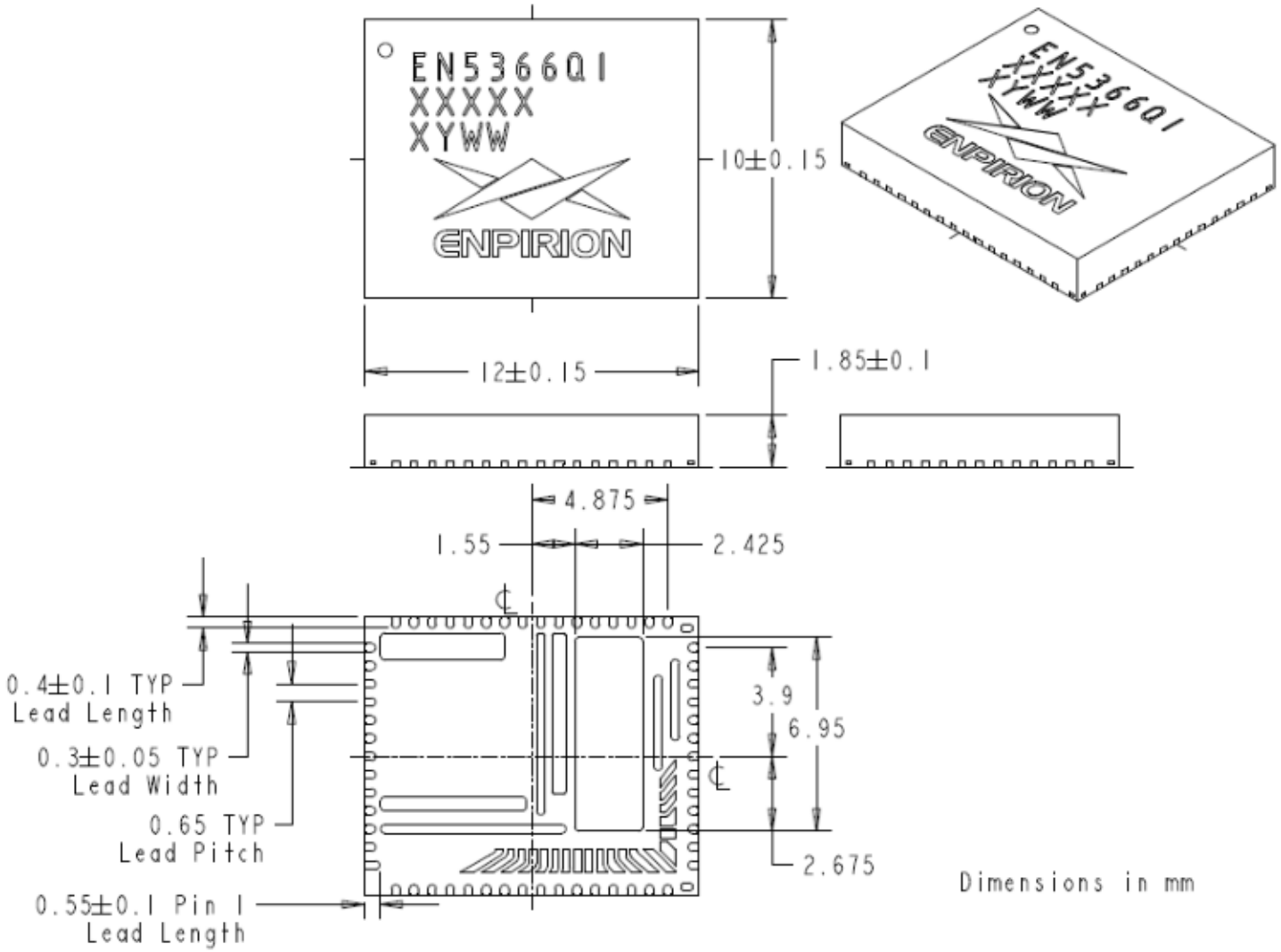


Figure 9. Package dimensions.

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