ESDS30x Data-Line Surge and ESD Protection Devices for High Speed Interfaces

1 Features

- IEC 61000-4-2 level 4 ESD protection:
  - ±30kV contact discharge
  - ±30kV air gap discharge
- IEC 61000-4-4 EFT protection:
  - 80 A (5/50ns)
- IEC 61000-4-5 surge protection:
  - 12A (8/20µs)
  - Low surge clamping voltage 6V at 12A Ipp
- IO capacitance:
  - 2.3pF (typical)
- DC breakdown voltage: 4.5V (minimum)
- Ultra low leakage current: 3nA (typical)
- Supports high speed interfaces up to 1 Gbps
- Industrial temperature range: –40°C to +125°C
- Easy flow-through routing package (ESDS302)

2 Applications

- End equipment:
  - Ethernet switches
  - Access points
  - Gateways
  - Printers
  - DVR and NVR
- Interfaces:
  - Ethernet 10/100/1000 Mbps
  - USB 2.0
  - GPIO

3 Description

The ESDS302, ESDS304 devices are uni-directional TVS ESD protection diode array in two and four channel configurations respectively, for Ethernet and USB surge protection up to 12A (8/20µs). The ESDS302, ESDS304 devices are rated to dissipate ESD strikes up to 30kV per the IEC 61000-4-2 international standard (> Level 4).

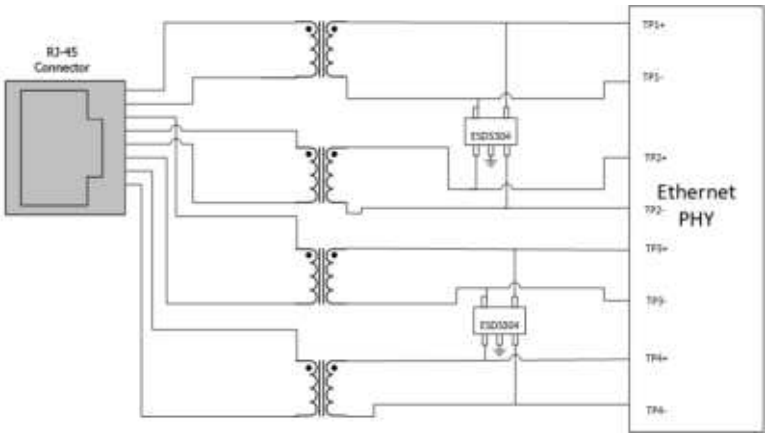
The devices features a 2.3pF IO capacitance per channel making it an excellent choice for protecting high-speed interfaces such as Ethernet™ 1G and USB 2.0. The low dynamic resistance and low clamping voltage provides system level protection against transient events.

The ESDS302, ESDS304 devices are offered in the industry standard 5-pin SOT23 packages.

Device Information

PART NUMBER(1)	CHANNEL COUNT	PACKAGE
ESDS302	2	DBV (SOT23, 5); 2 NC pins
ESDS304	4	DBV (SOT23, 5)

(1) For more information, see Section 10



Typical Application Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

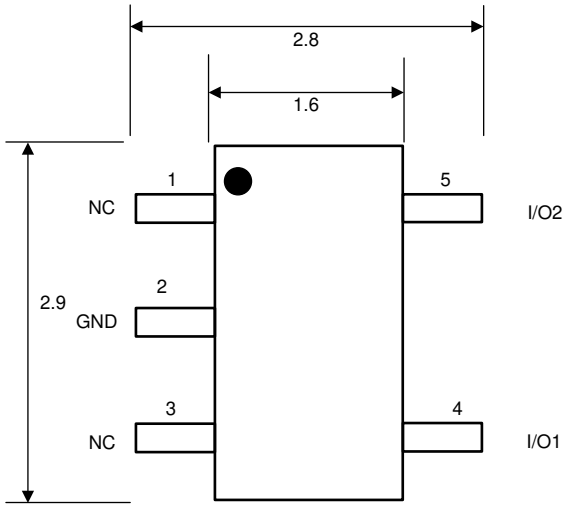


Figure 4-1. ESDS302 DBV Package, 5-Pin SOT23 (Top View)

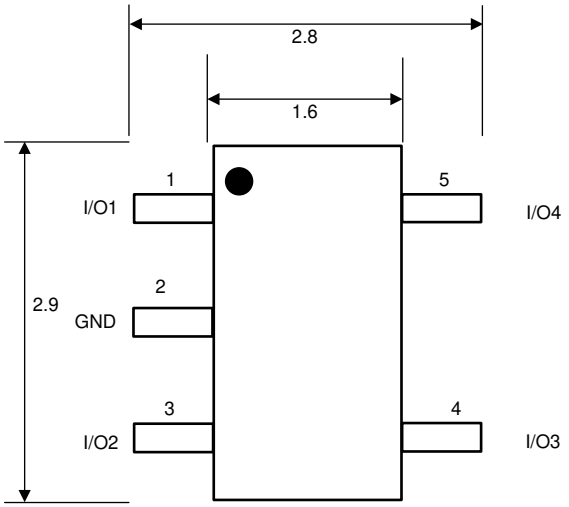


Figure 4-2. ESDS304 DBV Package, 5-Pin SOT23 (Top View)

Table 4-1. Pin Functions for ESDS302

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
I/O1	4	I/O	Surge/ESD protected channels. Connect to the lines being protected.
I/O2	5		
GND	2	GND	Ground. Connect to ground
NC	1	NC	Not connected; Used for optional straight-through routing. Can be left floating or grounded
NC	3		

(1) I = input, O = output GND = ground

Table 4-2. Pin Functions for ESDS304

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
I/O1	1	I/O	Surge/ESD protected channels. Connect to the lines being protected.
I/O2	3		
I/O3	4		
I/O4	5		
GND	2	GND	Ground. Connect to ground

(1) I = input, O = output GND = ground

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
IEC 61000-4-4 Electrical Fast Transient	Peak Power at 25 °C		80	A
IEC 61000-4-5 Surge (t_p 8/20µs)	Peak Power at 25 °C		85	W
	Peak Current at 25 °C		12	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings - JEDEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air Discharge, all pins	±30000	

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0		3.6	V
T_A	Operating Free Air Temperature	–40		125	°C

5.5 Thermal Information

THERMAL METRIC(1)		ESDS302 DBV (SOT-23) 5 PINS	ESDS304 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	176.2	133.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	125.7	85.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	88.4	49.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	71.4	30.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	88.2	49.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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5.6 Electrical Characteristics

At TA = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 500nA, across operating temperature range			3.6	V
$I_{LEAKAGE}$	Leakage current at 3.6V	V_{IO} = 3.6V, Any IO pin to GND		3	50	nA
V_{BRF}	Breakdown voltage, Any IO pin to GND (1)	I_{IO} = 1mA	4.5		7.5	V
V_{FWD}	Diode forward voltage, GND to IO pin	I_{IO} = 1mA		0.8		V
V_{HOLD}	Holding voltage, Any IO pin to GND (2)	I_{IO} = 1mA		5		V
V_{CLAMP}	Surge Clamping voltage, t_p = 8/20µs	I_{PP} = 1 A, Any IO pin to GND		5.1		V
		I_{PP} = 12A, Any IO pin to GND		6		V
		I_{PP} = 1 A, GND to any IO pin		1.2		V
		I_{PP} = 12A, GND to any IO pin		3		V
	TLP Clamping Voltage, t_p = 100ns	I_{PP} = 16A, any IO to GND pin		5.8		V
		I_{PP} = 16A, GND to any IO pin		3.1		V
C_{LINE}	Line capacitance, any IO to GND	V_{IO} = 0V, V_{p-p} = 30mV, f = 1MHz		2.3	2.8	pF
ΔC_{LINE}	Variation of line capacitance	C_{LINE1} - $C_{LINE2,}$ V_{IO} = 0V, Vp-p = 30mV, f = 1MHz		0.05	0.1	pF
C_{CROSS}	Line-to-line capacitance	V_{IO} = 0V, V_{rms} = 30mV, f = 1MHz		1.25	1.5	pF

(1) V_{BRF} is defined as the max voltage obtained at 1mA when sweeping the voltage up, before the device latches into the snapback state
(2) V_{HOLD} is defined as the voltage when 1mA is applied, after the device has successfully latched into the snapback state.

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5.7 Typical Characteristics

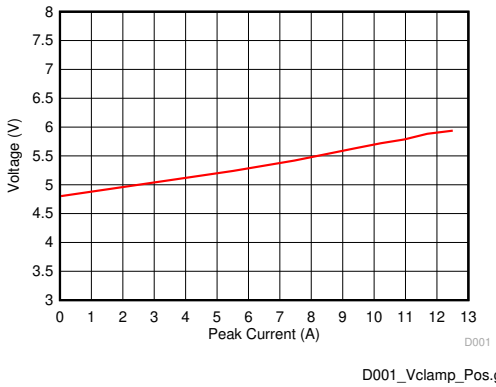


Figure 5-1. Surge Clamping Voltage vs. Peak Pulse Current (IEC 61000-4-5, tp = 8/20µs), Any IO Pin to GND

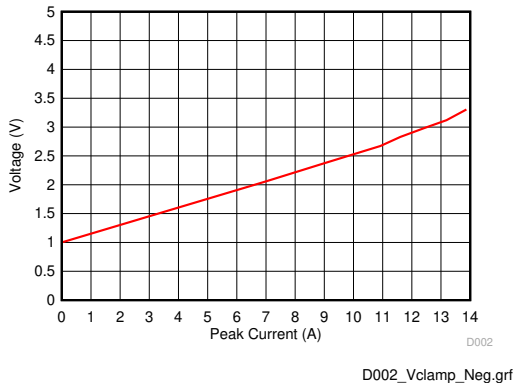


Figure 5-2. Surge Clamping Voltage vs. Peak Pulse Current (IEC 61000-4-5, tp = 8/20µs), GND to IO Pin

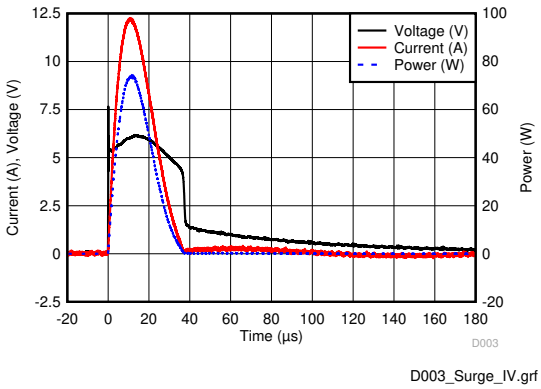


Figure 5-3. Surge Current, Clamping Voltage and Power Waveform (IEC-61000-4-5, t_p = 8/20µs), Any IO Pin to GND

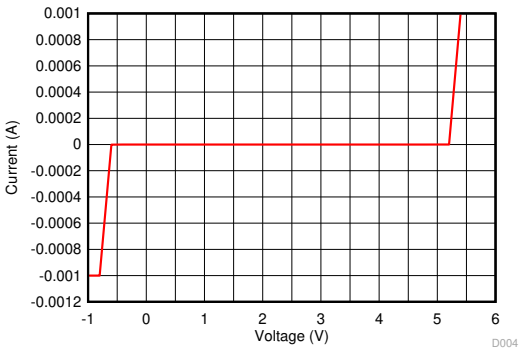


Figure 5-4. DC I-V Curve

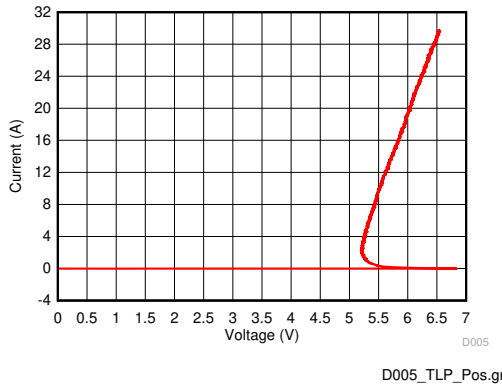


Figure 5-5. TLP I-V Curve, IO to GND, t_p = 100ns

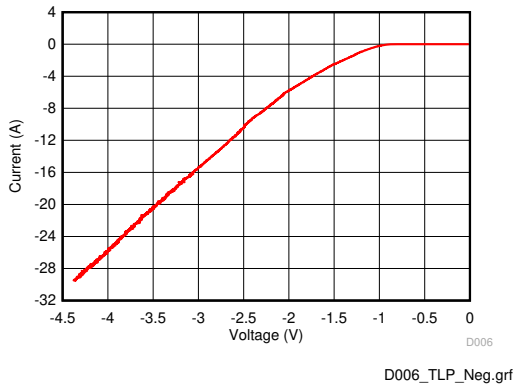


Figure 5-6. TLP I-V Curve, IO to GND Negative, t_p = 100ns

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5.7 Typical Characteristics (continued)

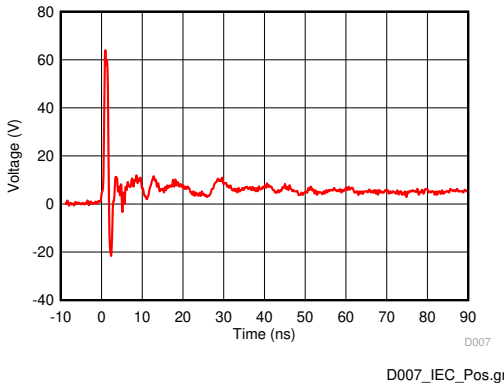


Figure 5-7. +8kV IEC 61000-4-2 Clamping Voltage Waveform, IO Pin to GND

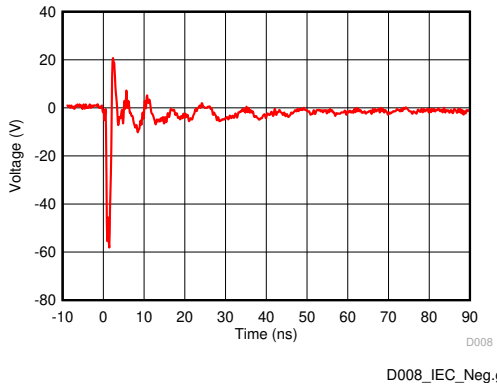


Figure 5-8. -8kV IEC 61000-4-2 Clamping Voltage Waveform, IO Pin to GND

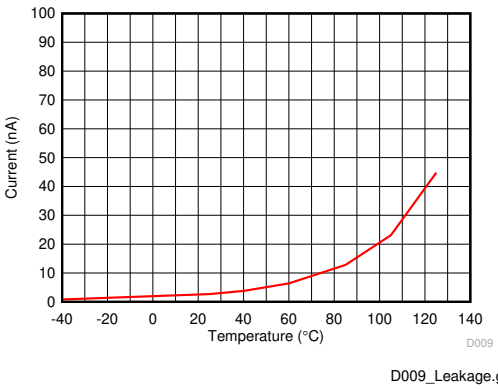


Figure 5-9. DC Leakage Current vs. Ambient Temperature, Bias Voltage = 3.6V

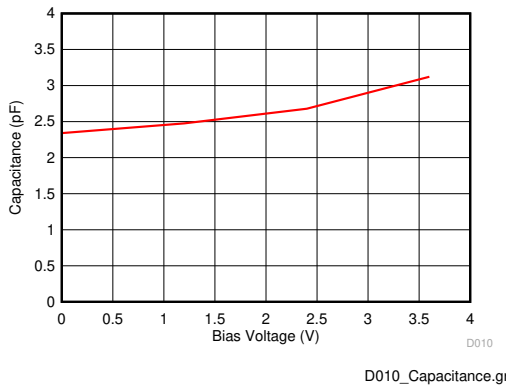


Figure 5-10. Capacitance vs. Bias Voltage at 25°C

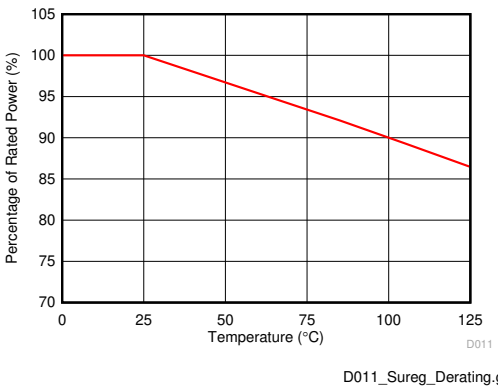


Figure 5-11. Surge Power Derating with Respect to Ambient Temperature

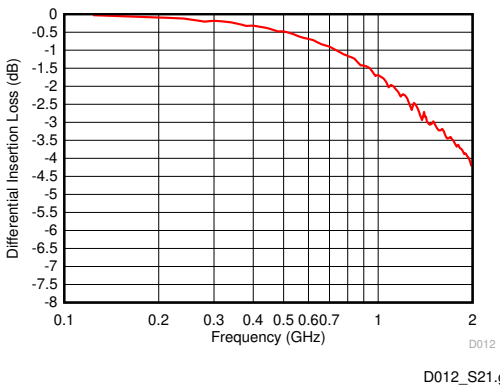


Figure 5-12. Differential Insertion Loss vs. Frequency

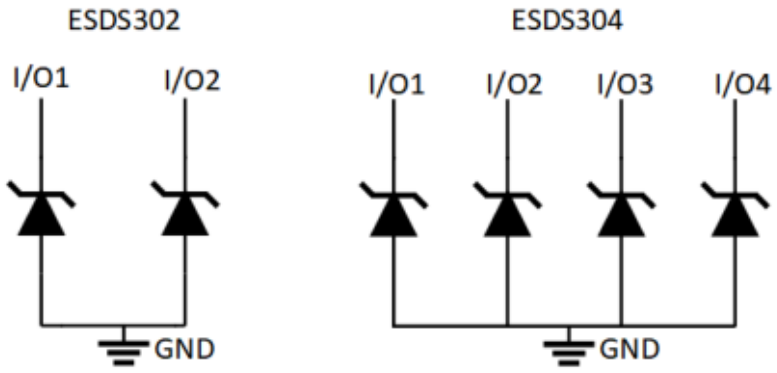
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6 Detailed Description

6.1 Overview

The ESDS304, ESDS302 devices are uni-directional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low capacitance makes this device an excellent choice for protecting any super high-speed signal pins.

6.2 Functional Block Diagram



6.3 Feature Description

The I/O pins of ESDS304 and ESDS302 can withstand surge events (IEC 61000-4-5, 8/20µs waveform) up to 12A and 85 W. These devices also provide ESD protection up to ±30kV contact and ±30kV air gap per IEC 61000-4-2 standard. The I/O pins can withstand an electrical fast transient burst of up to 80 A (IEC 61000-4-4 5/50ns waveform, 4kV with 50Ω impedance). The capacitance between each I/O pin to ground is 2.3pF (typical) and 2.8pF (maximum). This device supports data rates up to 1-Gbps. The reverse DC breakdown voltage of each I/O pin is a minimum of 4.5V. This design protects sensitive equipment from surges above the reverse standoff voltage of 3.6V. The I/O pins feature an ultra-low leakage current of 50nA (maximum) with a bias of 3.6V. This device features an industrial operating range of –40°C to +125°C.

6.4 Device Functional Modes

The ESDS304, ESDS302 devices are a passive integrated circuit that triggers when voltages are above V_{BRF} or below 0.7V. During ESD events, voltages as high as ±30kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of ESDS304, ESDS302 (usually within a few nano-seconds) the devices reverts to passive.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The ESDS304, ESDS302 devices are diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

7.2 Typical Application

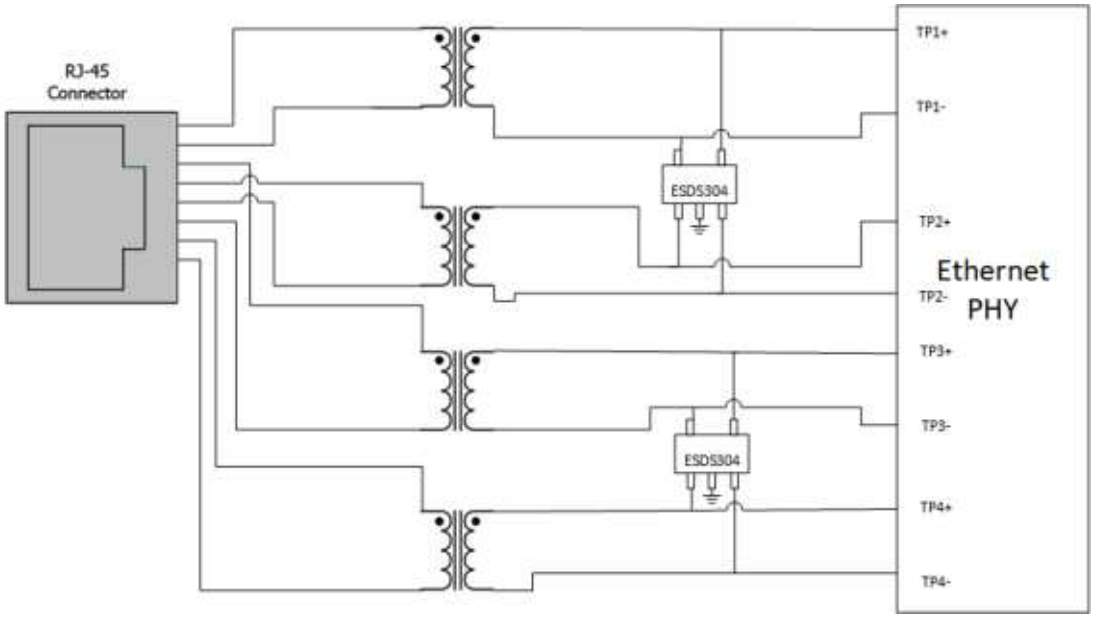


Figure 7-1. ESDS304 Protecting the Ethernet 1G Interface

7.2.1 Design Requirements

A typical operation for the ESDS304 would be protecting a high speed dataline similar to one shown in Figure 7-1. In this example, the ESDS304 is protecting an Ethernet PHY's data lines that has a nominal operating voltage of 3.6V. Many of the Ethernet interfaces that connect to long cables require protection against ±1kV surge test through a 42Ω coupling resistor and a 0.5µF capacitor, equaling roughly 24 A of surge current. Without any input protection, if a surge event is caused by lightning, coupling, ringing, or any other fault condition, this input voltage will rise to hundreds of volts for multiple microseconds, harming the device. For Ethernet 1000Base-T (1Gbps), application design parameters listed in Table 7-1 are known.

Table 7-1. Design Parameters

DESIGN PARAMETER	VALUE
Single ended signal voltage range on differential data line pairs	0 to 3.6V
Operating Frequency	125MHz

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7.2.2 Detailed Design Procedure

7.2.2.1 Signal Range

The ESDS304 has 4 identical surge protection channels with each channel supporting a signal range of 0 to 3.6V. The device will work well with any Ethernet PHY that drives the single ended voltage on the data line up to a 3.6V.

7.2.2.2 Operating Frequency

The ESDS304 has a capacitance of 2.3pF (typical) and can support the 125MHz operation of Ethernet 1000Base-T application

7.2.3 Application Curves

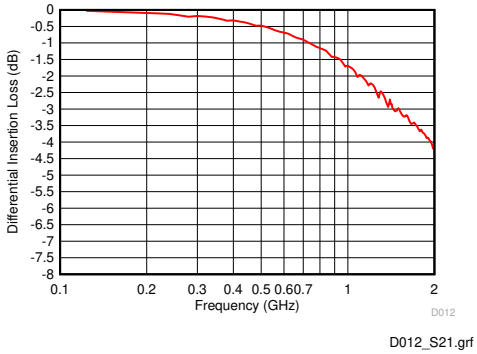


Figure 7-2. Differential Insertion Loss vs. Frequency

7.3 Power Supply Recommendations

The ESDS304, ESDS302 devices are passive ESD devices and there is no need to power them. Take care to not violate the recommended I/O specification (0V to 3.6V) so that the device functions properly.

7.4 Layout

7.4.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

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7.4.2 Layout Examples

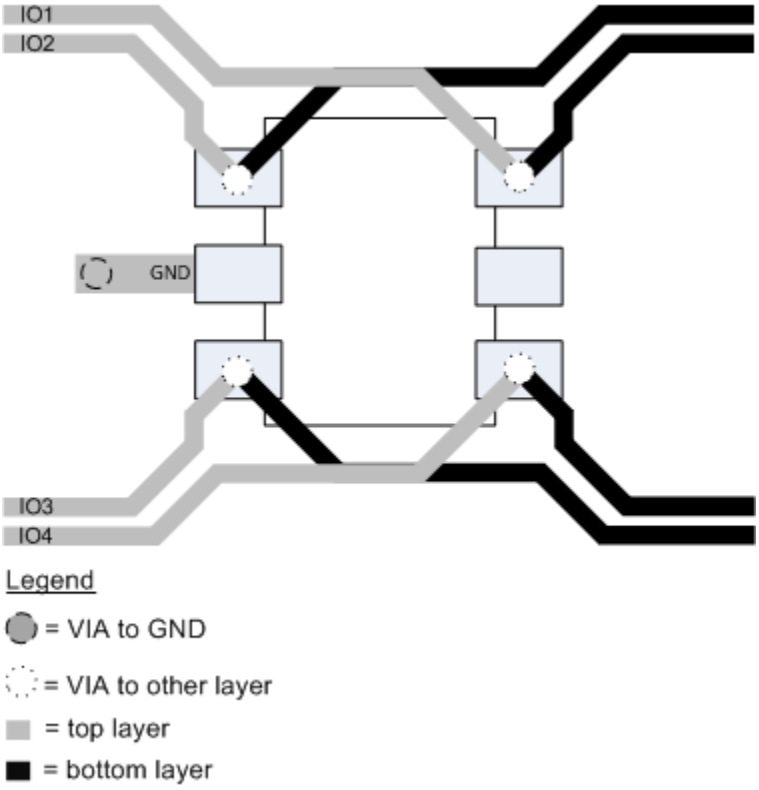


Figure 7-3. Layout Example for the 4-channel Device, ESDS304

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

Ethernet™ is a trademark of Xerox Corporation.
TI E2E™ is a trademark of Texas Instruments.
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8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2018) to Revision B (January 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated the format of the *Device Information* table to channel count	1
• Updated the table notes in the *ESD Ratings - JEDEC Specifications*	4

Changes from Revision * (May 2018) to Revision A (September 2018)	Page
• Changed data sheet status from Product Preview to Production Data	1
• Changed ESDS03802 and ESDS03804 part numbers to ESDS302 and ESDS304	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESDS302DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1R5B
ESDS304DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1R3B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

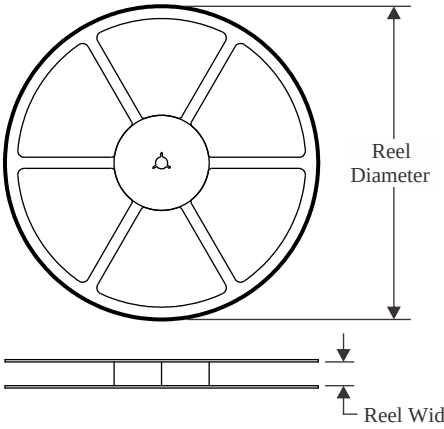
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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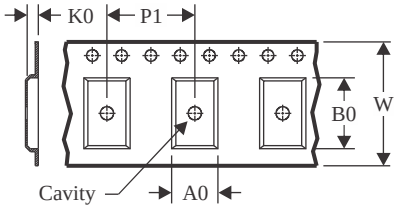
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

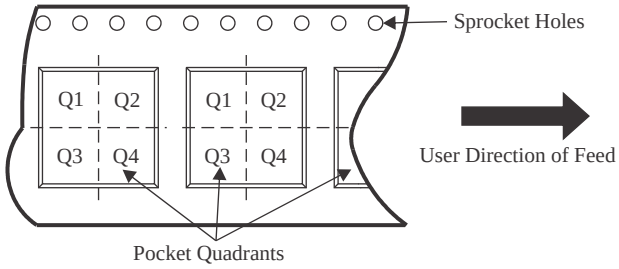


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

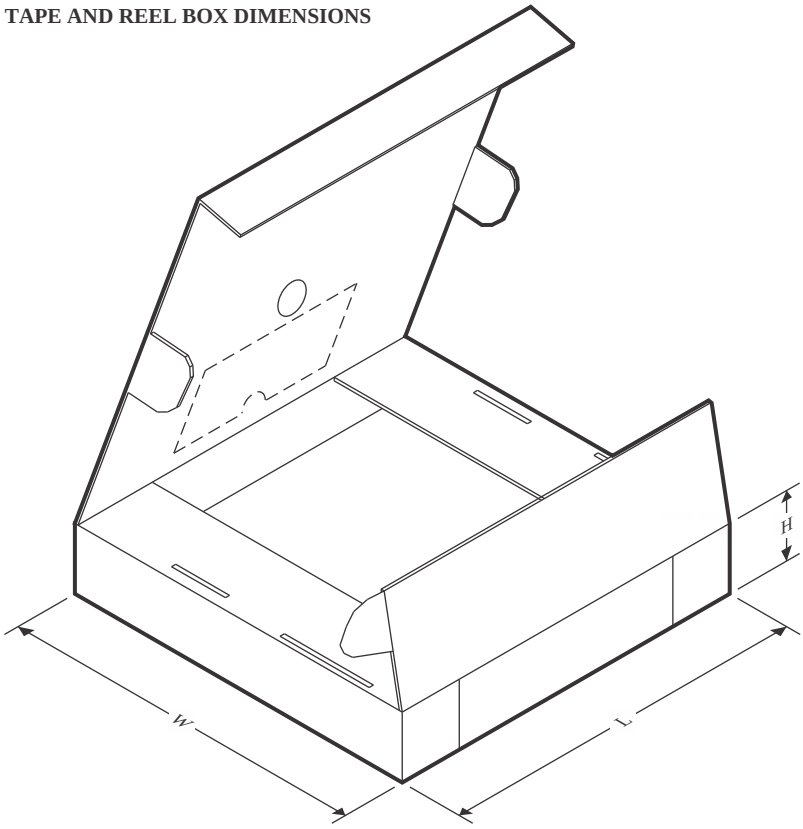
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESDS302DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
ESDS304DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

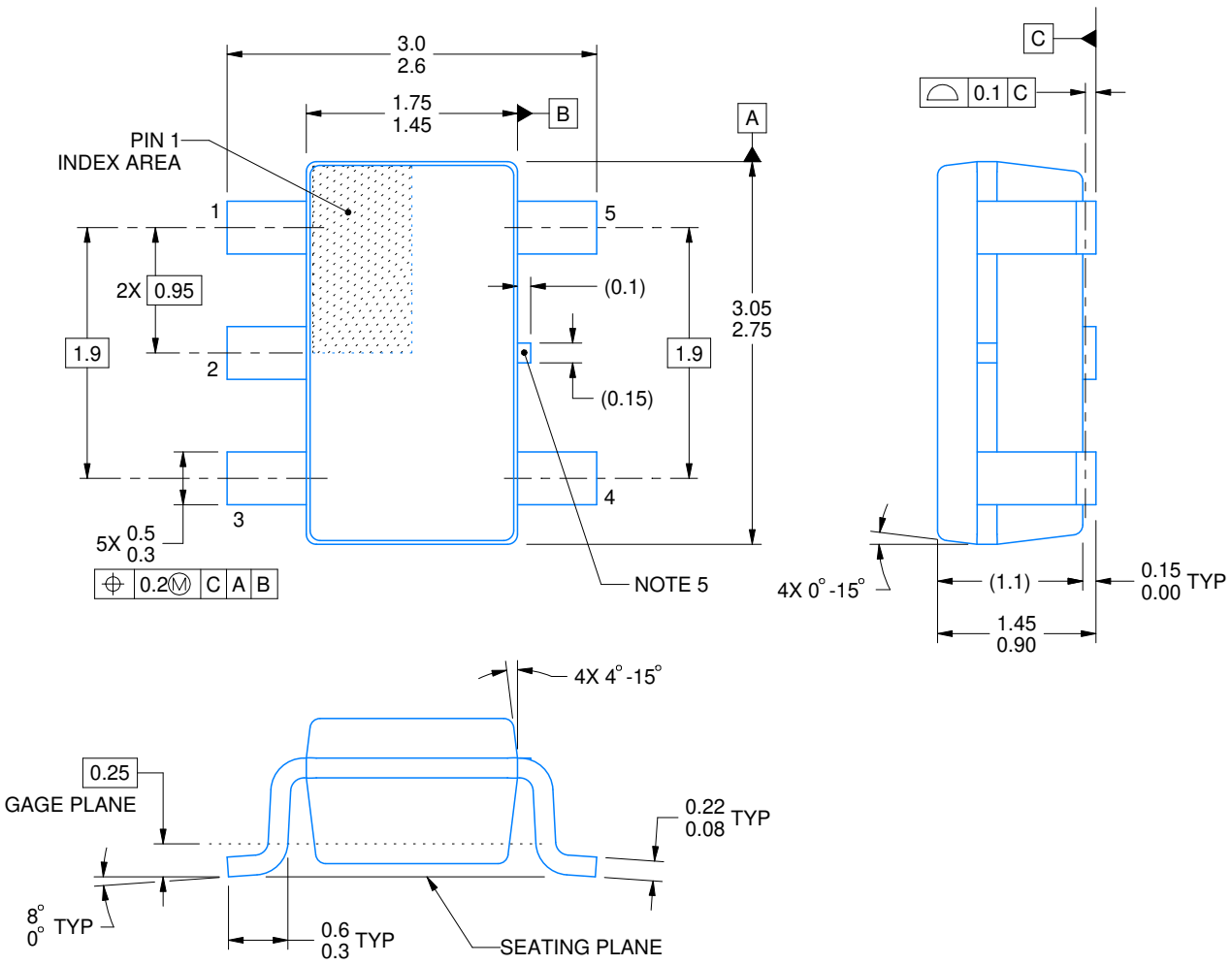
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESDS302DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
ESDS304DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

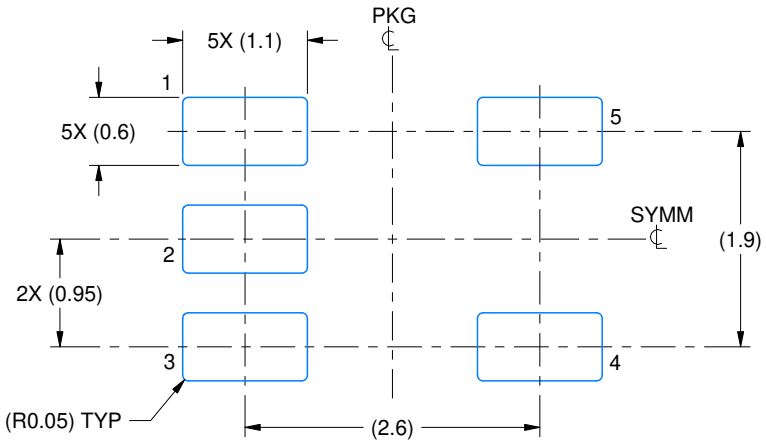
SMALL OUTLINE TRANSISTOR



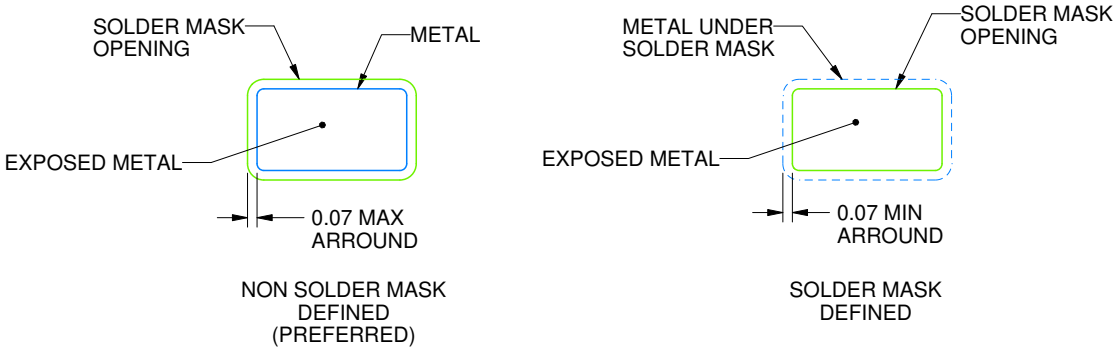
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

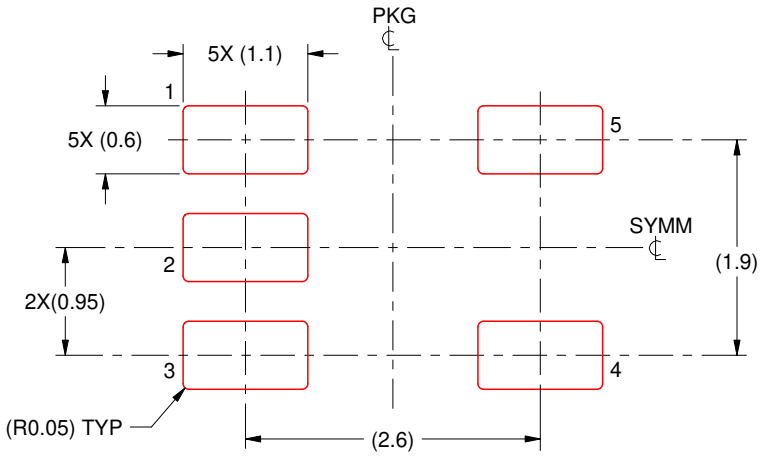


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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