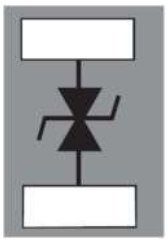
ESDU401-1BF4

Datasheet

40 V single line ESD protection with ultra-low capacitance



0201 package



Product status link
ESDU401-1BF4

Features

- Ultra Low capacitance : 1 pF
- Bidirectional device
- High working voltage : 40 V
- Low leakage current : 50 nA max.
- 0201 package size compatible
- Ultra small PCB area: 0.18 mm^2
- Low clamping voltage: 105 V at 16 A I_{pp} TLP
- Halogen free and RoHS compliant component
- Exceeds IEC 61000-4-2 level 4 standard:
  - ±16 kV (air discharge)
  - ±9.5 kV (contact discharge)

Application

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phones and accessories
- Tablets and notebooks
- Portable multimedia devices and accessories
- Wearable, home automation, healthcare
- Highly integrated systems

Description

The ESDU401-1BF4 is high voltage, ultra low capacitance bidirectional single line TVS diode designed to protect the data line or other I/O ports against ESD transients.

The device is ideal for all applications where both reduced line capacitance and board space saving are required.

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{pp}	Peak pulse voltage	IEC 61000-4-2 contact discharge IEC 61000-4-2 air discharge	±9.5 ±16	kV
P_{pp}	Peak pulse power (8/20 µs)		40	W
I_{pp}	Peak pulse current (8/20 µs)		0.7	A
T_j	Operating junction temperature range		-55 to +150	°C
T_{stg}	Storage junction temperature range		-65 to +150	
T_L	Maximum lead temperature for soldering during 10 s		260	

Figure 1. Electrical characteristics (definitions)

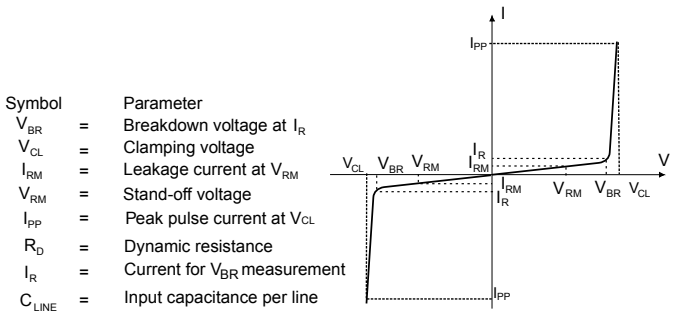


Table 2. Electrical characteristics (values) (T_{amb} = 25° C)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA		41	44	46	V
I_{RM}	Leakage current	V_{RM} = 40 V			50	nA
V_{CL}	Clamping voltage	IEC 61000-4-2, 8 kV contact discharge measured after 30 ns		105		V
V_{CL}	Clamping voltage	8/20 µs waveform, I_{PP} = 0.7 A		50		V
R_D	Dynamic resistance	Pulse duration 100 ns		3.5		Ω
C_{LINE}	Line capacitance	V_{LINE} = 40 V, F = 1 MHz, V_{OSC} = 30 mV		1.1	1.3	pF

1.1 Characteristics (curves)

Figure 2. Leakage current versus junction temperature (typical values)

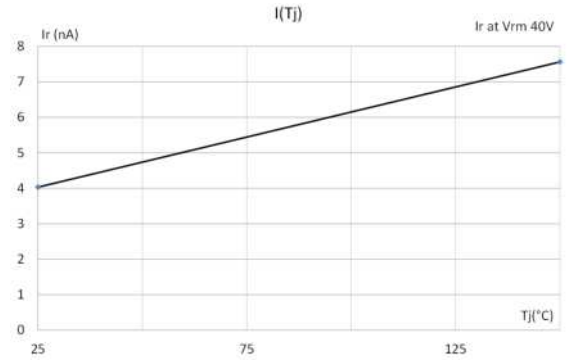


Figure 3. Junction capacitance versus applied voltage (typical values)

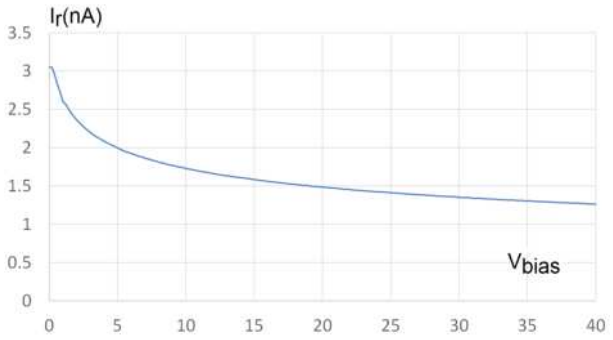


Figure 4. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

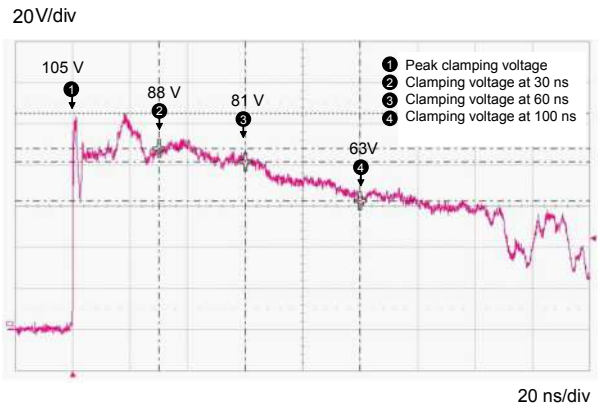


Figure 5. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

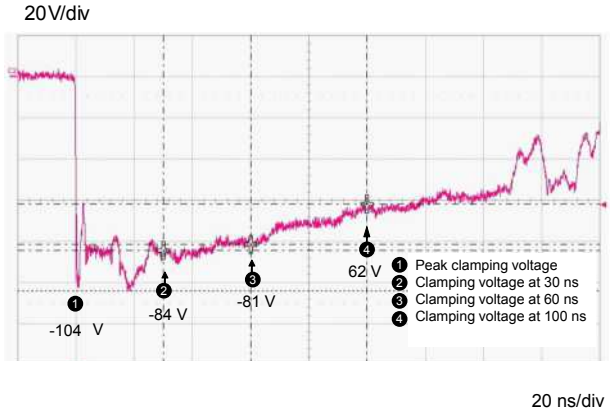
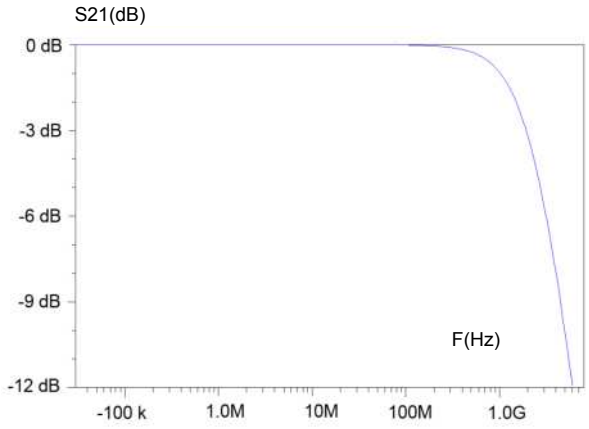


Figure 6. S21 attenuation measurement result



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 ST0201 package information

Figure 7. ST0201 package outline

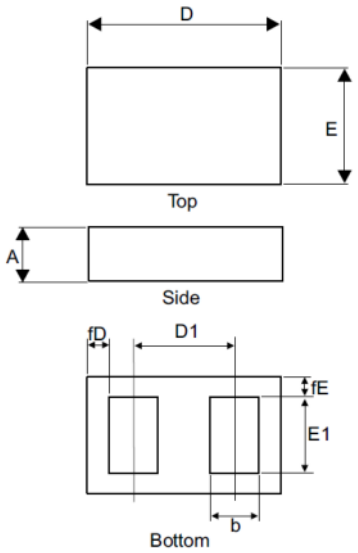
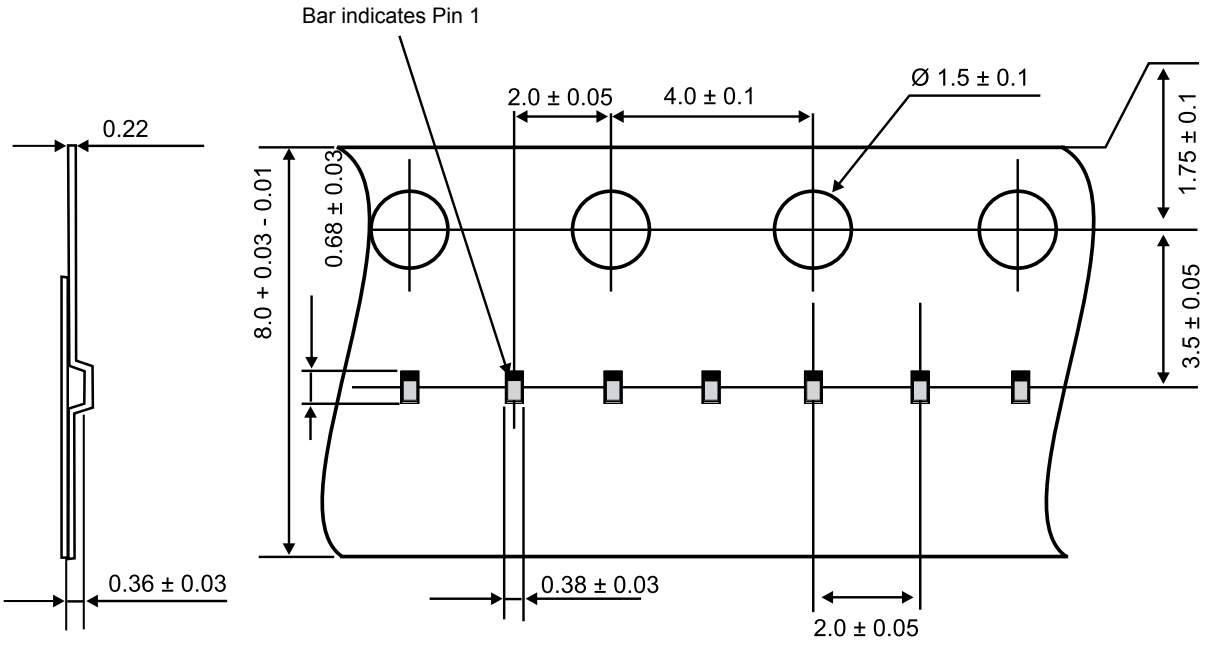


Table 3. ST0201 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.280	0.300	0.320	0.0110	0.0118	0.0126
b	0.125	0.140	0.155	0.0049	0.0055	0.0061
D	0.570	0.600	0.630	0.0224	0.0236	0.0248
D1		0.350			0.0138	
E	0.270	0.300	0.330	0.0106	0.0118	0.0130
E1	0.175	0.190	0.205	0.0069	0.0075	0.0081
fD	0.040	0.055	0.070	0.0015	0.0021	0.0028
fE	0.040	0.055	0.070	0.0115	0.0021	0.0028

Note: Marking can be rotated by 90° or 180° to differentiate assembly location.

Figure 8. Tape and reel specification

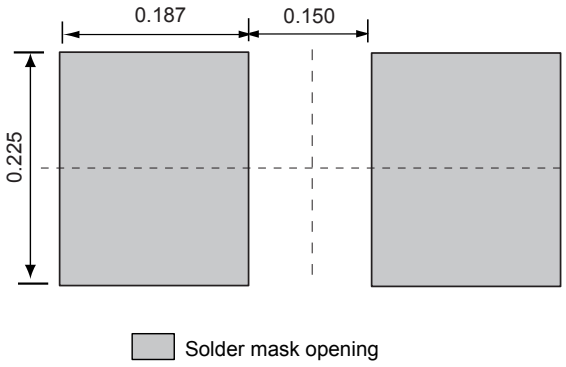


3 Recommendation on PCB assembly

3.1 Footprint

1. Footprint in mm
   a. SMD footprint design is recommended.

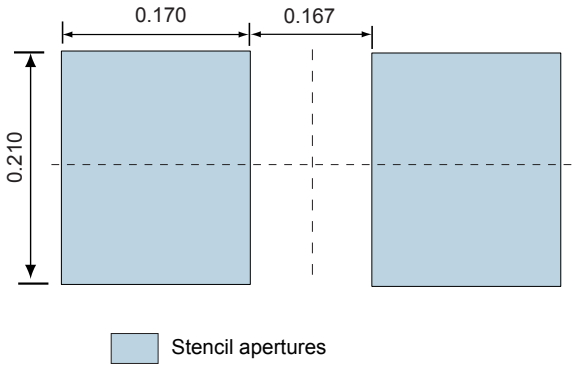
Figure 9. Footprint in mm



3.2 Stencil opening design

1. Reference design
   a. Stencil opening thickness: 75 µm / 3 mils

Figure 10. Recommended stencil window position in mm



3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-38 µm.

3.4 Placement

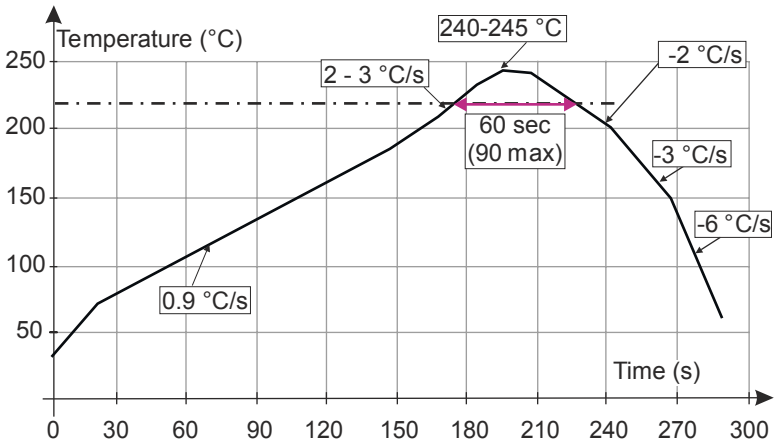
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.6 Reflow profile

Figure 11. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
ESDU401-1BF4	9(1)	ST0201	0.116 mg	15000	Tape and reel

1. *The marking can be rotated by multiples of 90° to differentiate assembly location*

Revision history

Table 5. **Document revision history**

Date	Revision	Changes
30-Sep-2019	1	First issue.

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