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May 2024

FAN41501
Ground Fault Interrupter Self-Test Digital Controller

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Features

- Meets 2015 UL943 Self-Test GFCI Requirement
- Internal 1-Second and 90-Minute Self-Test Timers
- Periodic Functional Testing for Key GFIC Components: GFCI Controller, Solenoid, Sense Transformer, and Silicon-Controlled Rectifier (SCR)
- Periodic EOL Testing without Compromising Normal GFCI Protection
- Built-in Noise Filters Reduce False EOL Signal
- Automatic EOL Reset Capability
- Easily Added to Existing GFCI Applications
- Built-in 5 V Shunt Regulator
- Energy-Saving System Solution
- Minimum External Components
- Space-Saving SuperSOT™ 6-Pin Package

Applications

- GFCI Output Receptacle
- GFCI Circuit Breakers
- Portable GFCI Cords

Description

The FAN41501 is a digital controller for periodic functional testing of key Ground Fault Circuit Interrupter (GFCI) components. In combination with an existing Fairchild GFCI controller, it periodically tests for the proper operation of the GFCI controller, solenoid, sense transformer, SCR, and other discrete components without disrupting power to the load or compromising normal GFCI protection functionality. If the FAN41501 detects a faulty GFCI component, it generates an End-of-Life (EOL) fault signal that can be used to deny power and/or automatically reset after the denial of power.

When the AC power is first applied, an internal timer starts a test cycle at one second. After this initial test cycle, the internal timer starts a test cycle every 90 minutes. During a test cycle, the FAN41501 simulates a ground fault and monitors the key GFCI components. If the FAN41501 detects a component fault, it verifies the fault several times to prevent a false EOL signal. At no time during a test cycle is the normal GFCI protection disabled or compromised.

The FAN41501 includes a 5 V shunt regulator, one-second timer, 90-minute timer, digital control logic, detection comparators, and an EOL driver output.

The FAN41501, together with a GFCI controller such as FAN4149, provides a complete UL943 GFCI function with automatic monitoring capability, low system power, and a minimum number of external components.

The 6-pin, SuperSOT™ package enables a low-cost, compact design and layout.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN41501SX	-35°C to +85°C	6-Lead, SuperSOT™, JEDEC M0-193, 1.6 mm	Tape and Reel

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Typical Application

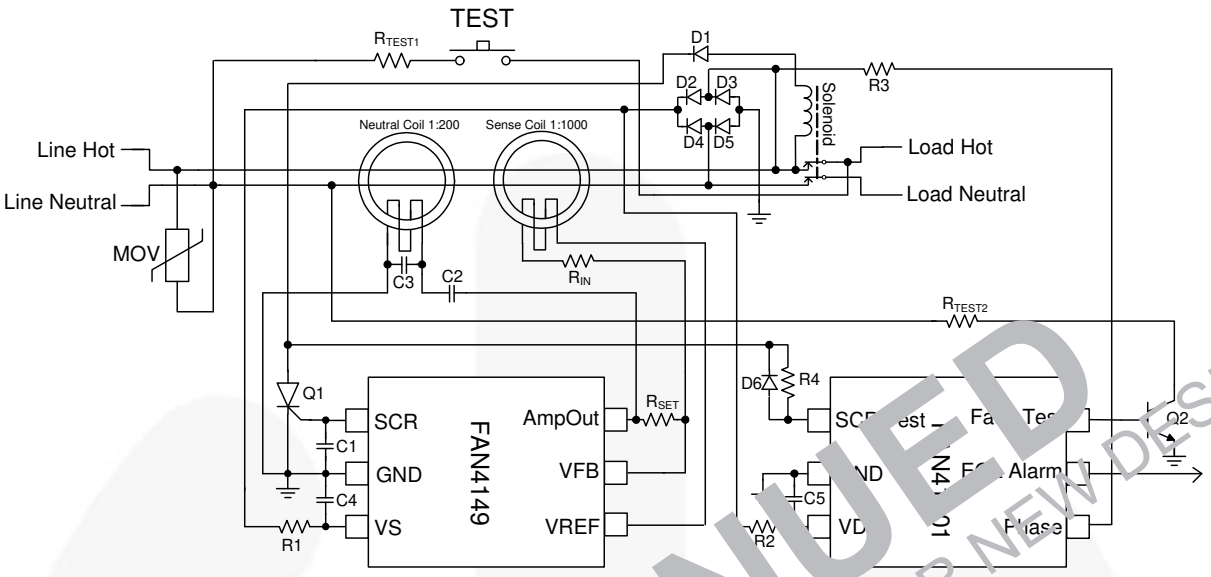


Figure 1. Typical Application

Table 1. Typical Values(3)

R1: 75 kΩ	R2: 75 kΩ	R3: 1 MΩ	R4: 909 kΩ
R_{SET}: 750 kΩ(4)	R_{IN}: 470 Ω	R_{TEST1}: 15 kΩ	R_{TEST2}: 10 kΩ
C1: 22 nF	C2: 10 nF	C3: 5.6 nF	C4: 220 nF
C5: 1 µF			

Notes:
1. Contact Fairchild Semiconductor for self-test requirement details.
2. Portions of this schematic are subject to U.S. patents 8,035,516 and 8,760,824.
3. XMFR: Magnetic Metals 50109/F3006.
4. Value depends on sense coil characteristics and application.

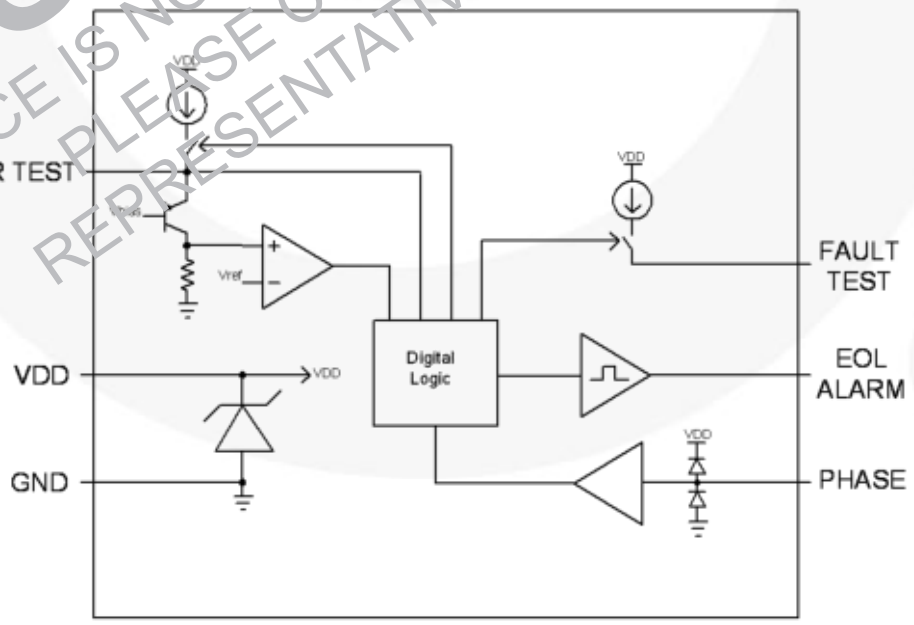


Figure 2. Block Diagram

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Pin Configuration

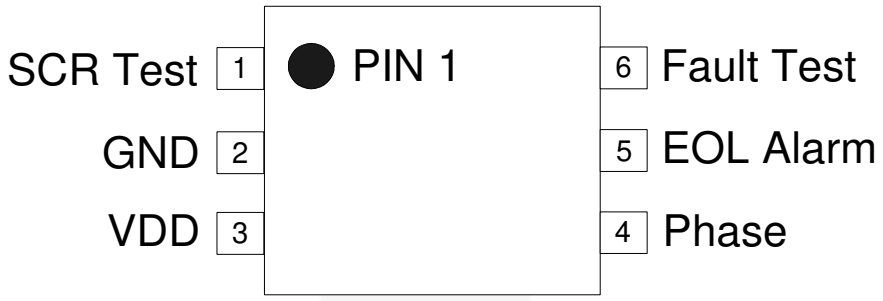


Figure 3. Pin Assignments

Pin Definitions

Pin #	Name	Description
1	SCR Test	SCR test input for SCR functionality
2	GND	Ground for FAN41501 circuitry
3	VDD	Voltage supply input for FAN41501 circuitry
4	Phase	Phase input for V_{AC} frequency
5	EOL Alarm	Alarm for end-of-life signal
6	Fault Test	Fault test output signal for ground-fault simulation

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Condition	Min.	Max.	Unit
I_{CC}	Supply Current	Continuous Current, VDD to GND		10	mA
V_{CC}	Supply Voltage	Continuous Voltage, VDD to GND	-0.8	7.0	V
		Continuous Voltage to Neutral, All Other Pins	-0.8	7.0	V
T_{STG}	Storage Temperature Range			+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, ANSI / ESDA / JEDEC JS-001-2012		2.5	kV
		Charged Device Model, JESD22-C10		1.0	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the data sheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings. Unless otherwise specified, refer to Figure 1. T_A=25°C, I_{SHUNT}=1 mA, and phase=60 Hz.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{REG}	Power Supply Shunt Regulator Voltage	VDD to GND	5.10	5.35	5.70	V
V_{UVLO_RST}	Under-Voltage Reset	VDD to GND	2.2	2.5	2.7	V
		Rising Hysteresis		150		mV
I_Q	Quiescent Current	VDD to GND= 4.5 V	350	450	550	µA
t_{FIRST}	First Timer Period	V_{DD} > 2.5 V	0.812	1.016	1.220	s
t_{PER}	Periodic Timer	Steady State	4400	5400	6400	s
t_{TOUT}	Test Cycle Time Out	Fault Testing	54	66	78	ms
t_{PHASE}	Phase Continuity Check Time Out	Phase Pin Continuity Check at Startup	40	60	80	ms
V_{PHASE_H}	Phase Voltage Clamp HIGH	I_H = 170 µA	5.8	6.3	6.6	V
V_{PHASE_L}	Phase Voltage Clamp LOW	I_L = -170 µA	-0.8	-0.6	-0.4	V
I_{PHASE_MAX}	Phase Maximum Current	I_{SHUNT} = 1.5 mA	-300		300	µA
V_{SCR_H}	SCR Test Input Clamp HIGH	I_H = 170 µA	5.0	5.4	5.8	V
V_{SCR_L}	SCR Test Input Clamp LOW	I_L = -170 µA	-0.8	-0.6	-0.4	V
I_{SCR_MAX}	SCR Test Maximum Current	I_{SHUNT} = 1.5 mA	-300		300	µA
I_{TEST}	Fault Test Current	Test Cycle	400	500		µA
V_{EOL_L}	EOL Alarm V_{OL}	No Load		0	200	mV
V_{EOL_H}	EOL Alarm V_{OH}	No Load	4.80	5.25		V
f_{EOL}	EOL Alarm	Latched Fault Output	3.00	3.75	4.25	Hz
I_{EOL}	EOL Alarm I_{OUT}	I_{SHUNT} = 2.0 mA	1			mA

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Functional Description

(Refer to Figure 1)

Starting in June 2015, UL943 will require all permanently connected GFCI products to perform a self test function. The FAN41501, together with a GFI controller device – like the FAN4149 – provides GFI fault protection and periodic self testing of the key GFCI components: solenoid, SCR, GFI controller, sense coil, and other discrete components.

The FAN41501 has an internal 5.35 V shunt regulator. With diodes D2-5 and resistor R2, the shunt regulator clamps the FAN41501 V_{DD} supply voltage to 5.35 V. Capacitor C5 provides bias during the V_{AC} zero phase crossing so the FAN41501 is continuously biased. When power is first applied, an internal Power-On-Reset (POR) circuit detects when V_{DD} is greater than 2.5 V. The POR circuit generates an internal reset pulse and initializes a one-second timer. After one second, the first self-test cycle starts. During the positive half cycle when the "line-hot" voltage is positive with respect to the "line-neutral" voltage, the SCR anode voltage is monitored by means of resistor R4 connected to pin 1 (SCR Test). The FAN41501 clamps this pin to VDD, mirrors the current through R4 to an internal low-pass filter circuit and compares its value to an internal reference threshold. When the current level exceeds the reference threshold, an internal latch is set. This test [illegible] the continuity of the solenoid and [illegible]. The threshold level is determined by:

$$Vth_{rms} = (65\ \mu A \times R[illegible] \quad (1)$$

where Vth_{rms} is the rms V_{AC} input voltage with a tolerance of ±10%.

With the recommended application values, the SCR anode voltage must exceed a worst-case peak voltage of approximately 65 V (rms). Equation (1) can be used if a lower threshold voltage value is desired to allow this test to pass during a brownout or voltage sag condition.

To test the functionality of the GFCI controller, sense coil, and SCR; a simulated ground fault condition is generated. Like the SCR Test pin, the Phase pin (pin 4) is clamped to V_{DD} + 700 mV, mirrors the current through R3 to an internal low-pass filter circuit, and compares its value to an internal reference. This internal circuit detects when the phase signal is near the end of the positive half cycle. When this occurs, an internal current source is enabled to bias the SCR Test pin. This prevents the SCR anode voltage from discharging to zero during the negative half cycle since it is reverse-biased by diode D1. At the end of the positive half cycle, the FAN41501 generates a current pulse for the Fault Test pin (pin 6). This current pulse enables transistor Q2, which biases the collector voltage of Q2 to a low voltage. During the negative half cycle when the line-neutral voltage is positive with respect to the line-hot voltage, current flows through resistor R_{TEST2} when Q2 is enabled. This current creates a simulated ground fault from line-neutral to load hot. This current is detected by the GFI controller (i.e. FAN4149) and, when it exceeds the programmed trip threshold set by R_{SET} (typically 5 mA_{rms}), the controller enables the SCR Q1 (*see FAN4149 datasheet for I_{FAULT} trip threshold equation*). The SCR quickly discharges the anode voltage, which is pre-biased by the FAN41501 control logic. The discharge of the anode voltage also biases the voltage at the SCR Test pin to a low voltage by forward-biasing diode D6. The FAN41501 monitors the SCR Test pin during this test cycle and sets a latch if the SCR is triggered. The simulated ground fault tests for the functionality of the controller, R1, D1, D2-5[5], sense coil, and SCR without opening the load contacts. The load contacts do not open during this test because D1 is reversed biased, which prevents current from energizing the solenoid. Once the FAN41501 detects the triggering of the SCR, the current pulse for Q2 is disabled and the bias current for pin SCR Test is removed. This disables the SCR so that during the next positive half cycle the solenoid is not energized. With the recommended application values, the simulated ground fault triggers the [illegible] with a V_{AC} input voltage greater than 85 V_{rms}. If a different voltage threshold is required, the R_{TEST2} resistor can be adjusted *(per the FAN4149 datasheet)*. Figure 4, Figure 5 and Figure 6 show a passing self-test cycle. The waveform of channel 4 shows when the Q2 transistor is enabled and a ground fault is simulated by the current through resistor R_{TEST2}. The channel 3 waveform shows the gate of the SCR Q1. Figure 6 shows the pre-bias for the SCR anode voltage, waveform on channel 1. Figure 6 illustrates that, when the gate of the SCR is enabled by the controller, the voltage on the SCR anode is quickly discharged. The FAN41501 detects this and a self-test cycle is completed with all of the required components passing. The Q2 bias is disabled, which causes the GFCI controller to disable the SCR gate bias.

Note:

5. Redundant diodes may be required.

If the first self-test cycle passes after power up, subsequent self-test cycles occur every 90 minutes. At no time does the FAN41501 disable the normal controller GFI protection circuitry.

If any one of the above self tests fail, the FAN41501 repeats the self testing until a 66 ms timer expires. If this occurs, the EOL latch is enabled and the FAN41501 EOL Alarm pin 5 goes HIGH. This signal can be connected to a separate SCR or to the gate of Q1 with a series diode. When the EOL Alarm goes HIGH, the SCR is enabled and energizes the solenoid, which opens the load contacts. When the EOL Alarm pin goes HIGH, if it is connected to the gate of an SCR, V_{DD} drops below 2.5 V. This generates a Power-On-Reset that resets the logic and repeats a self-test cycle in one second. Figure 7 to Figure 10 show a FAN41501 self-test cycle for a SCR, GFI controller, sense coil, and solenoid failure.

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The self test cycle lasts for 66 ms to allow four self-test cycle attempts. After the timer has expired, the EOL alarm is enabled. Figure 7 to Figure 10 show an example of the EOL alarm signal connected to the gate of an SCR. When the EOL alarm signal is enabled, the V_{DD} voltage is discharged, which causes a POR. The EOL alarm is disabled and a self-test cycle is repeated in one second.

In addition to the above GFCI tests, the FAN41501 also performs a pin 4 (Phase pin) continuity check when power is first detected. When V_{DD} exceeds 2.5 V, pin 4 is checked for an open or short. If this continuity check fails after 60 ms, the EOL alarm is enabled. Figure 11 shows an example of the Phase pin with R3 removed (floating pin). After approximately 60ms, the EOL alarm is enabled.

After a self-test cycle failure, the EOL alarm is latched HIGH for 133 ms. This signal generates a repetitive 3.75 Hz digital square wave. There are two ways to reset the EOL alarm signal. The first is POR as described above, which can occur if the AC power is cycled. Since it may be undesirable to cycle the AC power, the EOL alarm signal can also be connected to the gate of a SCR or "clamp diode" to generate a POR. If the EOL alarm signal is diode clamped when the EOL alarm signal goes HIGH, a high I_{OH} current is generated. This current is dependent on R2 and C5, however, if the datasheet values are used, the typical I_{OH} current can be greater than 5 mA. This high current can be used to "latch on" a SCR and cause V_{DD} to drop below 2.5 V, which generates a POR. Figure 11 shows the V_{DD} signal when the EOL alarm signal is connected to the gate of a SCR with a series diode. The high EOL alarm I_{OH} current causes V_{DD} to drop below 2.5 V during the V_{AC} zero crossing.

Another way to reset the EOL alarm signal is to detect a successful manual test cycle. If the FAN41501 is latched in an EOL state and detects a "manual test" (i.e., the TEST button is pressed) the FAN41501 disables the EOL alarm and perform sa self-test cycle in one second. If an EOL alarm state has occurred due to a pin 4 continuity check failure, the "manual test" reset option is disabled.

Referring to Figure 1, the EOL alarm signal must be used to open the load contacts (power denial) if a self-test cycle fails for the tested components (with the exception for a solenoid or SCR open failure). As described above, this can be done with a redundant SCR or by connecting the EOL alarm signal to Q1 via a series diode. If Q1 is used to open the load contacts, a gate resistor must be added from the GFCI controller gate drive pin to the gate of the SCR. If Q1 or the solenoid fails due to an open circuit, a visual EOL signal can be generated instead of power denial. This can be accomplished by making the series diode from the EOL Alarm pin to the gate of Q1 a LED diode. This diode flashes every second. Additionally, an LED diode can be added in series with R_{TEST2} and the collector of Q2. This LED diode can be used to provide a self-test signal at power up and then every 90 minutes. If the self-test cycle fails, it flashes every second.

In summary, the FAN41501 can be added to an existing UL943 circuit to comply with the 2015 UL self-test requirement. The small package size and the minimum required components allow for a compact, low-cost, GFCI self-test solution.

Contact a Fairchild Semiconductor representative for details about how to test the FAN41501 self-test features in production or for details about the 2015 UL943 self-test application requirements.

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Typical Performance Characteristics

Pass testing of all key components. Refer to evaluation board *(see www.fairchildsemi.com for details)*.

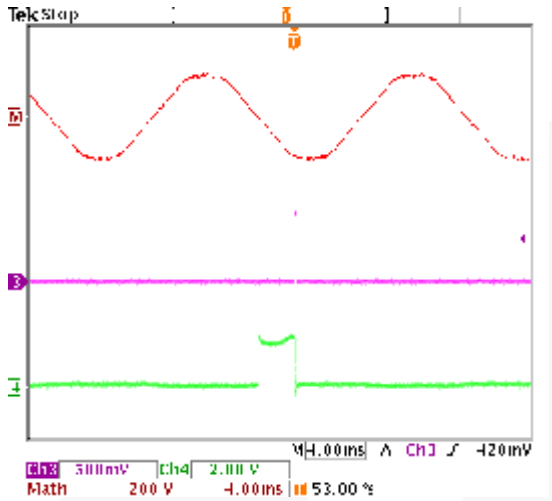


Figure 4. Pass GFCI, Sense Coil, Solenoid, SCR Tests; Ch Math: V_{AC} Input 200 V/Div, Ch3: SCR Gate, Ch4: Fault Test (Pin 6)[6]

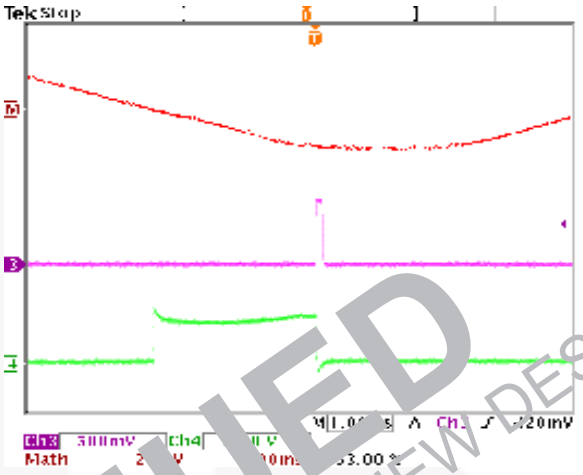


Figure 5. Pass Simulated Ground Fault Test; Math: V_{AC} Input 200 V/Div, Ch3: SCR Gate, Ch4: Fault Test (Pin 6)

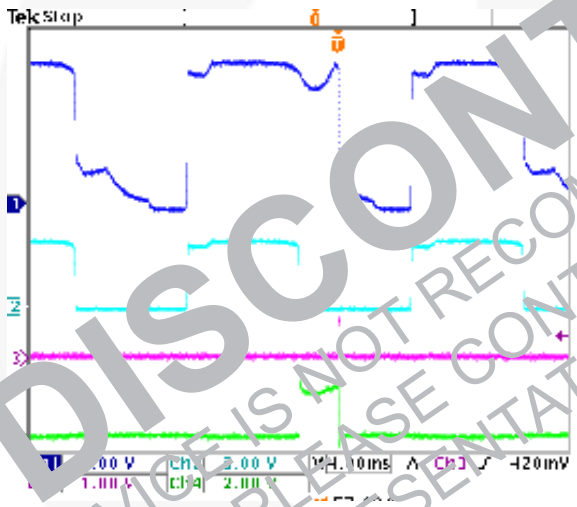


Figure 6. Pass Simulated Ground Fault Test; Ch1: SCR Test (Pin 1), Ch2: Phase (Pin 4), Ch3: SCR Gate, Ch4: Fault Test (Pin 6)[7]

Notes:

6. Anode voltage is tested during the positive half cycle (internal latch set when V_{AC} > 85 V_{rms}).
7. During the simulated ground fault test, the SCR discharges the pre-biased SCR Test pin.

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Ground Fault Tests

SCR, GFI, sense coil, and solenoid failures.

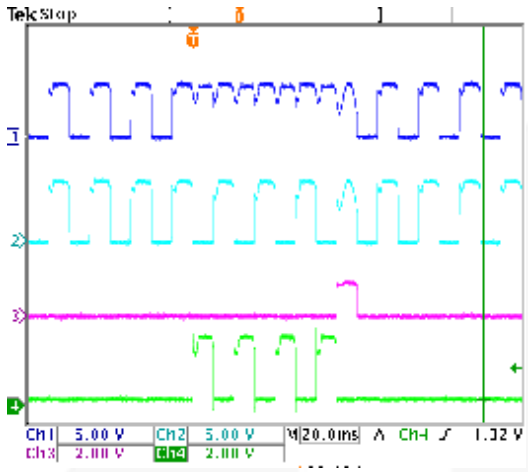


Figure 7. SCR Test Ch1: SCR Test (Pin 1), Ch 2: Phase (Pin 4), Ch 3: EOL Alarm (Pin 5), Ch 4: Fault Test (Pin 6)[8]

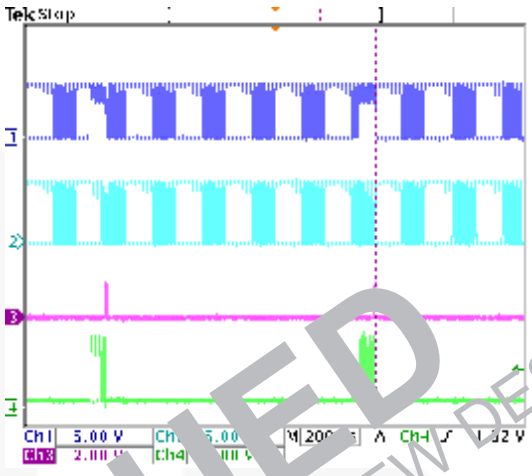


Figure 8. SCR Test Ch1: SCR Test (Pin 1); Ch2: Phase (Pin 4); Ch3: EOL Alarm (Pin 5), Ch4: Fault Test (Pin 6)[9]

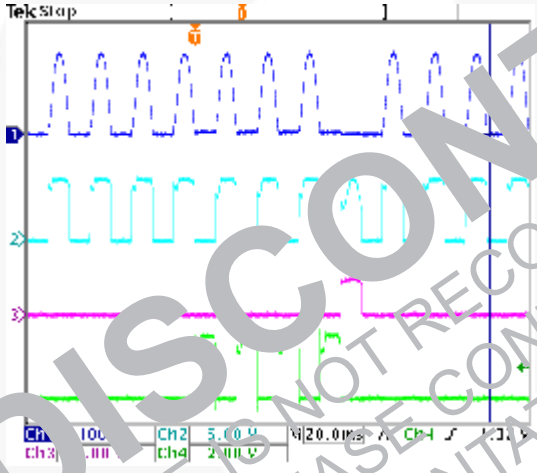


Figure 9. GFI / Sense Coil Tests Ch1: SCR Anode (100 V/div), Ch2: Phase (Pin 4), Ch3: EOL Alarm (Pin 5), Ch4: Fault Test (Pin 6)[10]

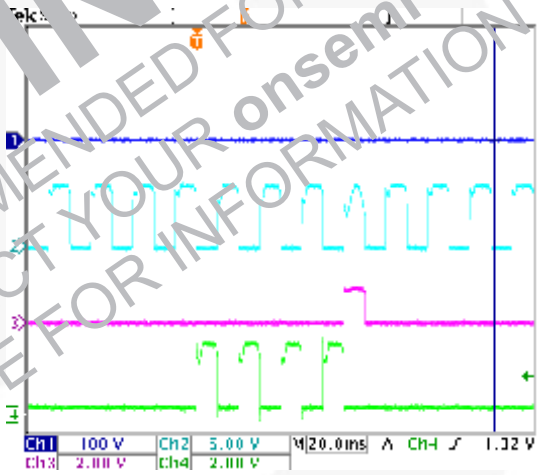


Figure 10. Solenoid Test Ch1: SCR Anode (100 V/Div), Ch2: Phase (Pin 4), Ch3: EOL Alarm (Pin 5), Ch4: Fault Test (Pin 6)[11]

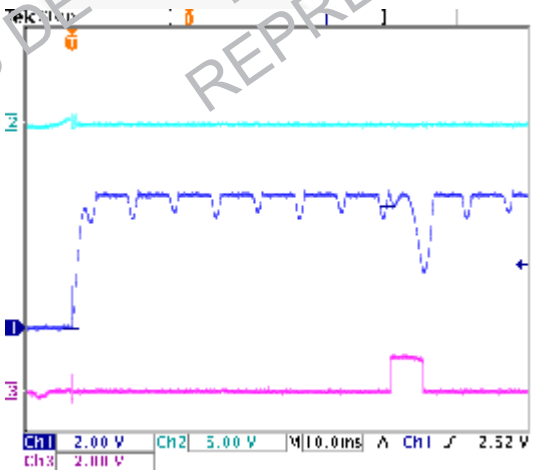


Figure 11. Phase Pin, Continuity Test; Ch1: VDD (Pin 3), Ch2: Phase (Pin 4), Ch3: EOL Alarm (Pin 5)[12,13]

Notes:

8. This test is with the SCR disabled. The EOL alarm signal is enabled after “time out” 66 ms timer has expired. The EOL alarm signal is connected to the gate of a SCR.
9. This test is the same as Figure 7, except for the time scale. After a self-test failure, an EOL alarm pulse is generated every one second.
10. This test is with the FAN4149 GFI controller disabled.
11. This test is with the solenoid open.
12. This test is with the Phase pin open.
13. If no signal is detected for the Phase pin within 60 ms of the POR, an EOL alarm is enabled. The SCR is enabled, which causes the V_{DD} voltage to drop and generates a POR cycle.

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Typical Temperature Characteristics

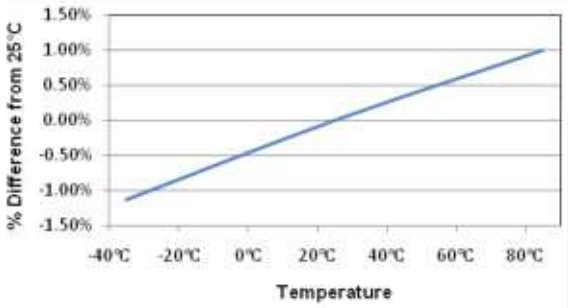


Figure 12. Shunt Regulator Voltage vs. Temperature

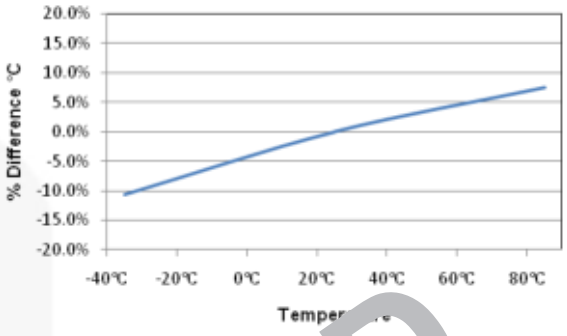


Figure 13. Quiescent Current vs. Temperature

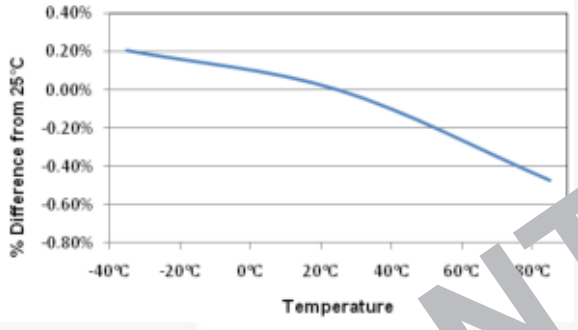


Figure 14. Under-Voltage Reset vs. Temperature

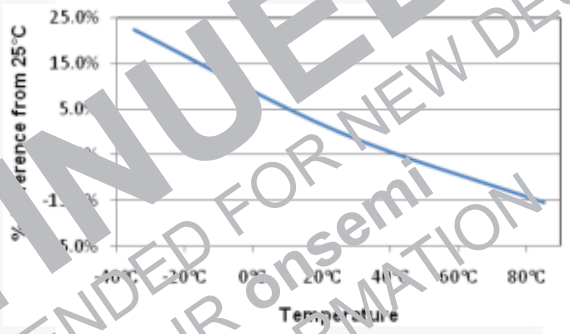


Figure 15. Phase Pin Continuity Check Time vs. Temperature

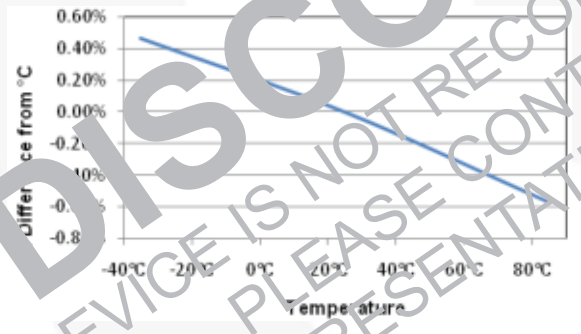


Figure 16. Phase Pin Voltage Clamp High vs. Temperature

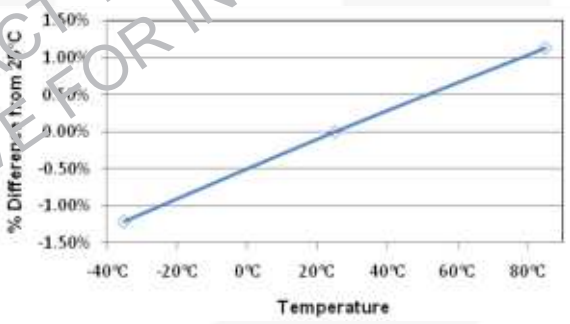


Figure 17. SCR Test Pin Voltage Clamp High vs. Temperature

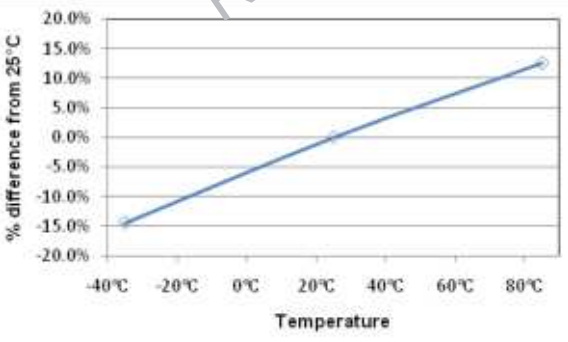


Figure 18. Fault Test Pin Current vs. Temperature

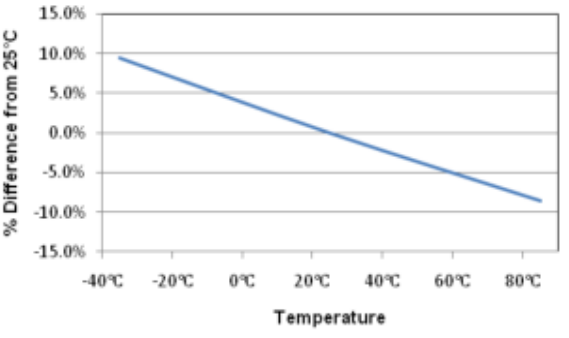


Figure 19. EOL Alarm Pin I_{OUT} vs. Temperature

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Physical Dimensions

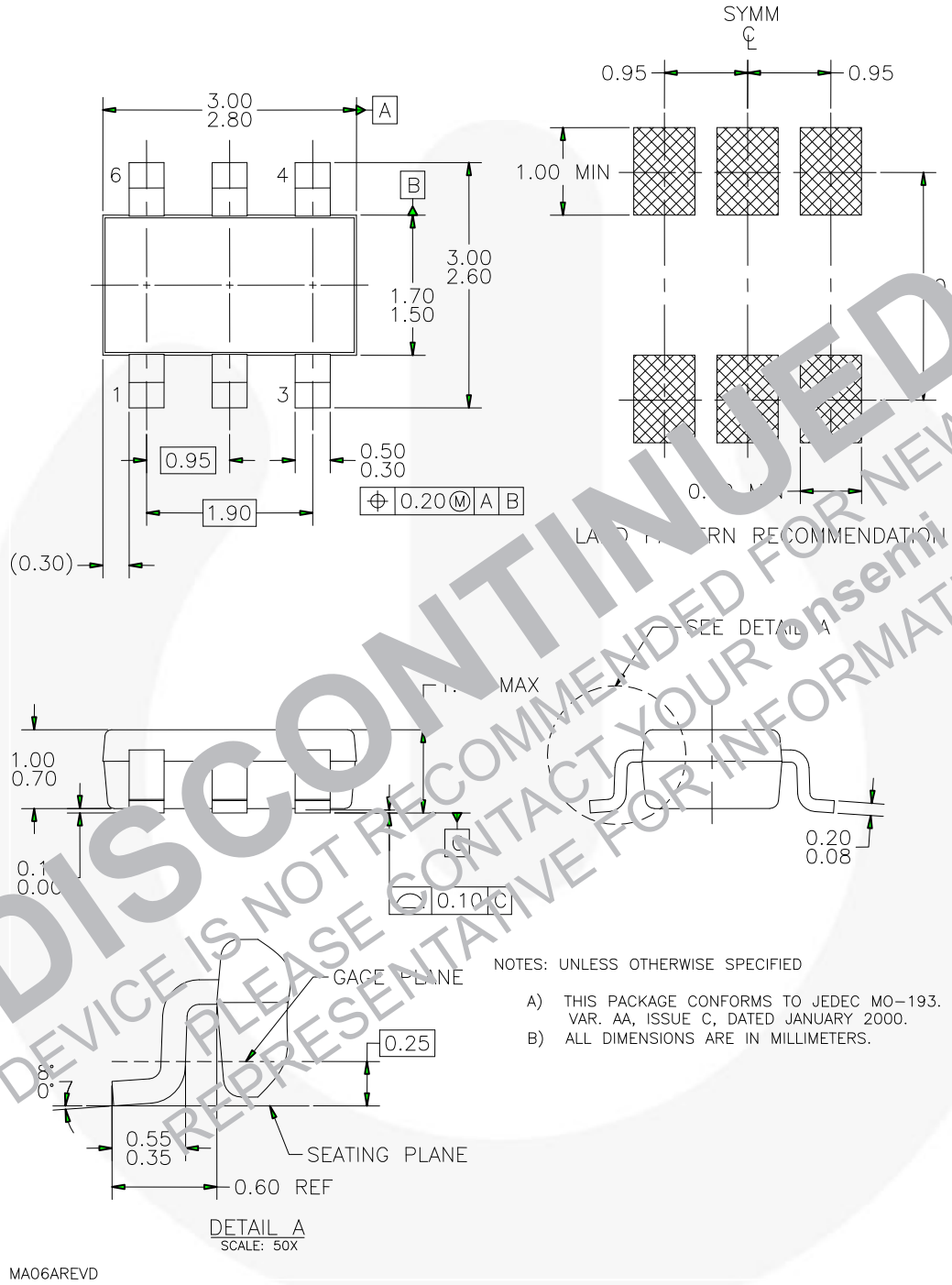


Figure 20. 6-Lead, SuperSOT™-6, JEDEC M0-193, 1.6 mm

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