Half Bridge Gate Driver

FAN7080-GF085



SOIC8
CASE 751EB

Description

The FAN7080−GF085 is a half−bridge gate drive IC with reset input and adjustable dead time control. It is designed for high voltage and high speed driving of MOSFET or IGBT, which operates up to 600 V. **onsemi**'s high−voltage process and common−mode noise cancellation technique provide stable operation in the high side driver under high−dV/dt noise circumstances. An advanced level−shift circuit allows high−side gate driver operation up to V_S = −5 V (typical) at V_{BS} = 15 V. Logic input is compatible with standard CMOS outputs. The UVLO circuits for both channels prevent from malfunction when V_{CC} and V_{BS} are lower than the specified threshold voltage. Combined pin function for dead time adjustment and reset shutdown make this IC packaged with space saving SOIC−8 Package. Minimum source and sink current capability of output driver is 250 mA and 500 mA respectively, which is suitable for junction box application and half and full bridge application in the motor drive system.

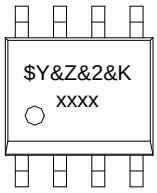
Features

- Automotive Qualified to AEC−Q100 and PPAP Capable
- Floating Channel for Bootstrap Operation to +600 V
- Tolerance to Negative Transient Voltage on VS Pin
- VS−pin dv/dt Immune
- Gate Drive Supply Range from 5.5 V to 20 V
- Under−Voltage Lockout (UVLO)
- CMOS Schmitt−triggered Inputs with Pull−down
- High Side Output In−phase with Input
- IN input is 3.3 V/5 V Logic Compatible and Available on 15 V Input
- Matched Propagation Delay for both Channels
- Dead Time Adjustable
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Junction Box
- Half and Full Bridge Application in the Motor Drive System

MARKING DIAGRAM



$Y	= **onsemi** Logo
&Z	= Assembly Plant Code
&2	= 2−Digit Date Code
&K	= Lot Run Traceability Code
xxxx	= Specific Device Code

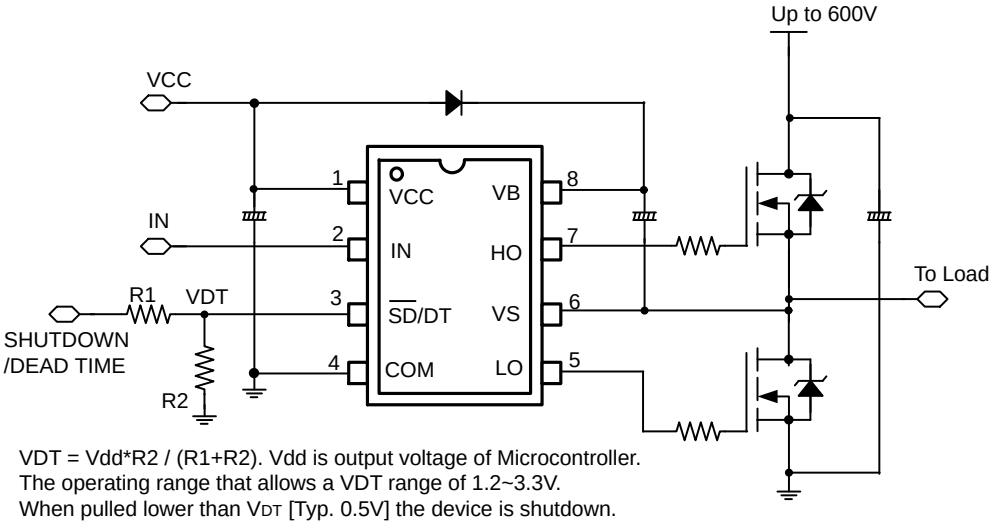
ORDERING INFORMATION

Device	Package	Shipping†
FAN7080M−GF085	SOIC8 (Pb−Free)	9500 / Tube
FAN7080MX−GF085		2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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TYPICAL APPLICATION



VDT = Vdd*R2 / (R1+R2). Vdd is output voltage of Microcontroller.
The operating range that allows a VDT range of 1.2~3.3V.
When pulled lower than V_{DT} [Typ. 0.5V] the device is shutdown.
Care must be taken to avoid below threshold spikes on pin 3 that can cause undesired shut down of the IC. For this reason the connection of the components between pin 3 and ground has to be as short as possible. And a capacitor (Typ. 0.02μF)between pin3 and COM can prevent this spike . This pin can not be left floating for the same reason.

Figure 1. Typical Application

BLOCK DIAGRAM

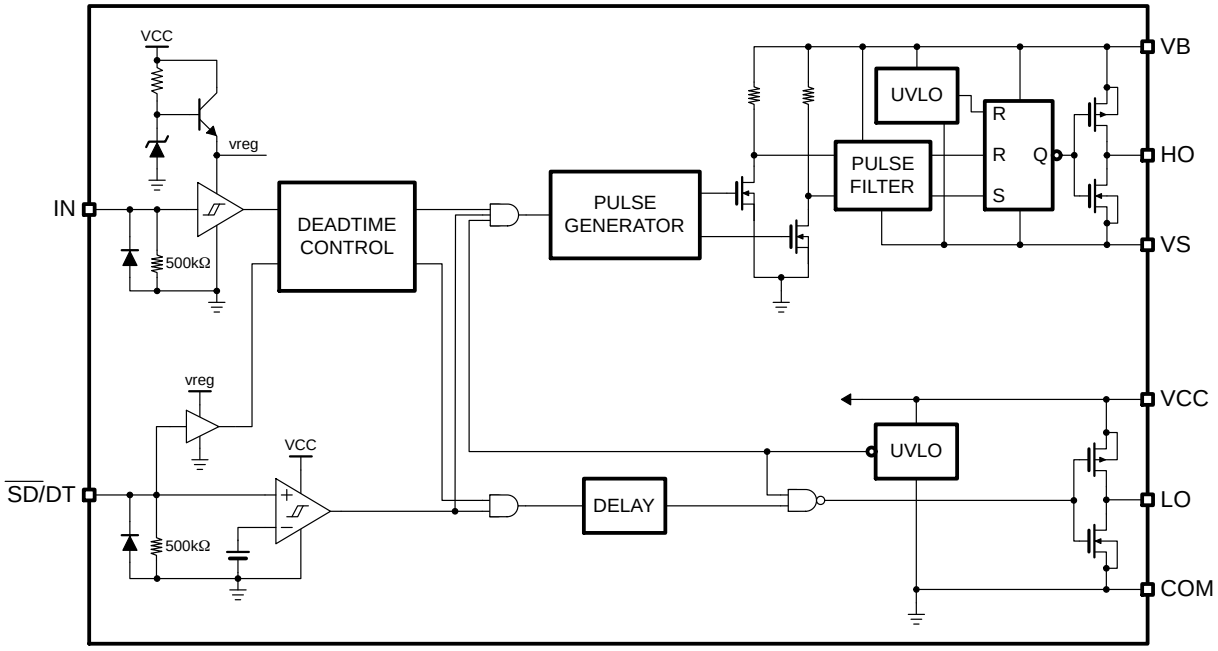


Figure 2. Block Diagram

PIN CONFIGURATION

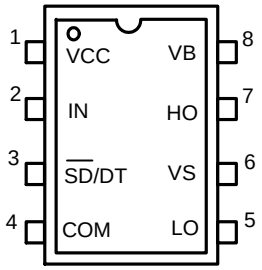


Figure 3. Pin Assignment (Top Through View)

PIN DESCRIPTIONS

Pin #	Name	I/O	Pin Function Description
1	V_{CC}	P	Driver Supply Voltage
2	IN	I	Logic input for high and low side gate drive output
3	$\overline{SD}$/DT	I	Shutdown Input and dead time setting
4	COM	P	Ground
5	LO	A	Low side gate drive output for MOSFET Gate connection
6	VS	A	High side floating offset for MOSFET Source connection
7	HO	A	High side drive output for MOSFET Gate connection
8	VB	P	Driver Output Stage Supply

ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristics	Min.	Max.	Unit
V_S	High−Side Floating Offset Voltage	V_B−25	V_B+0.3	V
V_B	High−Side Floating Supply Voltage	−0.3	625	V
V_{HO}	High−Side Floating Output Voltage	V_S−0.3	V_B+0.3	V
V_{LO}	Low−Side Floating Output Voltage	−0.3	V_{CC}+0.3	V
V_{CC}	Supply Voltage	−0.3	25	V
V_{IN}	Input Voltage for IN	−0.3	V_{CC}+0.3	V
I_{IN}	Input Injection Current (Note 1)		+1	mA
P_D	Power Dissipation (Notes 2, 3)		0.625	W
θ_{JA}	Thermal Resistance, Junction to Ambient (Note 2)		200	°C/W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	−55	150	°C
ESD	Human Body Model (HBM)		1000	V
	Charge Device Model (CDM)		500	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Guaranteed by design. Full function, no latchup. Tested at 10 V and 17 V.
2. The Thermal Resistance and power dissipation rating are measured per below conditions:
   JESD51−2: Integral circuits thermal test method environmental conditions, natural convection/Still Air
   JESD51−3: Low effective thermal conductivity test board for leaded surface−mount packages.
3. Do not exceed power dissipation (P_D) under any circumstances.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min.	Max.	Unit
V_{BS} (Note 4)	High−Side Floating Supply Voltage (DC) Transient: −10 V at 0.1 μs	V_S+6	V_S+20	V
V_S	High−Side Floating Supply Offset Voltage (DC) Transient: −25 V(max.) at 0.1 μs at V_{BS} < 25 V	−5	600	V
V_{HO}	High−Side Output Voltage	V_S	V_B	V
V_{LO}	Low−Side Output Voltage	0	V_{CC}	V
V_{CC}	Supply Voltage for Logic Input	5.5	20	V
V_{IN}	Logic Input Voltage	0	V_{CC}	V
dv/dt	Allowable Offset Voltage Slew Rate (Note 5)		50	V/ns
T_{PULSE}	Minimum Pulse Width (Notes 5, 6)	1100		ns
F_S	Switching Frequency (Note 6)		200	kHz
T_A	Operating Ambient Temperature	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. The Vs offset is tested w ith all supplies based at 15 V differential
5. Guaranteed by design.
6. When V_{DT} = 1.2 V. Ref er to Figures 5, 6, 7 and 8.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified −40°C ≤ T_A ≤ 125°C, V_{CC} = 15 V, V_{BS} = 15 V, V_S = 0 V, C_L = 1 nF)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VCC and VBS Supply Characteristics						
VCCUV+ VBSUV+	VCC and VBS Supply Under−Voltage Positive going Threshold			4.2	5.5	V
VCCUV− VBSUV−	VCC and VBS Supply Under−Voltage Negative going Threshold		2.8	3.6		V
VCCUVH VBSUVH	VCC and VBS Supply Under−Voltage Hysteresis		0.2	0.6		V
tDUVCC tDUVBS	Under−Voltage Lockout Response Time	VCC: 6 V→2.5 V or 2.5 V→6 V	0.5		20	μs
		VBS: 6 V→2.5 V or 2.5 V→6 V	0.5		20	
ILK	Offset Supply Leakage Current	VB = VS = 600 V		20	50	μA
IQBS	Quiescent VBS Supply Current	VIN = 0 or 5 V, VSDT = 1.2 V	20	75	150	μA
IQCC	Quiescent VCC Supply Current	VIN = 0 or 5 V, VSDT = 1.2 V		350	1000	μA
Input Characteristics						
VIH	High Logic level Input Voltage		2.7			V
VIL	Low Logic Level Input Voltage				0.8	V
IIN+	Logic Input High Bias Current	VIN = 5 V		10	50	μA
IIN−	Logic Input Low Bias Current	VIN = 0 V		0	2	μA
VDT	VDT Dead Time Setting Range		1.2		5.0	V
VSD	VSD Shutdow n Threshold Voltage			0.8	1.2	V
RSDT	High Logic Level Resistance for $\overline{SD}$ /DT	VSDT = 5 V	100	500	1100	kΩ
ISDT−	Low Logic Level Input bias Current for $\overline{SD}$ /DT	VSDT = 0 V		1	2	μA
Output Characteristics						
VOH(HO)	High Level Output Voltage (VCC − VHO)	IO = 0			0.1	V
VOL(HO)	Low Level Output Voltage (VHO)	IO = 0			0.1	V
IO+(HO)	Output High, Short−Circuit Pulse Current		250	300		mA

ELECTRICAL CHARACTERISTICS (continued)
(Unless otherwise specified −40°C ≤ T_A ≤ 125°C, V_{CC} = 15 V, V_{BS} = 15 V, V_S = 0 V, C_L = 1 nF)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Output Characteristics						
$I_{O-(HO)}$	Output Low , Short−Circuit Pulse Current		500	600		mA
$R_{OP(HO)}$	Equivalent Output Resistance				60	Ω
$R_{ON(HO)}$					30	
$V_{OH(LO)}$	High Level Output Voltage (V_B – V_{LO})	I_O = 0			0.1	V
$V_{OL(LO)}$	Low Level Output Voltage (V_{LO})	I_O = 0			0.1	V
$I_{O+(LO)}$	Output High, Short−Circuit Pulse Current		250			mA
$I_{O-(LO)}$	Output Low , Short−Circuit Pulse Current		500			mA
$R_{OP(LO)}$	Equivalent Output Resistance				60	Ω
$R_{ON(LO)}$					30	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DYNAMIC ELECTRICAL CHARACTERISTICS
(Unless otherwise specified −40°C ≤ T_A ≤ 125°C, V_{CC} = 15 V, V_{BS} = 15 V, V_S = 0 V, C_L = 1 nF)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{ON}	Turn−On Propagation Delay (Note 7)	V_S = 0 V		750	1500	ns
t_{OFF}	Turn−Off Propagation Delay	V_S = 0 V		130	250	ns
t_R	Turn−On Rise Time			40	150	ns
t_F	Turn−Off Fall Time			25	400	ns
D_T	Dead Time, LS Turn−off to HS Turn−on and HS Turn−on to LS Turn−off	V_{IN} = 0 or 5 V at VDT = 1.2 V	250	650	1200	ns
		V_{IN} = 0 or 5 V at VDT = 1.2 V	1600	2100	2600	
M_{DT}	Dead Time Matching Time	DT1 – DT2 at VDT = 1.2 V		35	110	ns
		DT1 – DT2 at VDT = 3.3 V			300	
M_{TON}	Delay Matching, HS and LS Turn−on	VDT = 1.2 V		25	110	ns
M_{TOFF}	Delay Matching, HS and LS Turn−off	VDT = 1.2 V		15	60	ns
t_{SD}	Shutdown Propagation Delay			180	330	ns
F_{S1}	Switching Frequency	V_{CC} = V_{BS} = 20 V			200	kHz
F_{S2}		V_{CC} = V_{BS} = 5.5 V			200	

7. t_{ON} includes DT

TYPICAL WAVEFORMS

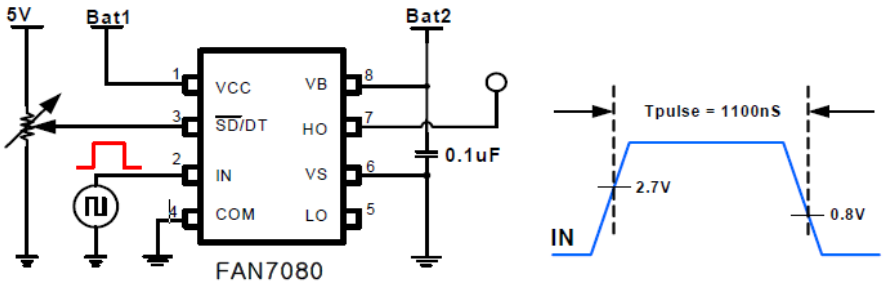


Figure 4. Short Pulse Width Test Circuit and Pulse Width Waveform

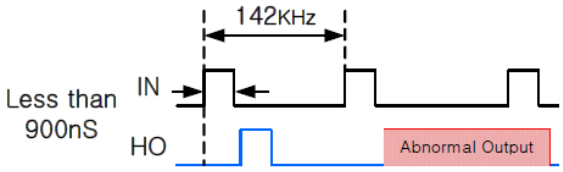


Figure 5. Abnormal Output Waveform with Pulse Width

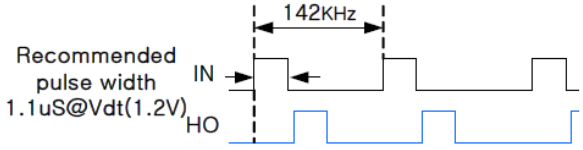


Figure 6. Recommendation of Pulse Width Output Waveform

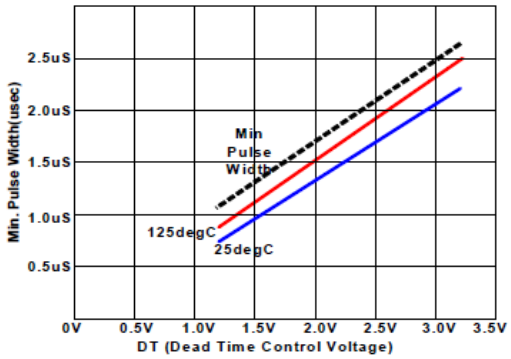


Figure 7. Pulse Width vs. V_{DT}

TYPICAL PERFORMANCE CHARACTERISTICS

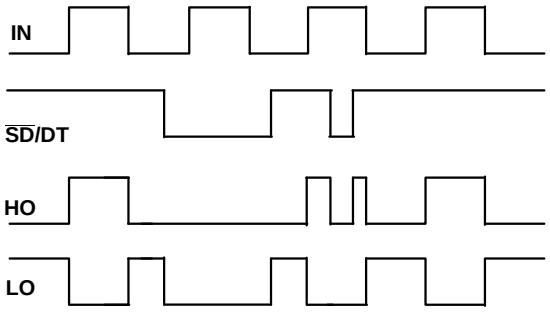


Figure 8. Input/Output Timing Diagram

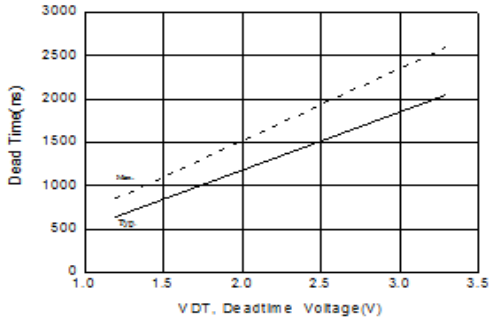
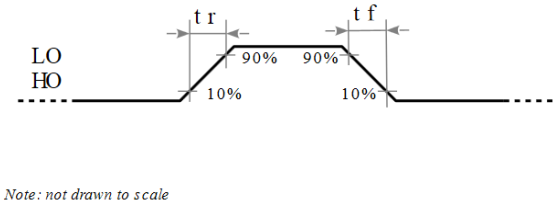


Figure 9. Dead Time vs. V_{DT}
(V_{CC} = V_{BS} = 15 V, −40°C < T_J < 125°C)



Note: not drawn to scale

Figure 10. Switching Time Waveform Definitions

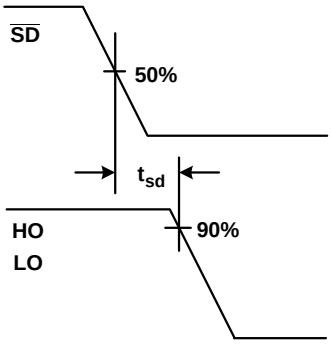


Figure 11. Shutdown Waveform Definitions

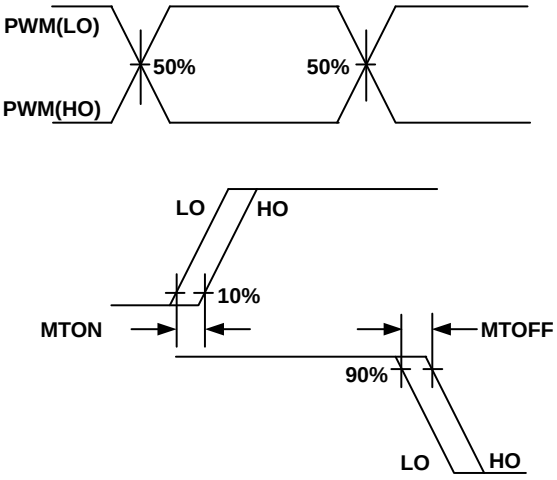
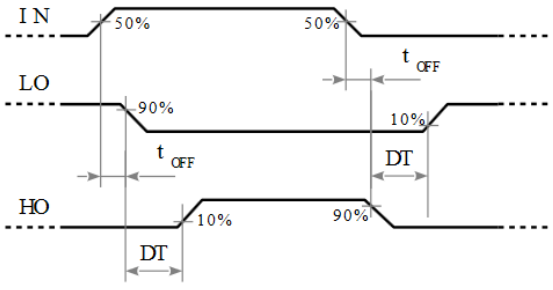


Figure 12. Delay Matching Waveform Definitions



Note: not drawn to scale

Figure 13. Dead Time Waveform Definitions

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

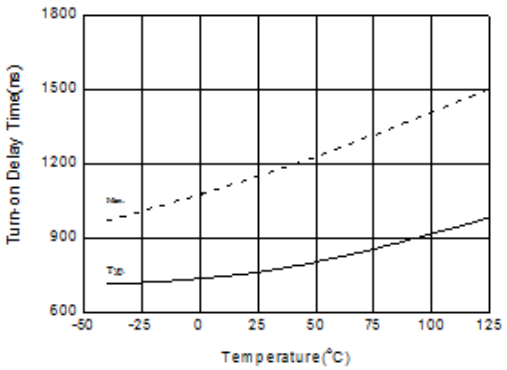


Figure 14. Turn−On Delay Time of HO vs. Temperature (V_{CC} = V_{BS} = 15 V, C_L = 1 nF)

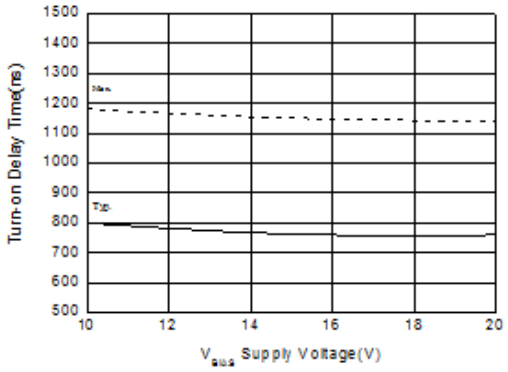


Figure 15. Turn−On Delay Time of HO vs. V_{BS} Supply Voltage (V_{CC} = 15 V, C_L = 1 nF, T_A = 25°C)

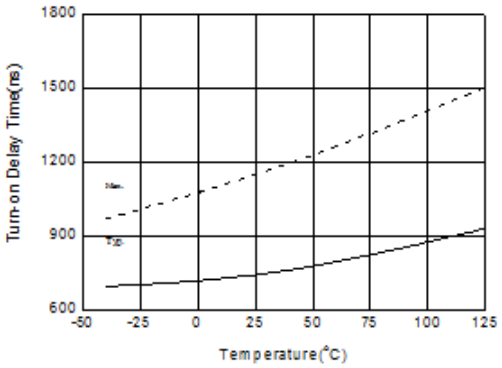


Figure 16. Turn−On Delay Time of LO vs. Temperature (V_{CC} = V_{BS} = 15 V, C_L = 1 nF)

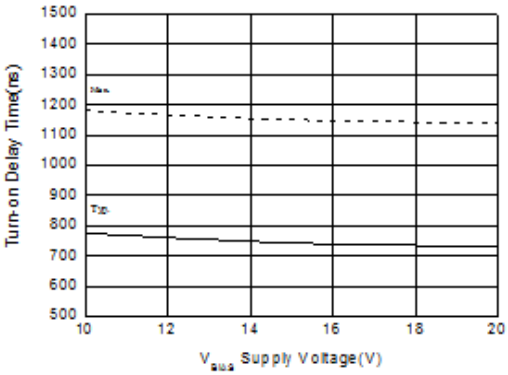


Figure 17. Turn−On Delay Time of LO vs. V_{BS} Supply Voltage (V_{CC} = 15 V, C_L = 1 nF, T_A = 25°C)

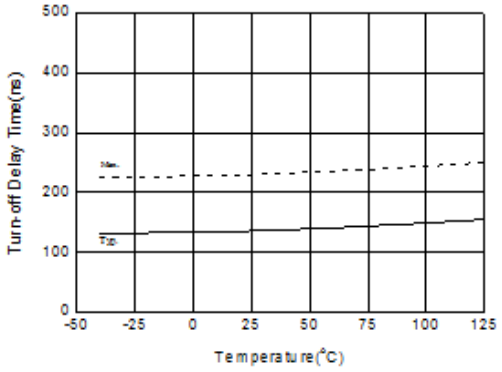


Figure 18. Turn−Off Delay Time of HO vs. Temperature (V_{CC} = V_{BS} = 15 V, C_L = 1 nF)

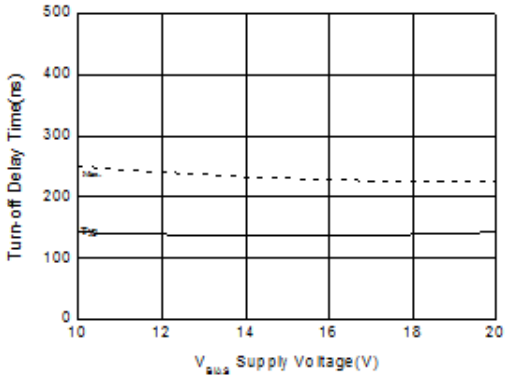


Figure 19. Turn−Off Delay Time of HO vs. V_{BS} Supply Voltage (V_{CC} = 15 V, C_L = 1 nF, T_A = 25°C)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

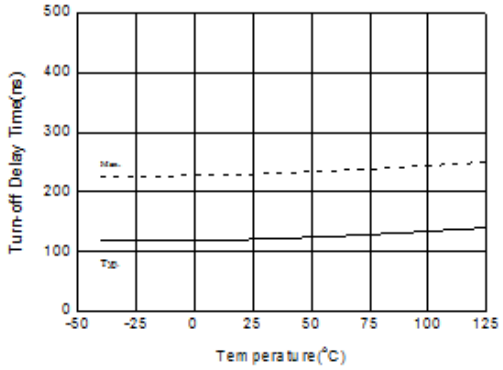


Figure 20. Turn−Off Delay Time of LO vs. Temperature (V_{CC} = V_{BS} = 15 V, C_L = 1 nF)

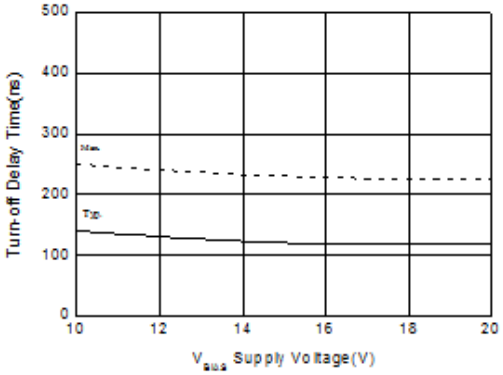


Figure 21. Turn−Off Delay Time of HO vs. V_{BS} Supply Voltage (V_{CC} = 15 V, C_L = 1 nF, T_A = 25°C)

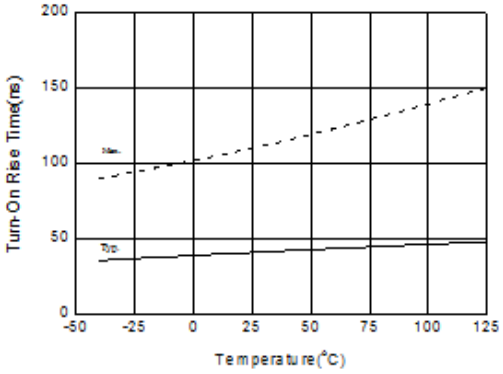


Figure 22. Turn−On Rise Time of HO vs. Temperature (V_{CC} = V_{BS} = 15 V, C_L = 1 nF)

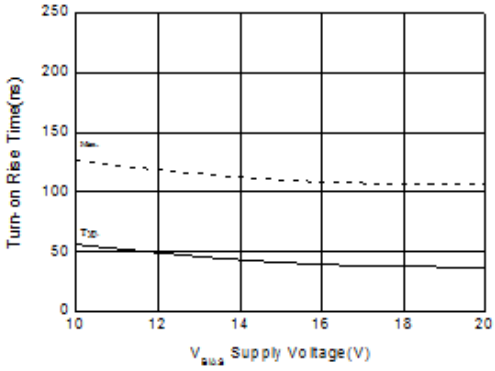


Figure 23. Turn−On Rise Time of HO vs. V_{BS} Supply Voltage (V_{CC} = 15 V, C_L = 1 nF, T_A = 25°C)

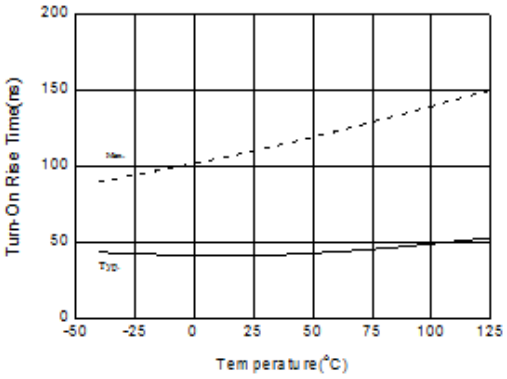


Figure 24. Turn−On Rise Time of LO vs. Temperature (V_{CC} = V_{BS} = 15 V, C_L = 1 nF)

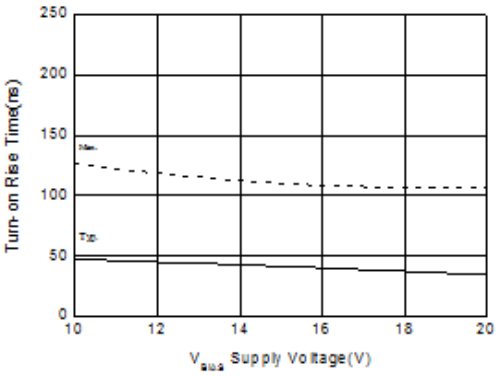


Figure 25. Turn−On Rise Time of LO vs. V_{BS} Supply Voltage (V_{CC} = 15 V, C_L = 1 nF, T_A = 25°C)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

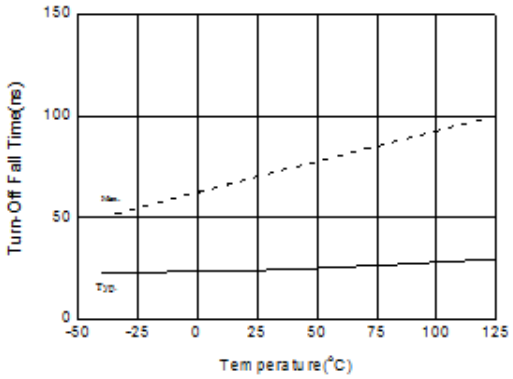


Figure 26. Turn−Off Fall Time of HO vs. Temperature (V_{CC} = V_{BS} = 15 V, C_L = 1 nF)

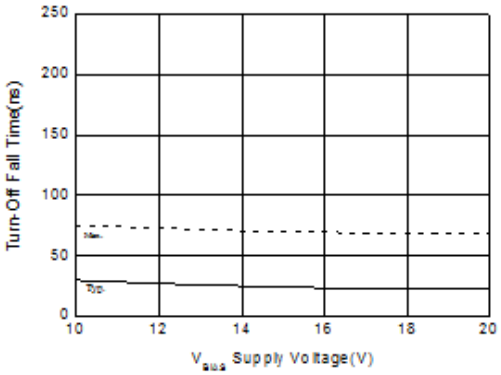


Figure 27. Turn−Off Fall Time of HO vs. V_{BS} Supply Voltage (V_{CC} = 15 V, C_L = 1 nF, T_A = 25°C)

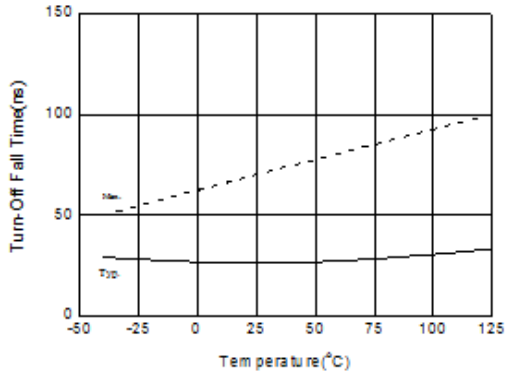


Figure 28. Turn−Off Fall Time of LO vs. Temperature (V_{CC} = V_{BS} = 15 V, C_L = 1 nF)

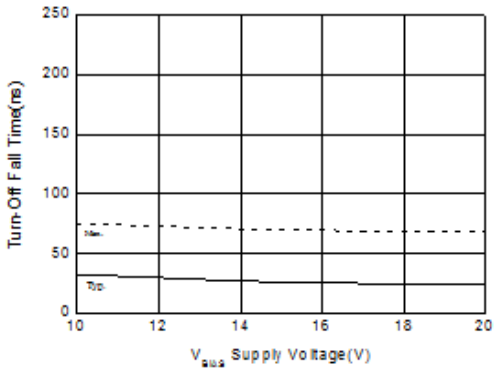


Figure 29. Turn−Off Fall Time of LO vs. V_{BS} Supply Voltage (V_{CC} = 15 V, C_L = 1 nF, T_A = 25°C)

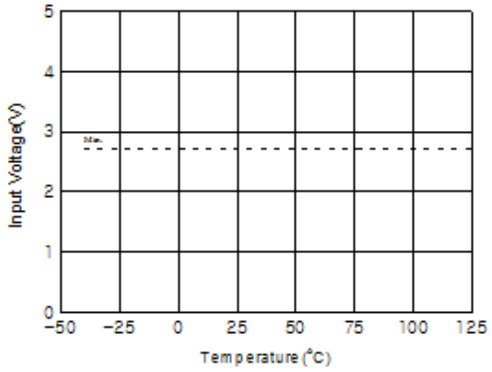


Figure 30. Logic Low Input Voltage vs. Temperature

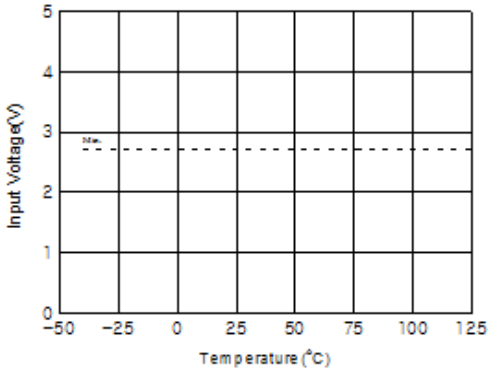


Figure 31. Logic High Input Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

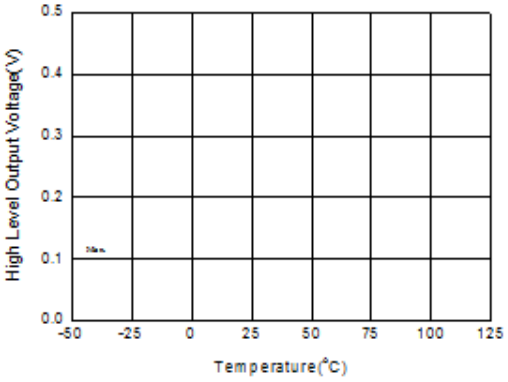


Figure 32. High Level Output of HO vs. Temperature (V_{CC} = V_{BS} = 15 V)

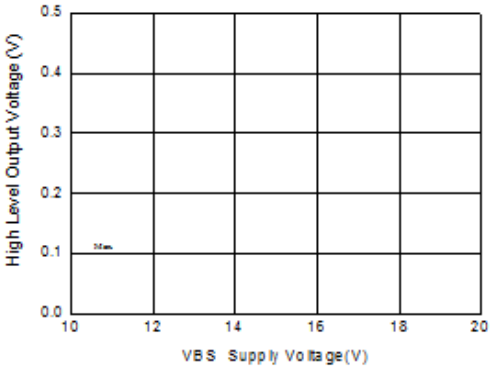


Figure 33. High Level Output of HO vs. V_{BS} Supply Voltage (V_{CC} = 15 V, T_A = 25°C)

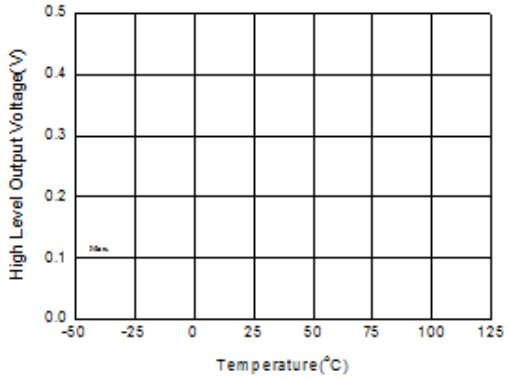


Figure 34. High Level Output of LO vs. Temperature (V_{CC} = V_{BS} = 15 V)

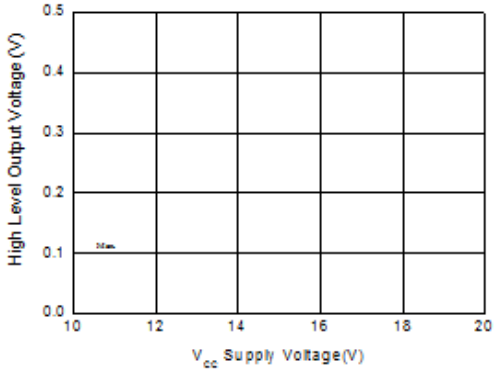


Figure 35. High Level Output of LO vs. V_{BS} Supply Voltage (V_{CC} = 15 V, T_A = 25°C)

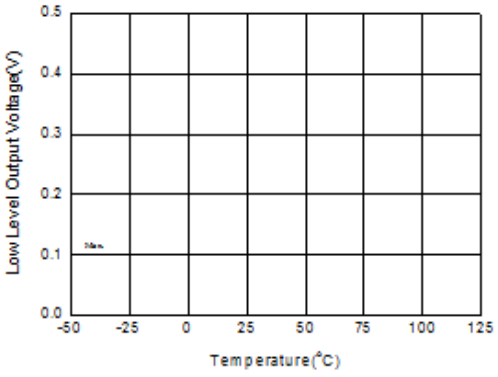


Figure 36. Low Level Output of HO vs. Temperature (V_{CC} = V_{BS} = 15 V)

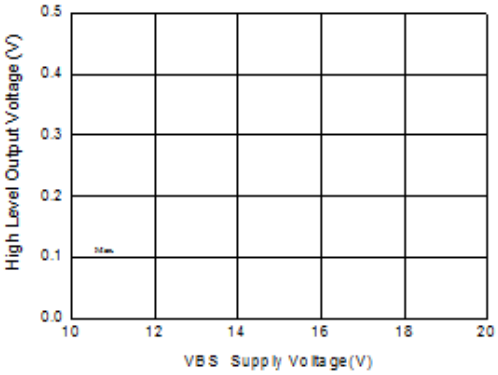


Figure 37. Low Level Output of HO vs. V_{BS} Supply Voltage (V_{CC} = 15 V, T_A = 25°C)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

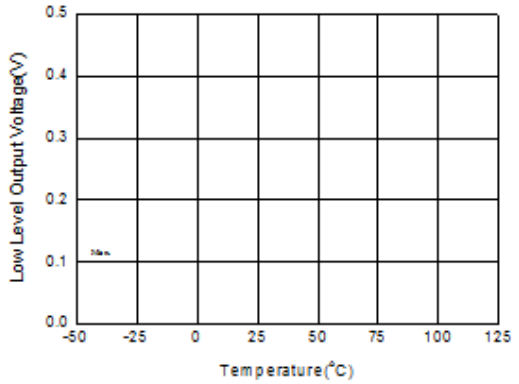


Figure 38. Low Level Output of LO vs. Temperature (V_{CC} = V_{BS} = 15 V)

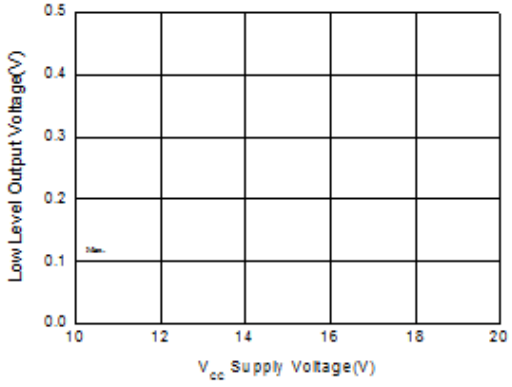


Figure 39. Low Level Output of LO vs. V_{CC} Supply Voltage (V_{CC} = 15 V, T_A = 25°C)

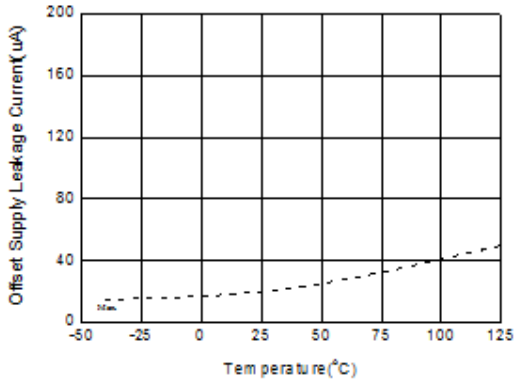


Figure 40. Offset Supply Leakage Current vs. Temperature (V_{CC} = V_{BS} = 600 V)

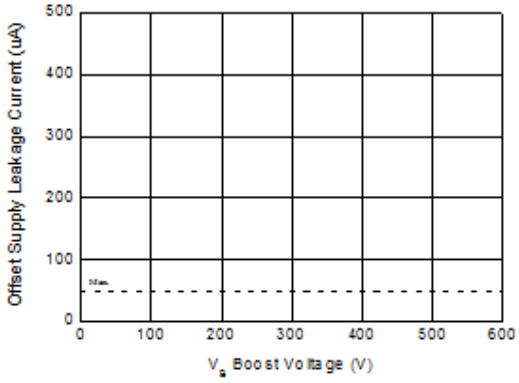


Figure 41. Offset Supply Leakage Current vs. V_B Boost Voltage (V_{CC} = 15 V, T_A = 25°C)

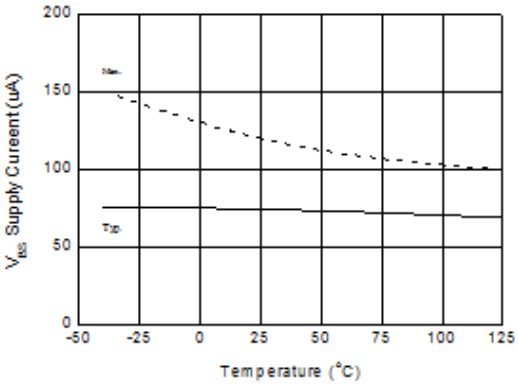


Figure 42. V_{BS} Supply Current vs. Temperature (V_{BS} = 15 V)

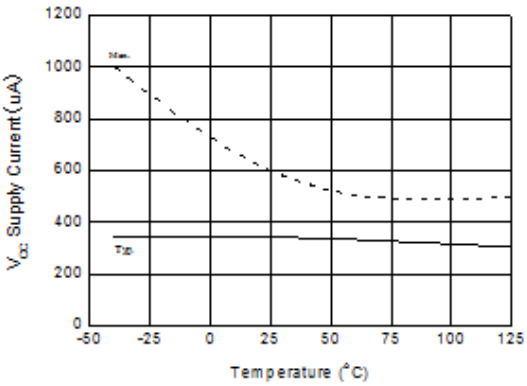


Figure 43. V_{CC} Supply Current vs. Temperature (V_{CC} = 15 V)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

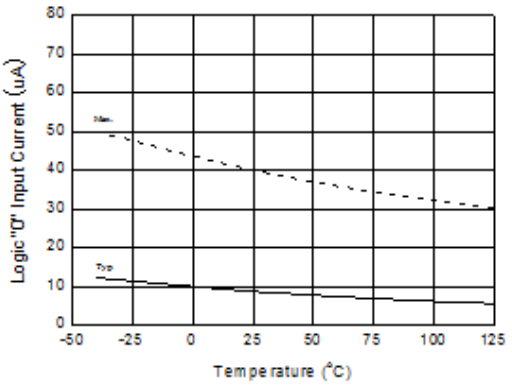


Figure 44. Logic High Input Current vs. Temperature (V_{IN} = 5 V)

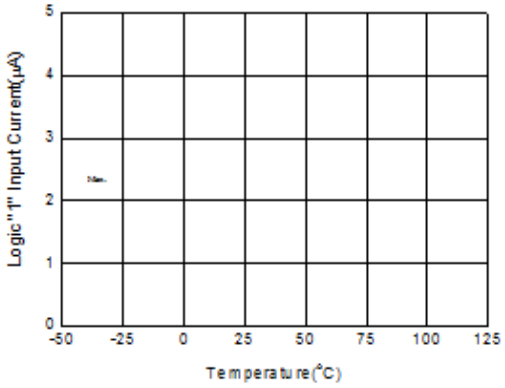


Figure 45. Logic Low Input Current vs. Temperature (V_{IN} = 5 V)

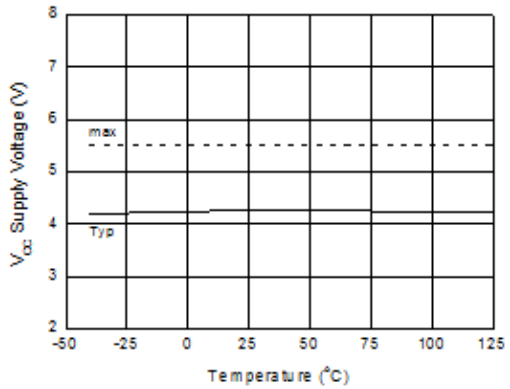


Figure 46. V_{CC} Under−Voltage Threshold (+) vs. Temperature

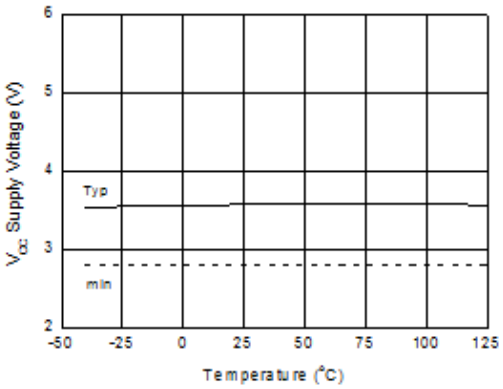


Figure 47. V_{CC} Under−Voltage Threshold (−) vs. Temperature

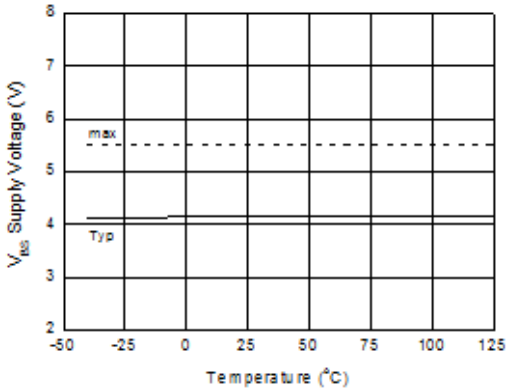


Figure 48. V_{BS} Under−Voltage Threshold (+) vs. Temperature

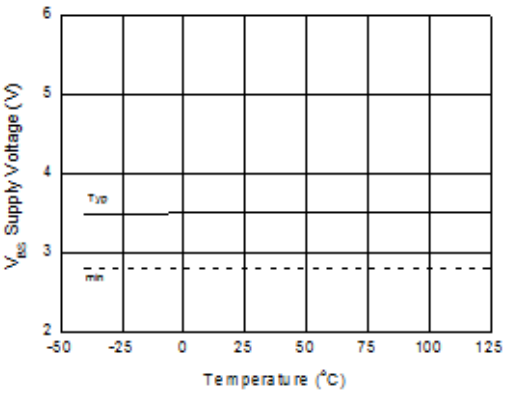


Figure 49. V_{BS} Under−Voltage Threshold (−) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

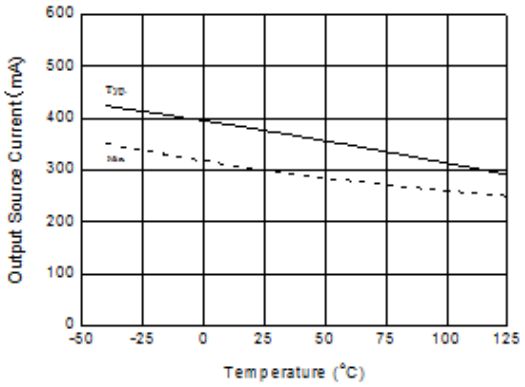


Figure 50. Output Source Current of HO vs. Temperature (V_{CC} = V_{BS} = 15 V)

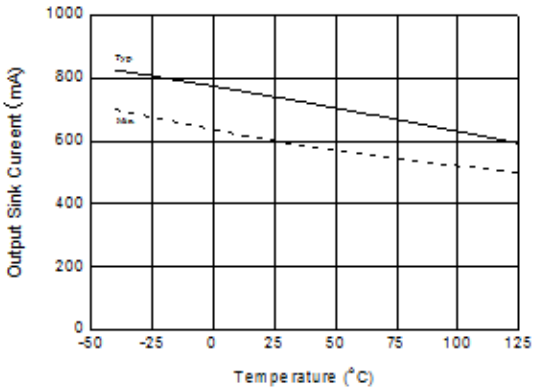


Figure 51. Output Sink Current of HO vs. Temperature (V_{CC} = V_{BS} = 15 V)

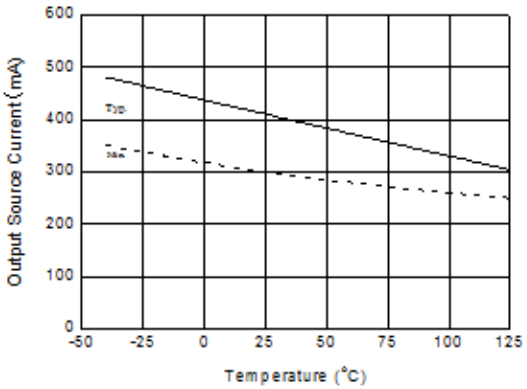


Figure 52. Output Source Current of LO vs. Temperature (V_{CC} = V_{BS} = 15 V)

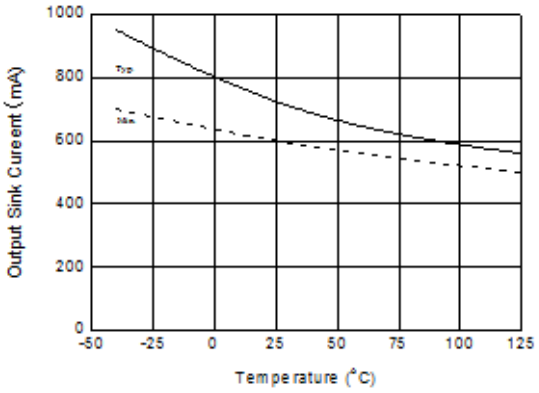


Figure 53. Output Sink Current of LO vs. Temperature (V_{CC} = V_{BS} = 15 V)

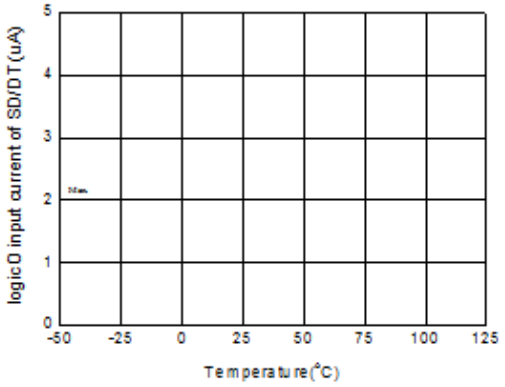


Figure 54. Logic Low Input Current of $\overline{SD}$/DT vs. Temperature

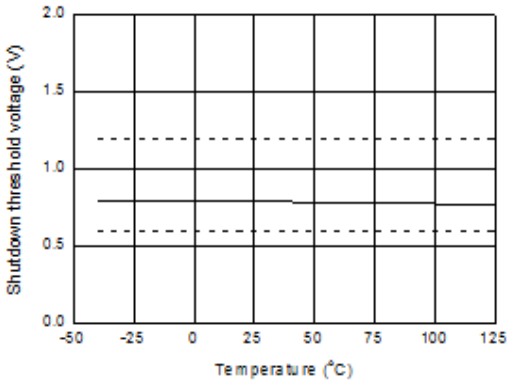


Figure 55. Shutdown Threshold Voltage vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

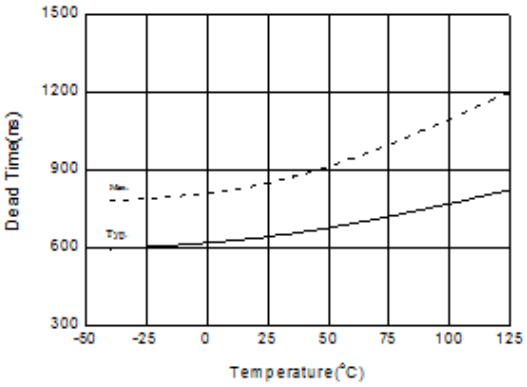


Figure 56. Deadtime vs. Temperature (V_{CC} = V_{BS} = 15 V, V_{DT} = 1.2 V)

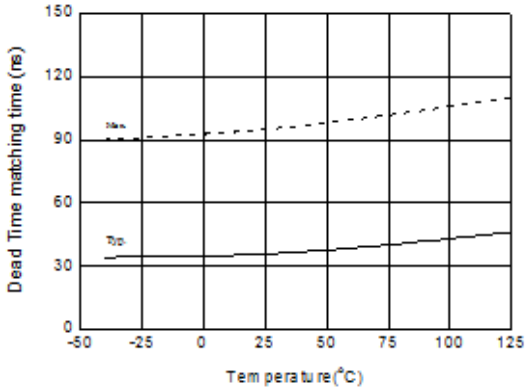


Figure 57. Deadtime Matching Time vs. Temperature (V_{CC} = V_{BS} = 15 V, V_{DT} = 1.2 V)

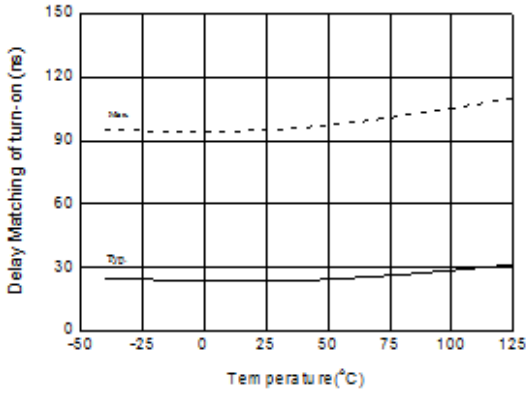


Figure 58. Turn−on Delay Matching vs. Temperature (V_{CC} = V_{BS} = 15 V, V_{DT} = 1.2 V)

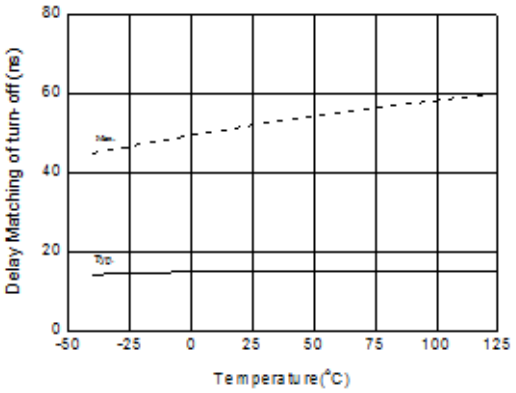


Figure 59. Turn−off Delay Matching vs. Temperature (V_{CC} = V_{BS} = 15 V, V_{DT} = 1.2 V)

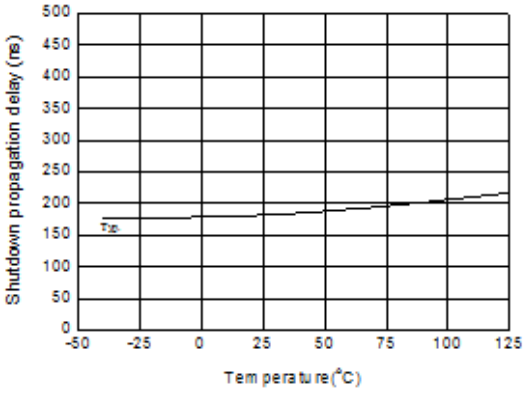


Figure 60. Shutdown Propagation Delay vs. Temperature

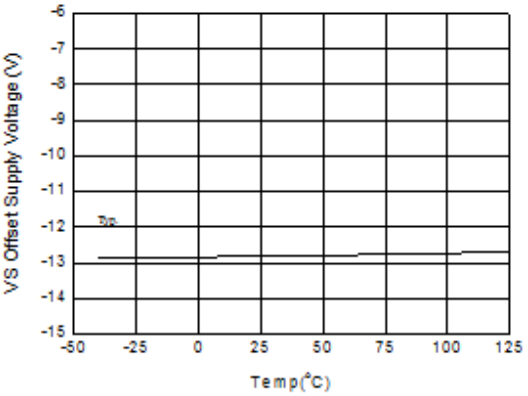
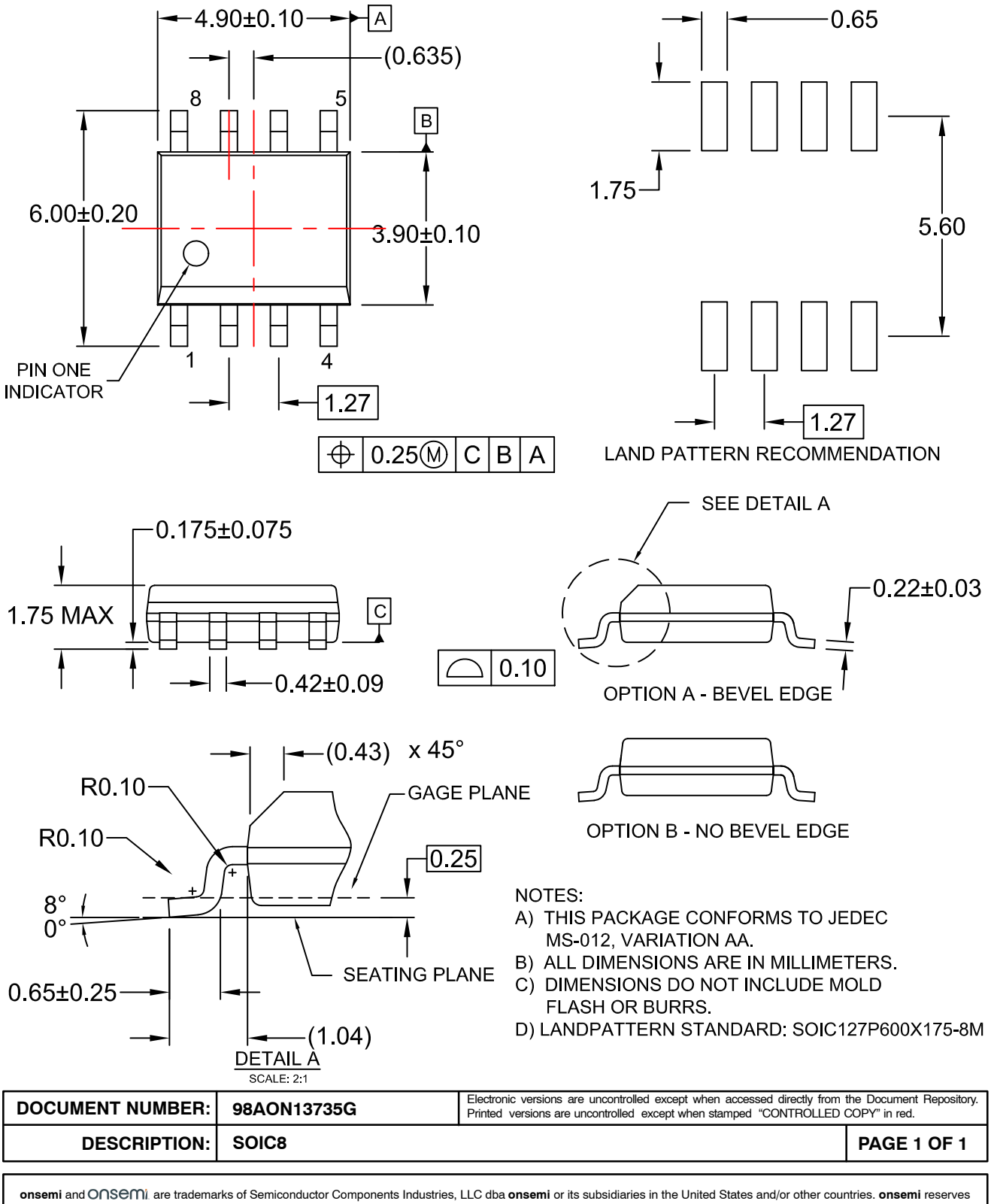


Figure 61. Maximum vs. Negative Offset Voltage vs. Temperature (V_{CC} = V_{BS} = 15 V)

SOIC8
CASE 751EB
ISSUE A

DATE 24 AUG 2017



NOTES:
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