

# ON Semiconductor

## Is Now



To learn more about onsemi™, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

onsemi and onsemi. and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using onsemi products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by onsemi. "Typical" parameters which may be provided in onsemi data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. onsemi does not convey any license under any of its intellectual property rights nor the rights of others. onsemi products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use onsemi products for any such unintended or unauthorized application, Buyer shall indemnify and hold onsemi and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that onsemi was negligent regarding the design or manufacture of the part. onsemi is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.



ON Semiconductor®

## FAN7083-GF085

### High Side Gate Driver with Reset

#### Features

- Qualified to AEC Q100
- Floating channel designed for bootstrap operation up fully operational to + 600V
- Tolerance to negative transient voltage on VS pin
- dv/dt immune.
- Gate drive supply range from 10V to 20V
- Under-voltage lockout
- CMOS Schmitt-triggered inputs with pull-down
- High side output in phase with input
- RESET input is 3.3V and 5V logic compatible

#### Typical Applications

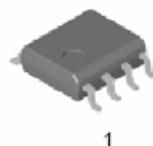
- Diesel and gasoline injectors/valves
- MOSFET-and IGBT high side driver applications



#### Description

The FAN7083-GF085 is a high-side gate drive IC with reset input. It is designed for high voltage and high speed driving of MOSFET or IGBT, which operates up to 600V. ON Semiconductor's high-voltage process and common-mode noise cancellation technique provide stable operation in the high side driver under high-dv/dt noise circumstances. An advanced level-shift circuit allows high-side gate driver operation up to  $V_S = -5V$  (typical) at  $V_{BS} = 15V$ . Logic input is compatible with standard CMOS out-puts. The UVLO circuits prevent from malfunction when VCC and VBS are lower than the specified threshold voltage. It is available with space saving SOIC-8 Package. Minimum source and sink current capability of output driver is 200mA and 400mA respectively, which is suitable for magnetic-and piezo type injectors and general MOSFET/IGBT based high side driver applications.

#### SOIC-8



#### Ordering Information

| Device          | Package | Operating Temp. |
|-----------------|---------|-----------------|
| FAN7083M-GF085  | SOIC-8  | -40 °C ~ 125 °C |
| FAN7083MX-GF085 | SOIC-8  | -40 °C ~ 125 °C |

X : Tape & Reel type



## Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM.

| Parameter                                             | Symbol | Min.   | Max.    | Unit |
|-------------------------------------------------------|--------|--------|---------|------|
| High side floating supply offset voltage              | VS     | VB-25  | VB+0.3  | V    |
| High side floating supply voltage                     | VB     | -0.3   | 625     | V    |
| High side floating output voltage                     | VHO    | Vs-0.3 | VB+0.3  | V    |
| Supply voltage                                        | VCC    | -0.3   | 25      | V    |
| Input voltage for IN                                  | VIN    | -0.3   | VCC+0.3 | V    |
| Input voltage for RESET                               | VRESET | -0.3   | VCC+0.3 | V    |
| Power Dissipation <sup>1)</sup>                       | Pd     |        | 0.625   | W    |
| Thermal resistance, junction to ambient <sup>1)</sup> | Rthja  |        | 200     | °C/W |
| Electrostatic discharge voltage (Human Body Model)    | VESD   | 1K     |         | V    |
| Charge device model                                   | VCDM   | 500    |         | V    |
| Junction Temperature                                  | Tj     |        | 150     | °C   |
| Storage Temperature                                   | Ts     | -55    | 150     | °C   |

Note: 1) The thermal resistance and power dissipation rating are measured bellow conditions;

JESD51-2: Integrated Circuit Thermal Test Method Environmental Conditions - Natural convection(StillAir)

JESD51-3 : Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Package

## Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. -40°C ≤ Ta ≤ 125°C

| Parameter                                                 | Symbol             | Min.                                                | Max.    | Unit |
|-----------------------------------------------------------|--------------------|-----------------------------------------------------|---------|------|
| High side floating supply voltage<br>-10V Transient 0.2us | VB                 | Vs + 10                                             | Vs + 20 | V    |
| High side floating supply offset voltage(DC)              | VS                 | -4 (@VBS ≥ 10V)<br>-5 (@VBS ≥ 11.5V)                | 600     | V    |
| High side floating supply offset voltage(Transient)       | VS                 | -25 (~200ns)<br>-20(200ns~240ns)<br>-7(240ns~400ns) | 600     | V    |
| High side floating output voltage                         | VHO                | Vs                                                  | VB      | V    |
| Allowable offset voltage Slew Rate <sup>1)</sup>          | dv/dt              | -                                                   | 50      | V/ns |
| Supply voltage                                            | VCC                | 10                                                  | 20      | V    |
| Input voltage for IN                                      | VIN                | 0                                                   | Vcc     | V    |
| Input voltage for RESET                                   | VRESET             | 0                                                   | Vcc     | V    |
| Switching Frequency <sup>2)</sup>                         | Fs                 |                                                     | 200     | KHz  |
| Minimum Pulse Width <sup>(3)</sup>                        | T <sub>pulse</sub> | 85                                                  | -       | ns   |
| Ambient Temperature                                       | Ta                 | -40                                                 | 125     | °C   |

Note : 1) Guaranteed by design.

2) Duty = 0.5

3) Guaranteed by design. Refer to Figure 4a, 4b and 4c on Page 9.

## Statics Electrical Characteristics

Unless otherwise specified,  $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ ,  $V_{CC} = 15\text{V}$ ,  $V_{BS} = 15\text{V}$ ,  $V_{RESET} = 5\text{V}$ ,  $V_S = 0\text{V}$ ,  $R_L = 50\Omega$ ,  $C_L = 2.5\text{nF}$ .

| Parameter                                                        | Symbol           | Conditions                                                     | Min.       | Typ. | Max.     | Unit     |
|------------------------------------------------------------------|------------------|----------------------------------------------------------------|------------|------|----------|----------|
| <b>Vcc and VBS supply Characteristics</b>                        |                  |                                                                |            |      |          |          |
| VCC and VBS supply under voltage positive going threshold        | VCCUV+<br>VBSUV+ | -                                                              | -          | 9.0  | 9.8      | V        |
| VCC and VBS supply under voltage negative going threshold        | VCCUV-<br>VBSUV- | -                                                              | 7.4        | 8.4  | -        | V        |
| VCC and VBS supply under voltage hysteresis                      | VCCUVH<br>VBSUVH | -                                                              | 0.2        | 0.6  | -        | V        |
| Under voltage lockout response time                              | tduvcc<br>tduvbs | VCC: 10V-->7.3V or 7.3V-->10V<br>VBS: 10V-->7.3V or 7.3V-->10V | 0.5<br>0.5 |      | 20<br>20 | us<br>us |
| Offset supply leakage current                                    | ILK              | $V_B = V_S = 600\text{V}$                                      | -          | -    | 50       | uA       |
| Quiescent VBS supply current                                     | IQBS             | $V_{IN}=0$ , $V_{RESET}=5\text{V}$                             | -          | 50   | 100      | uA       |
|                                                                  |                  |                                                                |            |      |          |          |
| Quiescent Vcc supply current                                     | IQCC1            | $V_{IN}=V_{RESET}=0$                                           | -          | 65   | 140      | uA       |
| Quiescent Vcc supply current                                     | IQCC2            | $V_{IN}=15\text{V}$ , $V_{RESET}=0$                            | -          | 75   | 160      | uA       |
| <b>Input Characteristics</b>                                     |                  |                                                                |            |      |          |          |
| High logic level input voltage for IN                            | VIH              | -                                                              | 0.63Vcc    |      | -        | V        |
| Low logic level input voltage for IN                             | VIL              | -                                                              | -          | -    | 0.4Vcc   | V        |
| High logic level input current for IN                            | IIN+             | $V_{IN}=15\text{V}$                                            | -          | 15   | 50       | uA       |
| Low logic level input bias current for IN                        | IIN-             | $V_{IN}=0$                                                     | -          | 0    | 1        | uA       |
| High logic level input voltage for $\overline{\text{RESET}}$     | VRIH             | -                                                              | 3.0        | -    | -        | V        |
| Low logic level input voltage for $\overline{\text{RESET}}$      | VRIL             | -                                                              | -          | -    | 1.4      | V        |
| High logic level input current for $\overline{\text{RESET}}$     | IRIN+            | $V_{RESET}=5\text{V}$                                          | -          | 5    | 30       | uA       |
| Low logic level input bias current for $\overline{\text{RESET}}$ | IRIN-            | $V_{RESET}=0$                                                  | -          | 0    | 1        | uA       |
| <b>Output characteristics</b>                                    |                  |                                                                |            |      |          |          |
| High level output voltage, $V_{BIAS}-V_O$                        | VOH              | $I_O=0$                                                        | -          | -    | 0.1      | V        |
| Low level output voltage, $V_O$                                  | VOL              | $I_O=0$                                                        | -          | -    | 0.1      | V        |
| Peak output source current                                       | IO1+             | -                                                              | 200        | -    | -        | mA       |
| Peak output sink current                                         | IO1-             | -                                                              | 400        | -    | -        | mA       |
| Equivalent output resistance                                     | ROP              |                                                                |            | 54   | 75       | $\Omega$ |
|                                                                  | RON              |                                                                |            | 24   | 38       | $\Omega$ |

Note: The input parameter are referenced to COM. The VO and IO parameters are referenced to COM.

## Dynamic Electrical Characteristics

Unless otherwise specified,  $-40^{\circ}\text{C} \leq T_a \leq 125^{\circ}\text{C}$ ,  $V_{CC} = 15\text{V}$ ,  $V_{BS} = 15\text{V}$ ,  $V_{RESET} = 5\text{V}$ ,  $V_S = 0\text{V}$ ,  $R_L = 50\Omega$ ,  $C_L = 2.5\text{nF}$ .

| Parameter                                  | Symbol               | Conditions                                                  | Min. | Typ. | Max. | Unit |
|--------------------------------------------|----------------------|-------------------------------------------------------------|------|------|------|------|
| IN-to-output turn-on propagation delay     | t <sub>plh</sub>     | 50% input level to 10% output level,<br>V <sub>S</sub> = 0V | -    | 115  | 250  | ns   |
| IN-to-output turn-off propagation delay    | t <sub>phl</sub>     | 50% input level to 90% output level<br>V <sub>S</sub> = 0V  | -    | 90   | 200  | ns   |
| RESET-to-output turn-off propagation delay | t <sub>phl_res</sub> | 50% input level to 90% output level                         | -    | 90   | 200  | ns   |
| RESET-to-output turn-on propagation delay  | t <sub>plh_res</sub> | 50% input level to 10% output level                         | -    | 115  | 250  | ns   |
| Output rising time                         | t <sub>r1</sub>      | T <sub>j</sub> =25°C, V <sub>BS</sub> =15V                  | -    | 200  | 400  | ns   |
|                                            | t <sub>r2</sub>      |                                                             | -    | -    | 500  | ns   |
| Output falling time                        | t <sub>f1</sub>      | T <sub>j</sub> =25°C, V <sub>BS</sub> =15V                  | -    | 25   | 200  | ns   |
|                                            | t <sub>f2</sub>      |                                                             | -    | -    | 400  | ns   |

## Application Information

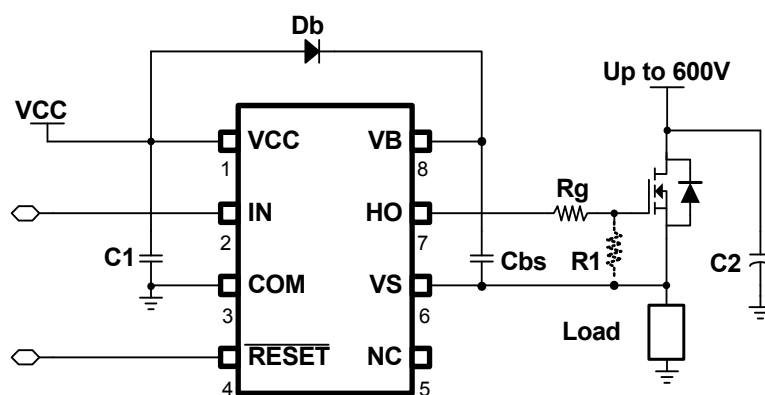
### 1. Relationship in input/output and supplies

| VCC        | VBS        | RESET | IN   | HO  |
|------------|------------|-------|------|-----|
| < VCCUVLO- | X          | X     | X    | OFF |
| X          | < VBSUVLO- | X     | X    | OFF |
| X          | X          | LOW   | X    | OFF |
| X          | X          | X     | LOW  | OFF |
| > VCCUVLO+ | > VBSUVLO+ | HIGH  | HIGH | ON  |

Notes:

X means independent from signal

## Typical Application Circuit



## Typical Waveforms

### 1. Input/Output Timing

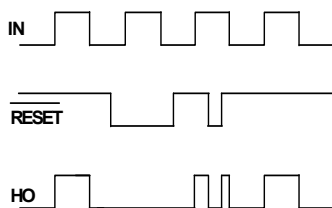


Figure 1a. Input/output Timing Diagram

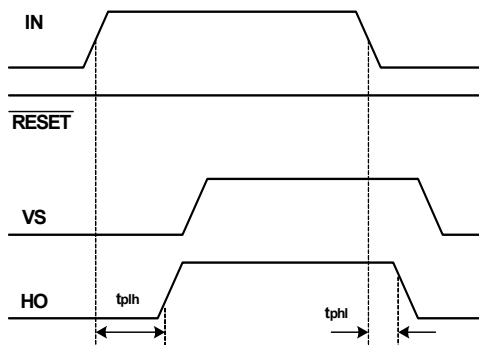


Figure 1b. Input(IN)/output Timing Diagram

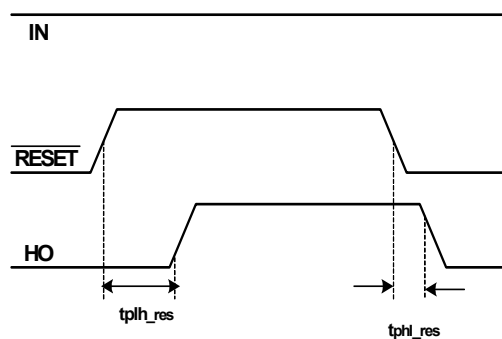


Figure 1c. Input(RESET)/output Timing Diagram

### 2. Output(HO) Switching Timing

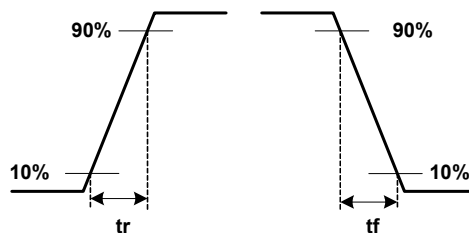


Figure 2. Switching Time Waveform Definitions

### 3.VB Drop Voltage Diagram

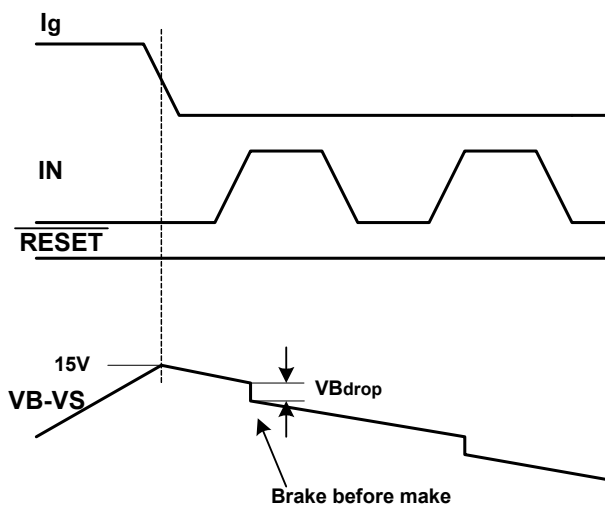


Figure 3a. VB Drop Voltage Diagram

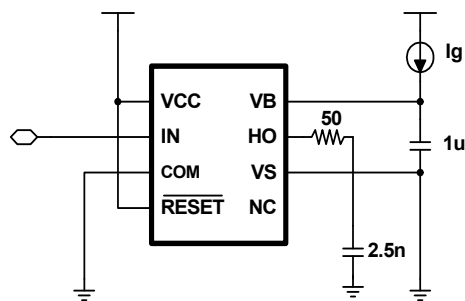


Figure3b. VB Drop Voltage Test Circuit

### 4.Recommendation Min. Short Pulse Width

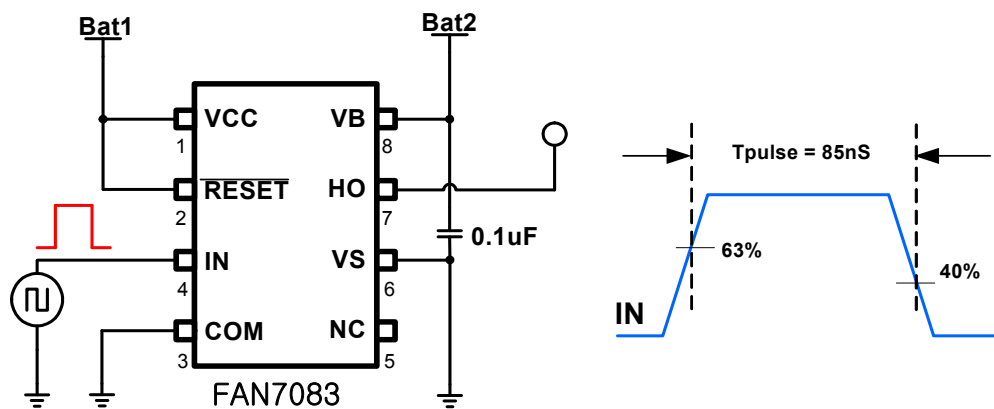


Figure 4a.Short Pulse Width Test Circuit and Pulse Width Waveform

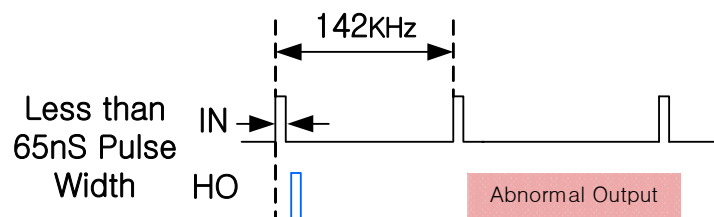


Figure 4b. Abnormal Output Waveform with short pulse width

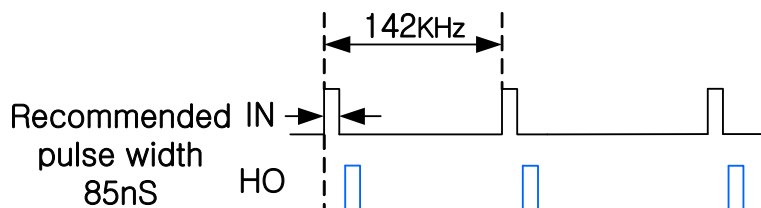


Figure 4c. Recommendation of pulse width Output Waveform

## Performance Graphs

This performance graphs based on ambient temperature  $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$

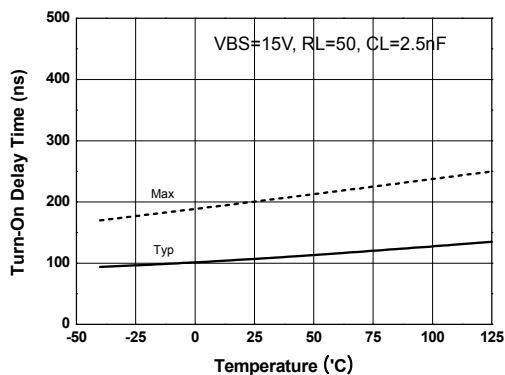


Figure 5a. Turn-On Delay Time vs Temperature

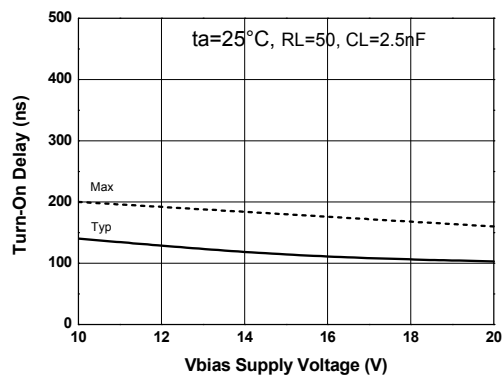


Figure 5b. Turn-On Delay Time vs VBS Supply Voltage

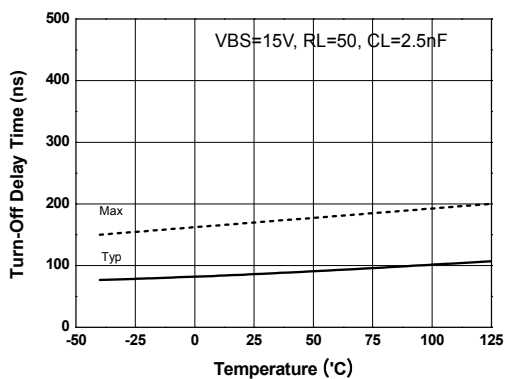


Figure 6a. Turn-Off Delay Time vs Temperature

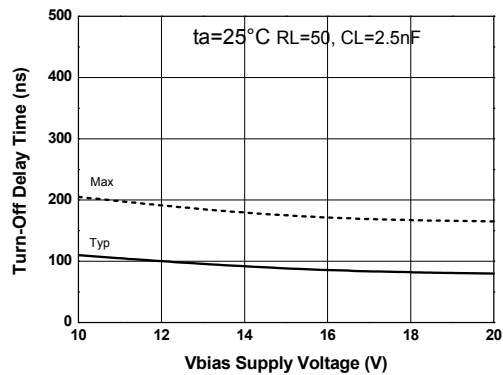


Figure 6b. Turn-Off Delay Time vs VBS Supply Voltage

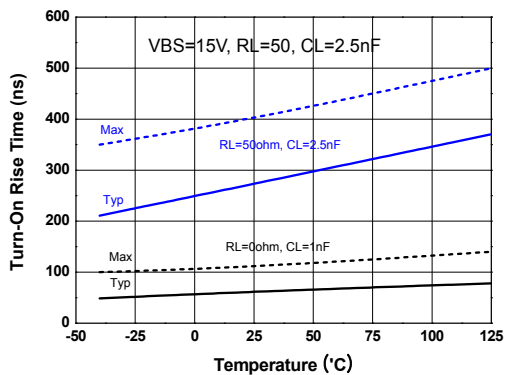


Figure 7a. Turn-On Rise Time vs Temperature

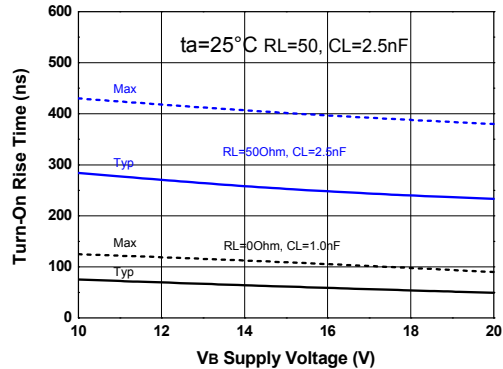


Figure 7b. Turn-On Rise Time vs VBS Supply Voltage

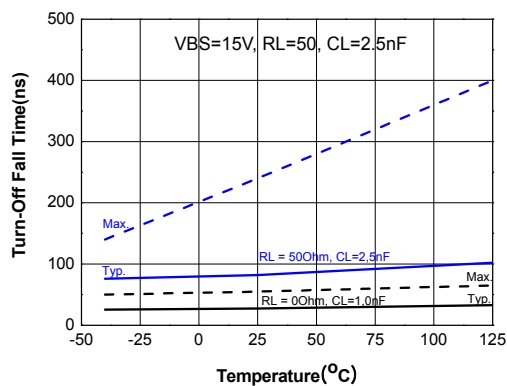


Figure 8a. Turn-Off Falling Time vs Temperature

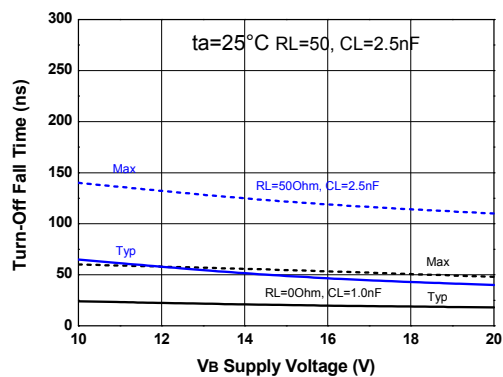


Figure 8b. Turn-Off Falling Time vs VBS Supply Voltage

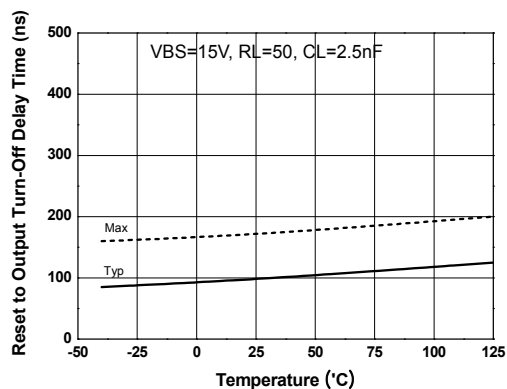


Figure 9a. RESET to output Turn-Off Delay Time vs Temperature

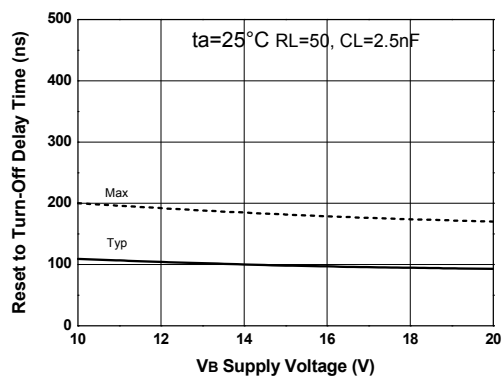


Figure 9b. RESET to output Turn-Off Delay Time vs VBS Supply

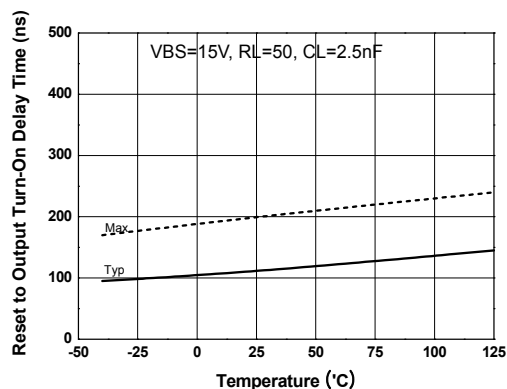


Figure 10a. RESET to output Turn-On Delay Time vs Temperature

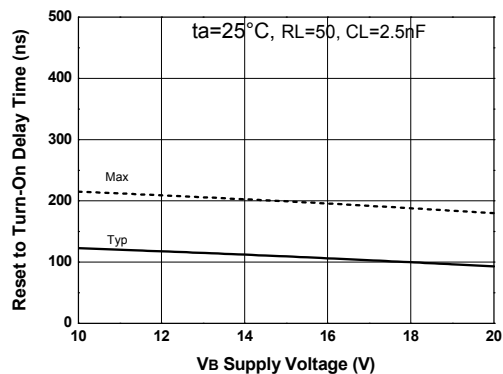


Figure 10b. RESET to output Turn-On Delay Time vs VBS Supply

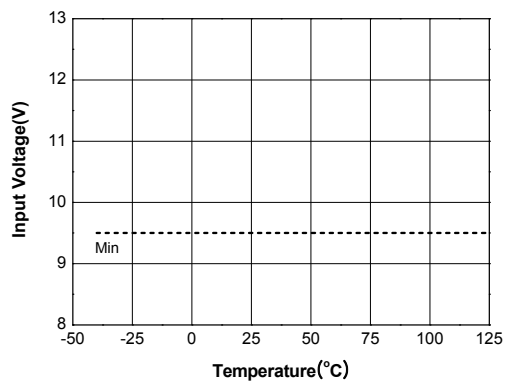


Figure 11a. Logic "1" IN Threshold vs Temperature

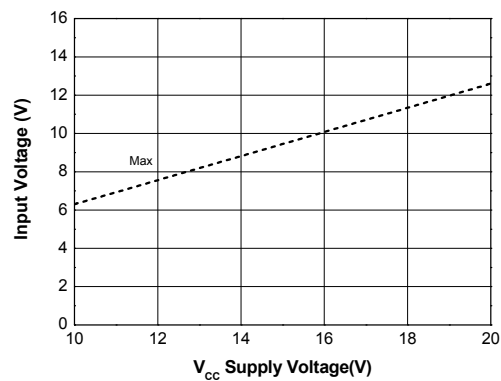


Figure 11b. Logic "1" IN Threshold vs VCC Supply Voltage

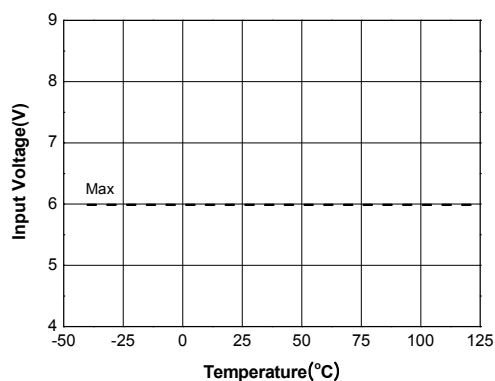


Figure 12a. Logic "0" IN Threshold vs Temperature

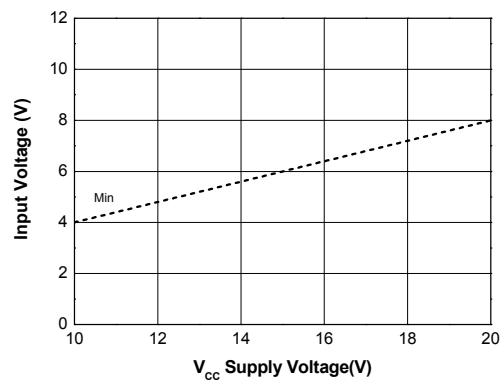


Figure 12b. Logic "0" IN Threshold vs VCC Supply Voltage

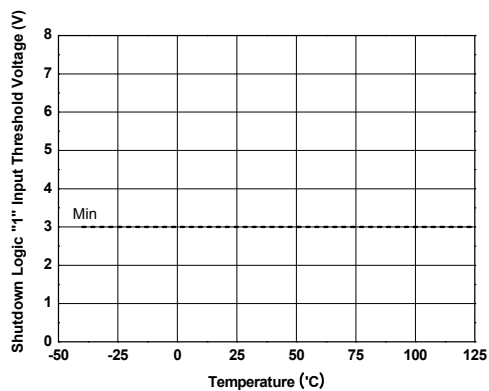


Figure 13a. Logic "1" Reset Threshold vs Temperature

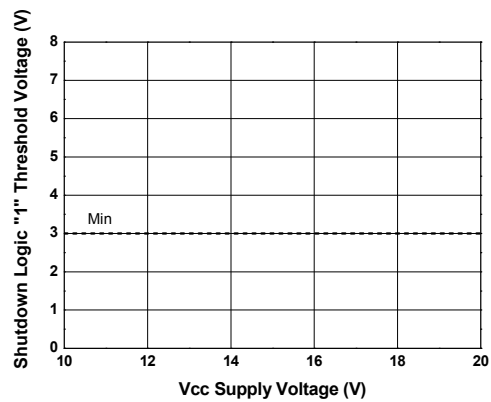


Figure 13b. Logic "1" Reset Threshold vs VCC Supply Voltage

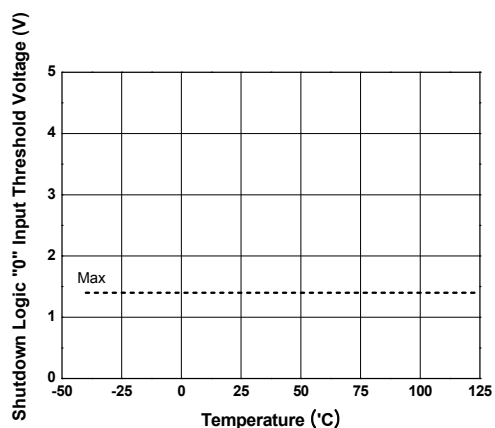


Figure 14a. Logic "0" Reset Threshold vs Temperature

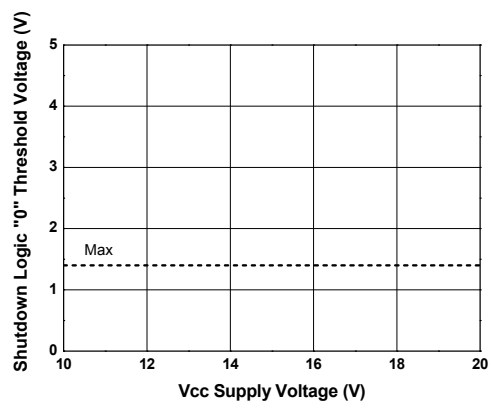


Figure 14b. Logic "0" Reset Threshold vs VCC Supply Voltage

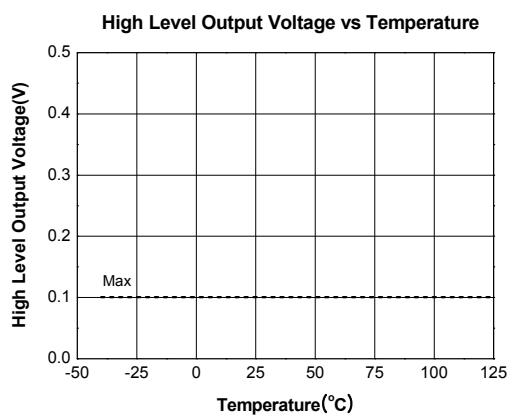


Figure 15a. High Level Output vs Temperature

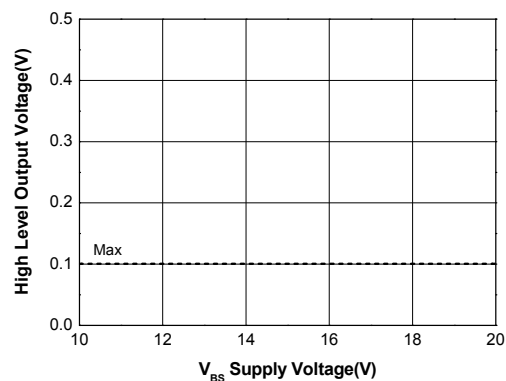


Figure 15b. High Level Output vs VBS Supply Voltage

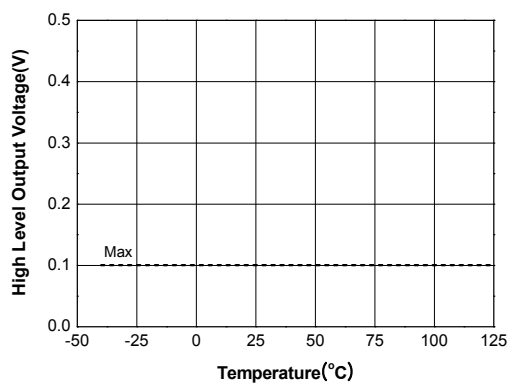


Figure 16a. Low Level Output vs Temperature

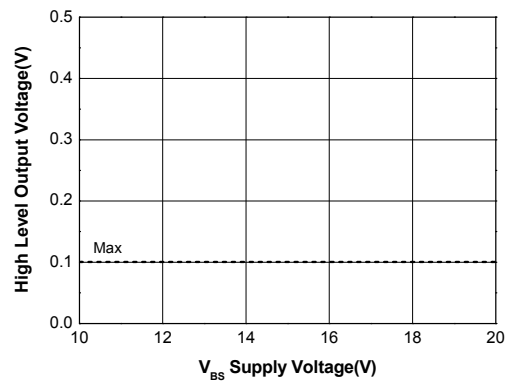


Figure 16b. Low Level Output vs VBS Supply Voltage

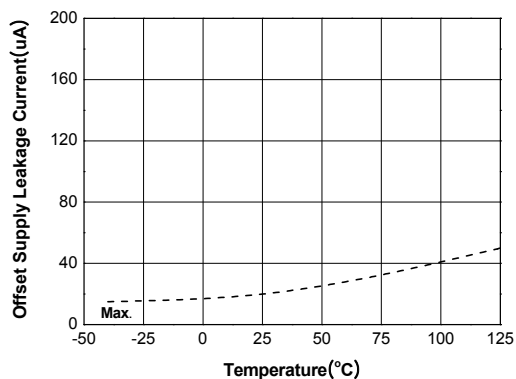


Figure 17a. Offset Supply Leakage vs Temperature

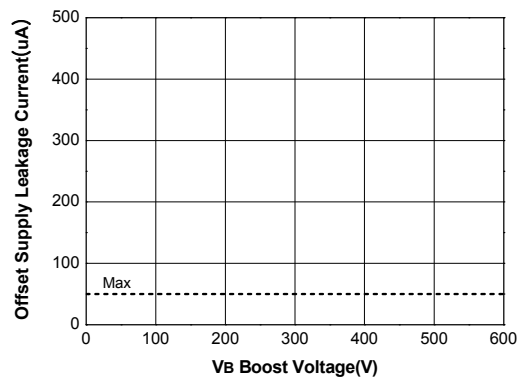


Figure 17b. Offset Supply Leakage vs Voltage

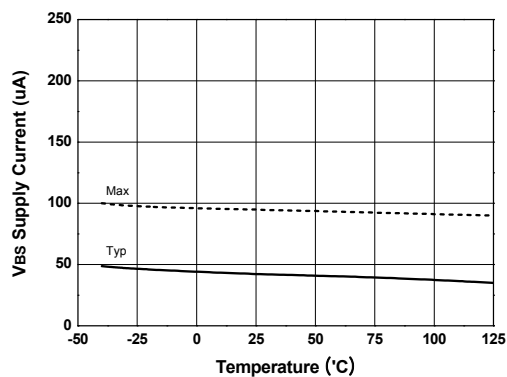


Figure 18a. VBS Supply Current vs Temperature

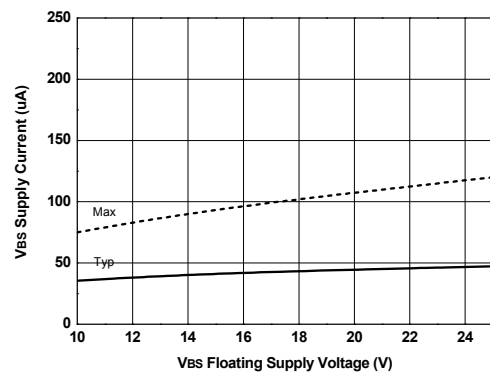


Figure 18b. VBS Supply Current vs VBS Supply Voltage

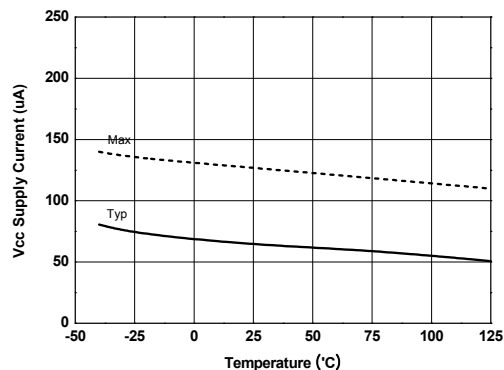


Figure 19a. VCC supply Current vs Temperature

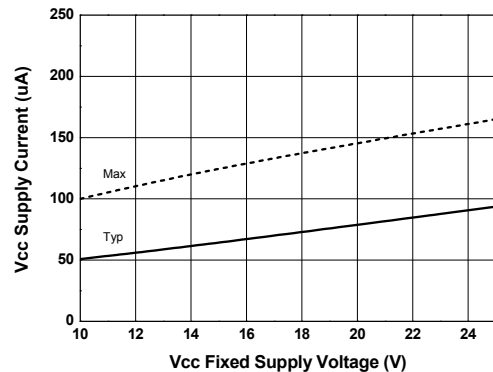


Figure 19b. VCC supply Current vs VCC Supply Voltage

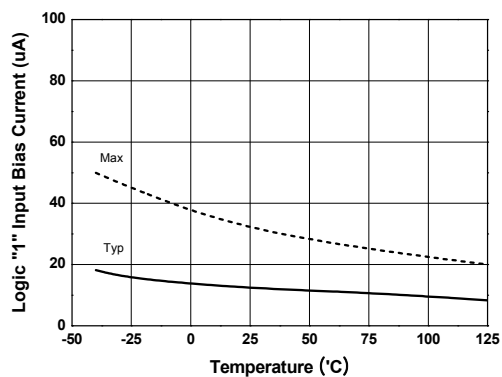


Figure 20a. Logic "1" IN Current vs Temperature

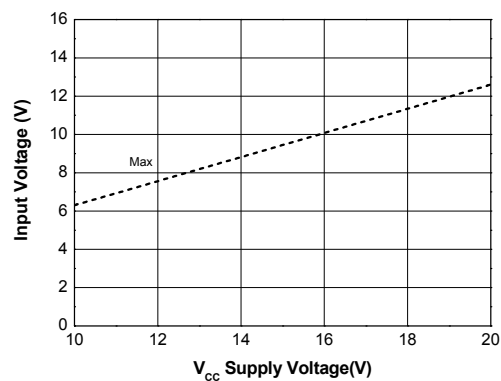


Figure 20b. Logic "1" IN Current vs Voltage

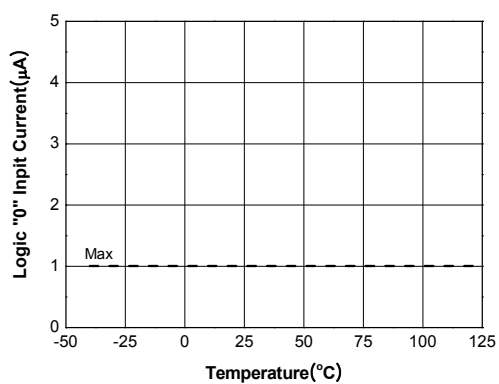


Figure21a. Logic "0" IN Current vs Temperature

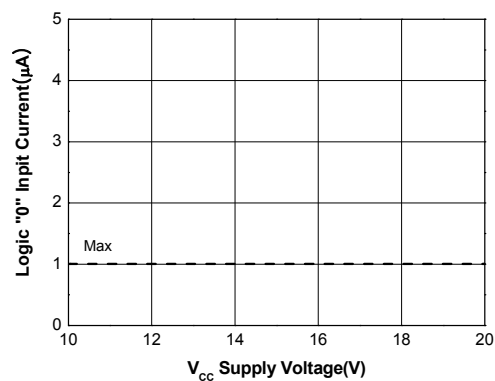


Figure 21b. Logic "0" IN Current vs Voltage

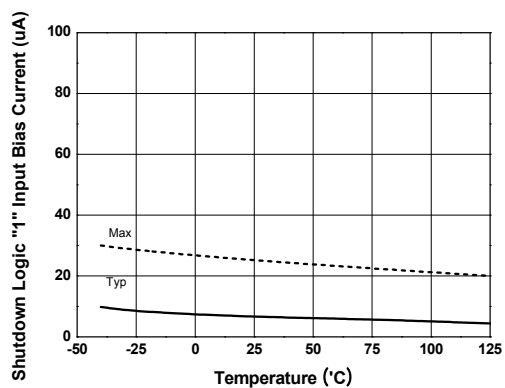


Figure 22. Logic "1" Reset Current vs Temperature

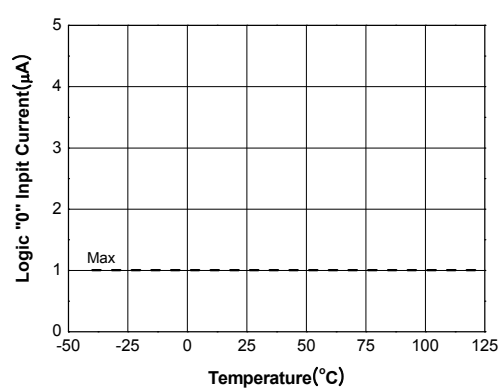


Figure 23. Logic "1" Reset Current vs Temperature

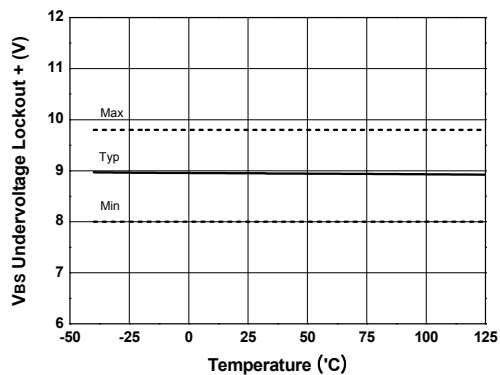


Figure 24a. VBS Undervoltage(+) vs Temperature

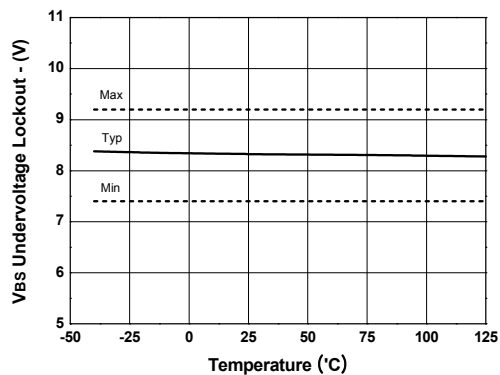


Figure 24b. VBS Undervoltage(-) vs Temperature

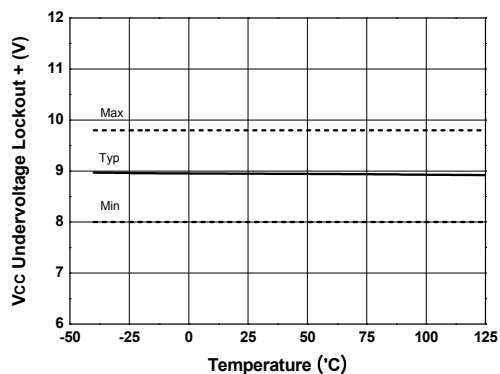


Figure 25a. VCC Undervoltage(+) vs Temperature

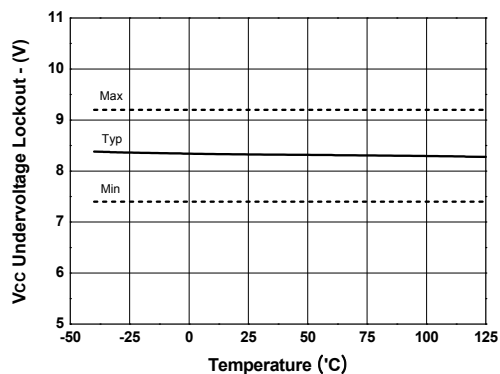


Figure 25b. VCC Undervoltage(-) vs Temperature

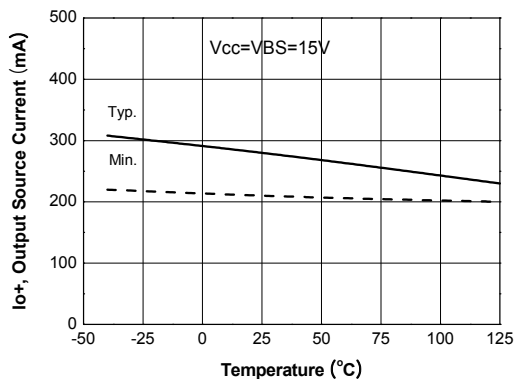


Figure 26a. Output Source Current vs Temperature

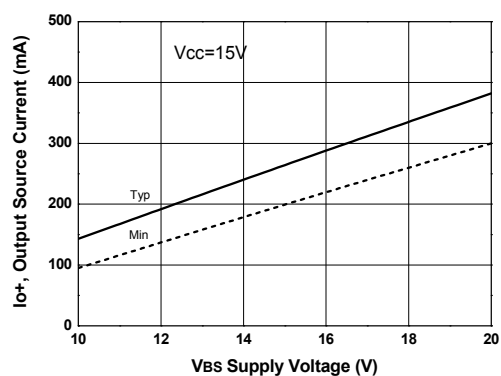


Figure 26b. Output Source Current vs Voltage

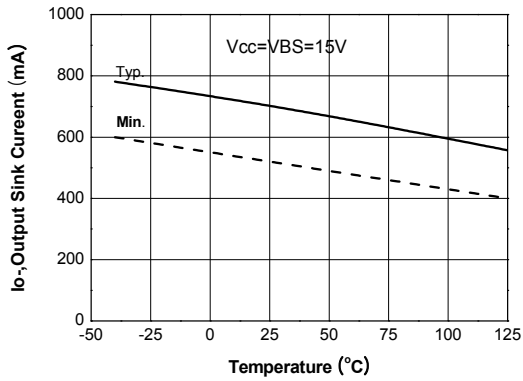


Figure 27a. Output Sink Current vs Temperature

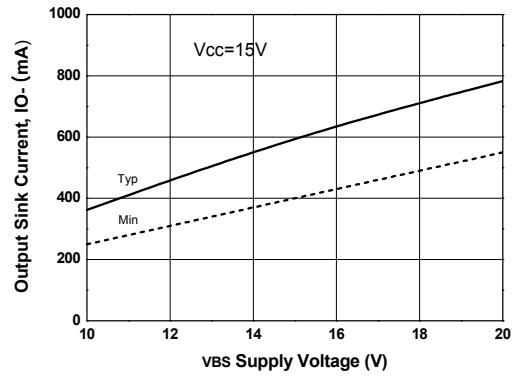


Figure 27b. Output Sink Current vs Voltage

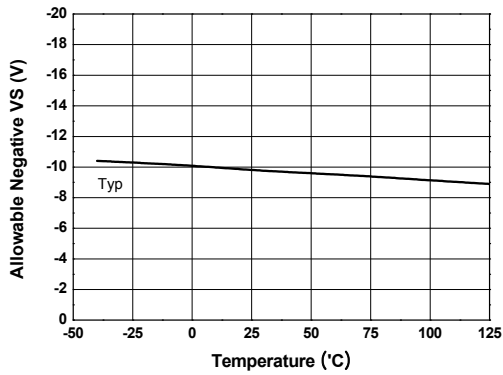


Figure 28a. Negative Allowable Offset vs Temperature

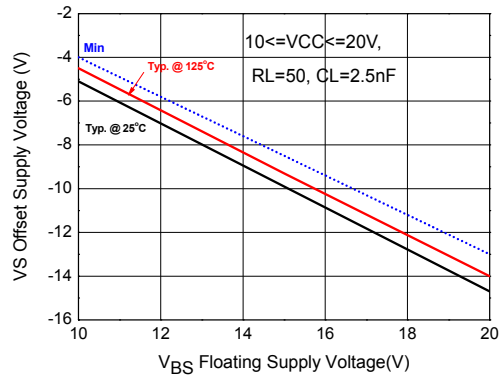


Figure 28b. Negative Allowable Offset vs Voltage

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910

**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local  
Sales Representative