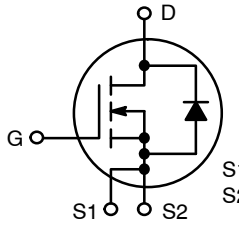
MOSFET – Power, N-Channel, SUPERFET III, Easy Drive

650 V, 30 A, 99 mΩ

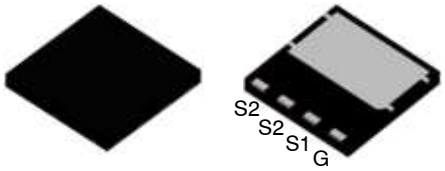
FCMT099N65S3

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	99 mΩ @ 10 V	30 A



S1: Driver Source
S2: Power Source

POWER MOSFET



PQFN4 8X8 2P
CASE 483AP

Description

SUPERFET III MOSFET is **onsemi**'s brand−new high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on−resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate. Consequently, SUPERFET III MOSFET is very suitable for the switching power applications such as server / telecom power, adaptor and solar inverter applications.

The Power88 package is an ultra−slim surface−mount package (1 mm high) with a low profile and small footprint (8x8 mm^2). SUPERFET III MOSFET in a Power88 package offers excellent switching performance due to lower parasitic source inductance and separated power and drive sources. Power88 offers Moisture Sensitivity Level 1 (MSL 1).

Features

- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 87 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 56 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 500 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies
- UPS / Solar

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot Code
FCMT099N65S3	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	DC	±30	V
		AC (f > 1 Hz)	±30	V
I_D	Drain Current	Continuous (T_C = 25°C)	30	A
		Continuous (T_C = 100°C)	19	
I_{DM}	Drain Current	Pulsed (Note 1)	75	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		145	mJ
I_{AS}	Avalanche Current (Note 1)		4.4	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		2.27	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	(T_C = 25°C)	227	W
		Derate Above 25°C	1.82	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 s		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 4.4 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 15 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.55	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 4)	45	

4. Device on 1 in^2 pad 2 oz copper pad on 1.5 x 1.5 in. board of FR−4 material.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Reel Size	Tape Width	Shipping†
FCMT099N65S3	FCMT099N65S3	PQFN8	–	–	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650			V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150°C	700			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C		0.68		V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V			10	μA
		V_{DS} = 520 V, T_C = 125°C		2.77		
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 0.7 mA	2.5		4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 15 A		87	99	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 15 A		17		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz		2270		pF
C_{oss}	Output Capacitance			50		pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		500		pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		74		pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 400 V, I_D = 15 A, V_{GS} = 10 V (Note 5)		56		nC
Q_{gs}	Gate to Source Gate Charge			13		nC
Q_{gd}	Gate to Drain “Miller” Charge			23		nC
ESR	Equivalent Series Resistance	f = 1 MHz		0.5		Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 15 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 5)		22		ns
t_r	Turn-On Rise Time			20		ns
$t_{d(off)}$	Turn-Off Delay Time			58		ns
t_f	Turn-Off Fall Time			5		ns
SOURCE-DRAIN DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source to Drain Diode Forward Current				30	A
I_{SM}	Maximum Pulsed Source to Drain Diode Forward Current				75	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 15 A			1.2	V
t_{rr}	Reverse Recovery Time	V_{DD} = 400 V, I_{SD} = 15 A, dI_F/dt = 100 A/μs		352		ns
Q_{rr}	Reverse Recovery Charge			6.5		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Essentially independent of operating temperature typical characteristics.

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TYPICAL PERFORMANCE CHARACTERISTICS

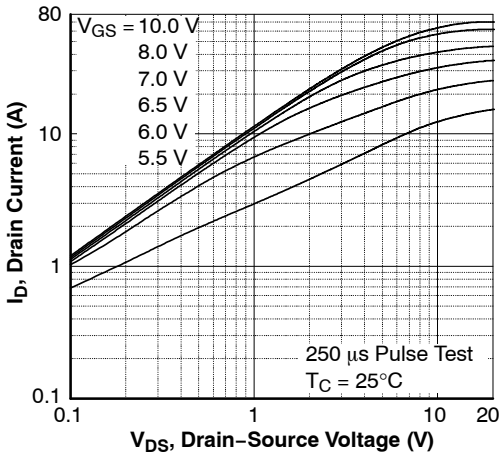


Figure 1. On−Region Characteristics

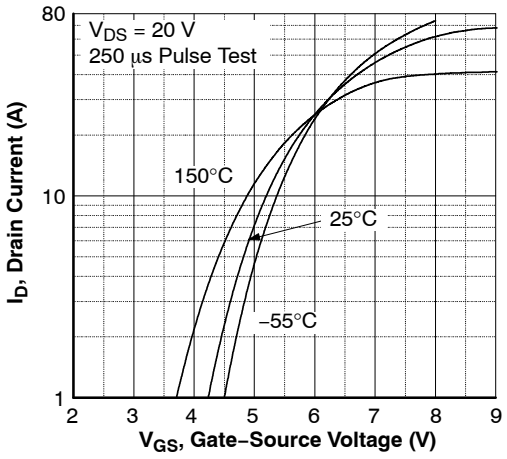


Figure 2. Transfer Characteristics

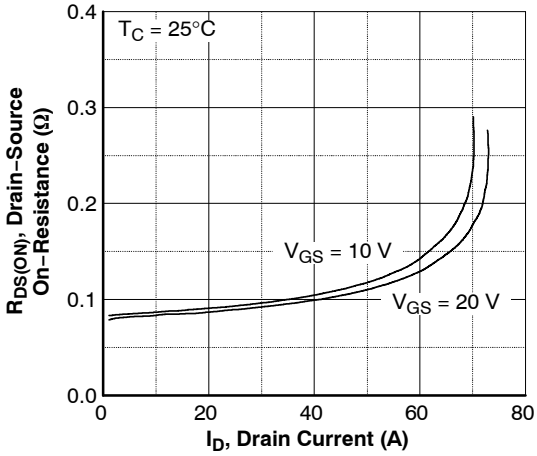


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

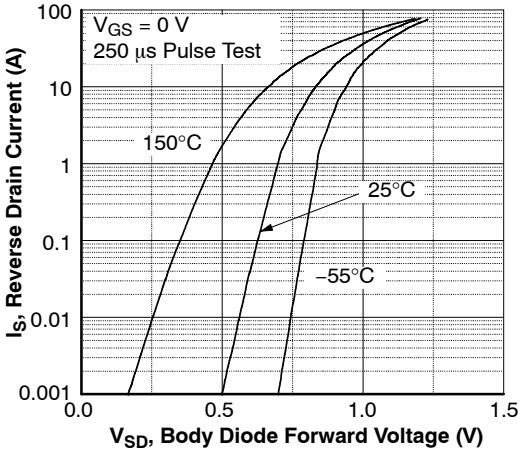


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

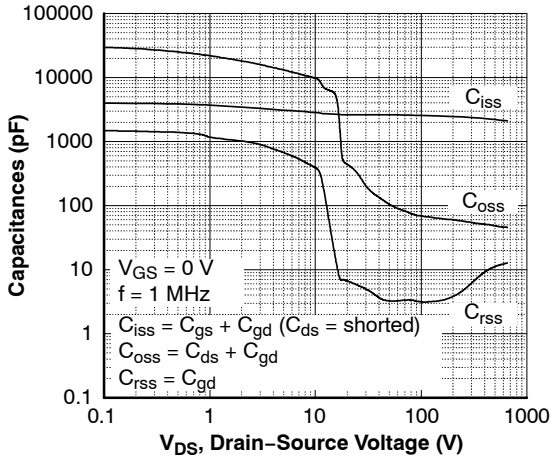


Figure 5. Capacitance Characteristics

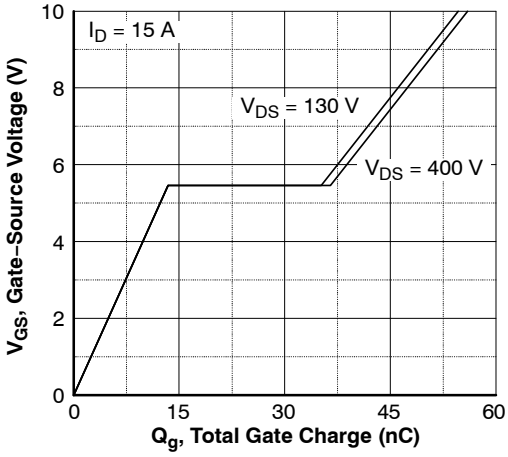


Figure 6. Gate Charge Characteristics

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

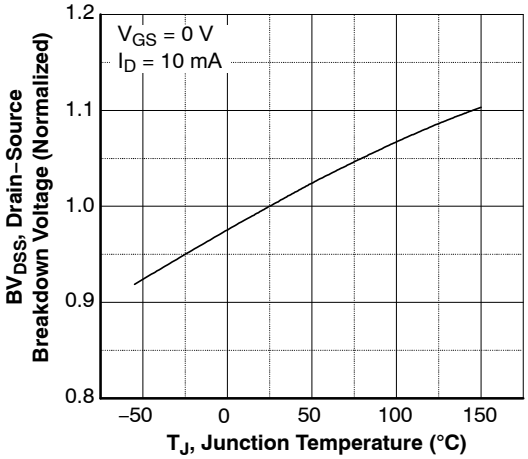


Figure 7. Breakdown Voltage Variation vs. Temperature

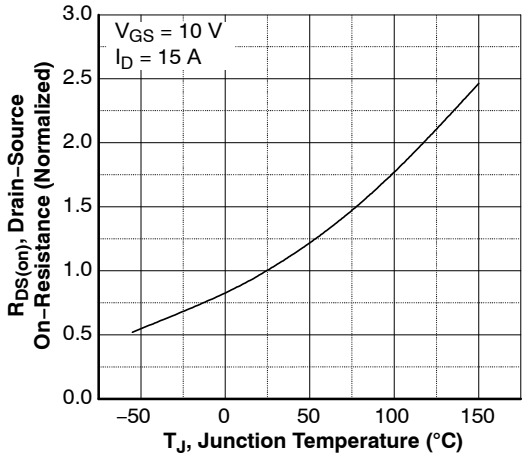


Figure 8. On−Resistance Variation vs. Temperature

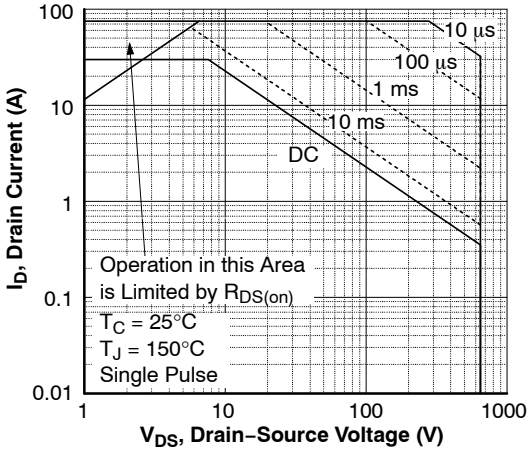


Figure 9. Maximum Safe Operating Area

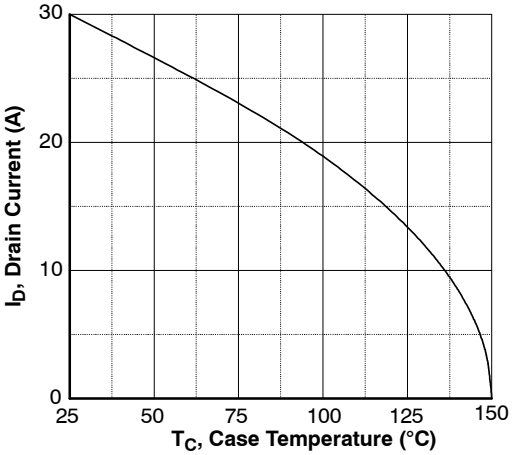


Figure 10. Maximum Drain Current vs. Case Temperature

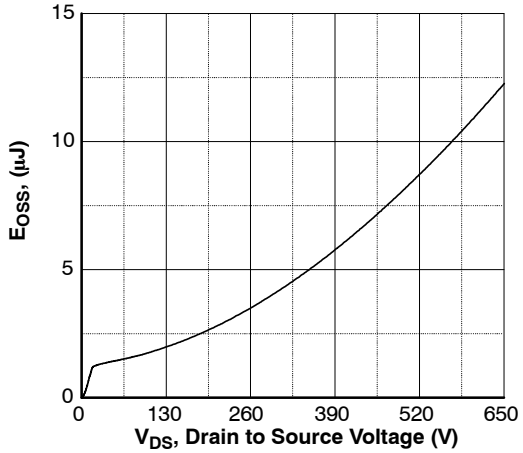


Figure 11. E_{OSS} vs. Drain to Source Voltage

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

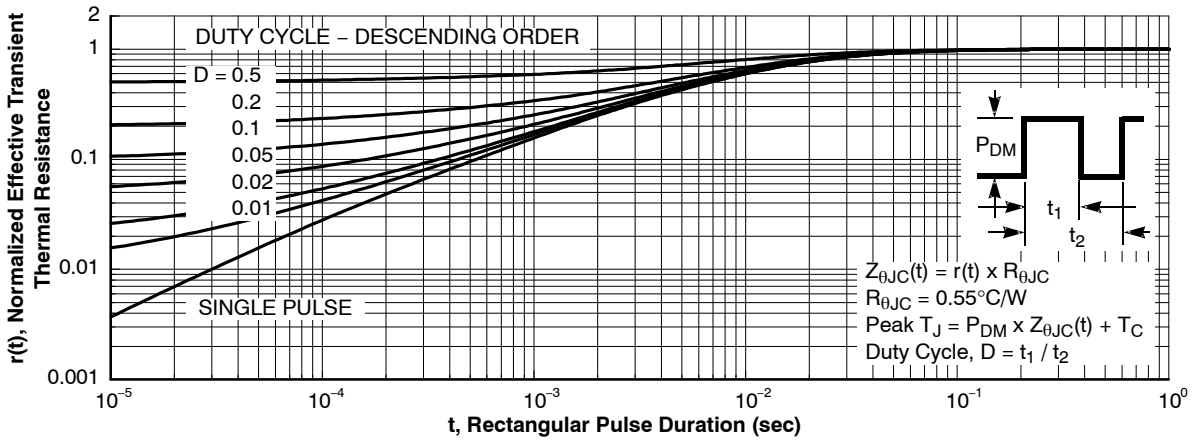


Figure 12. Transient Thermal Response Curve

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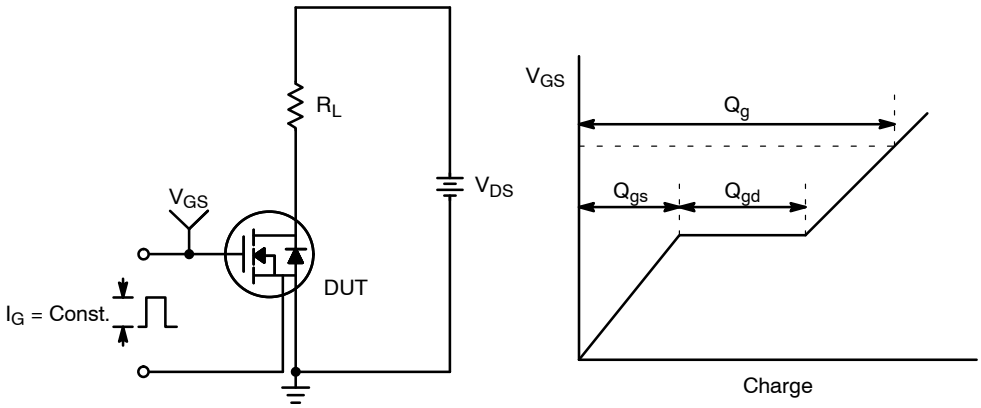


Figure 13. Gate Charge Test Circuit & Waveform

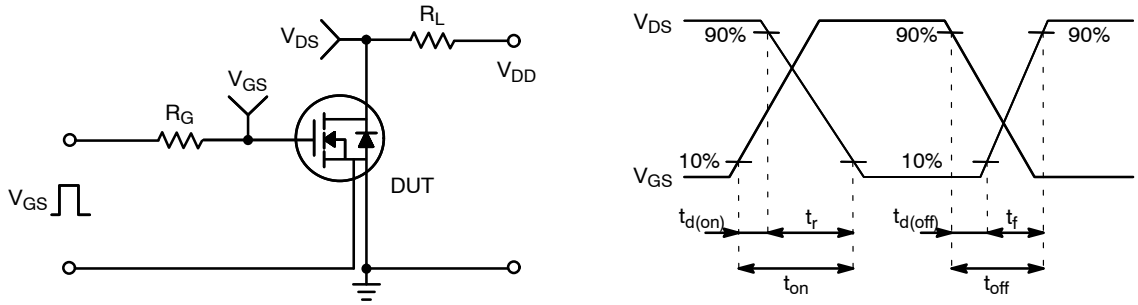


Figure 14. Resistive Switching Test Circuit & Waveforms

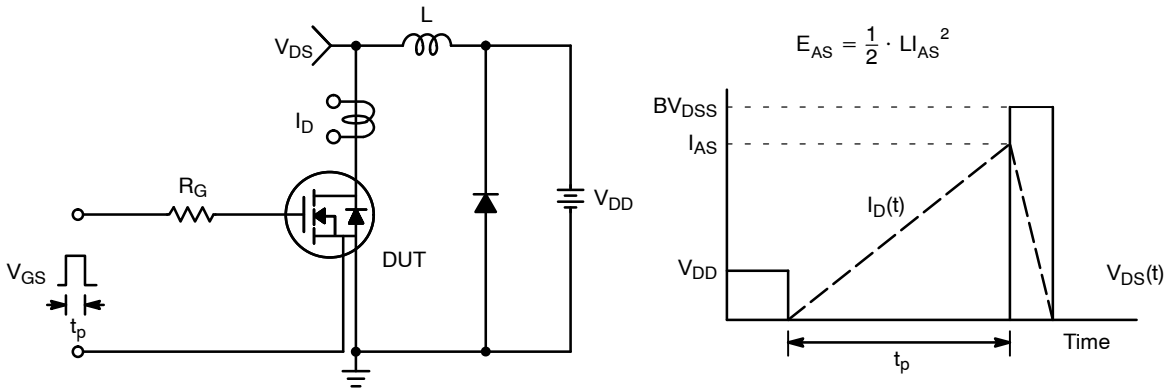


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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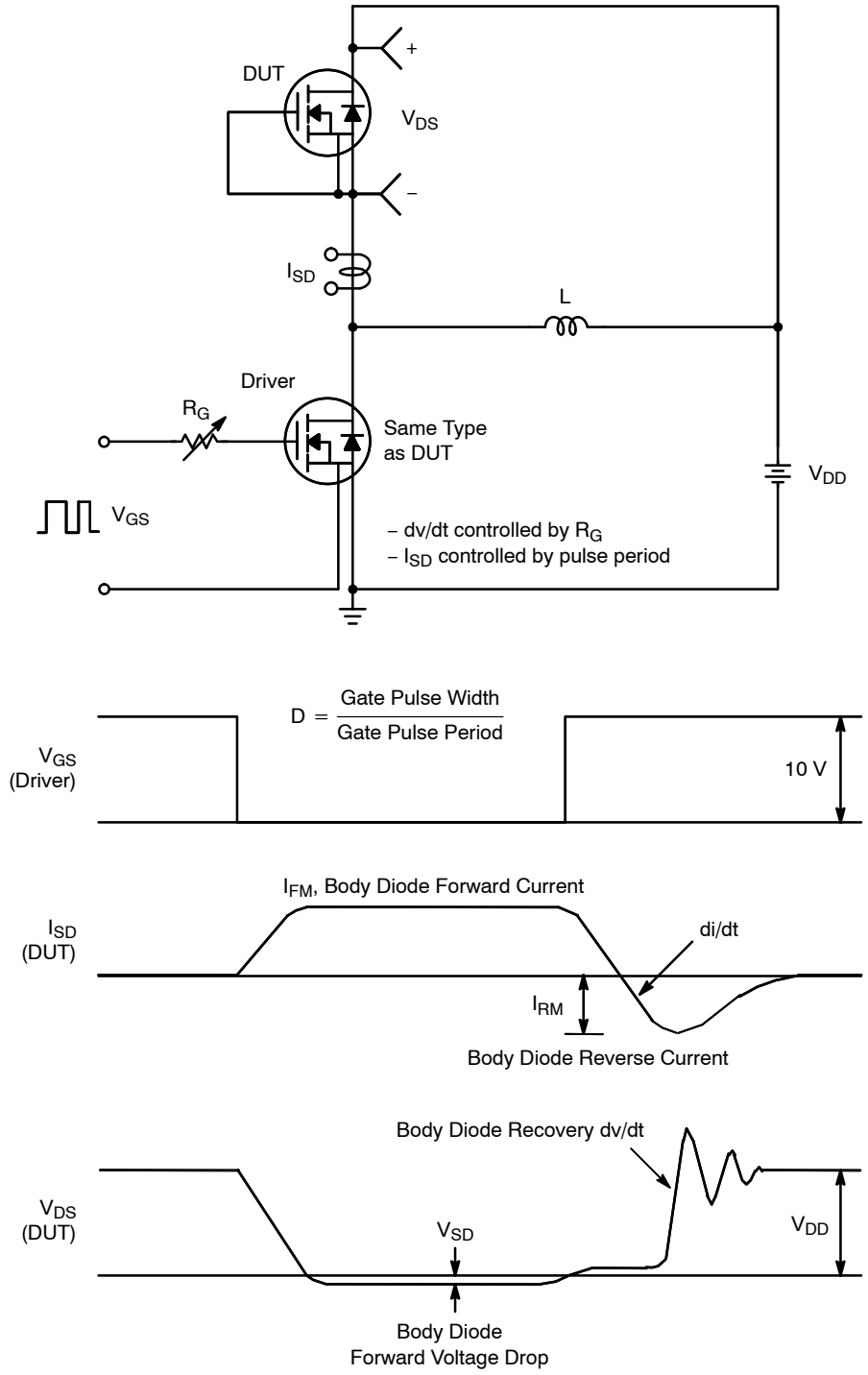


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

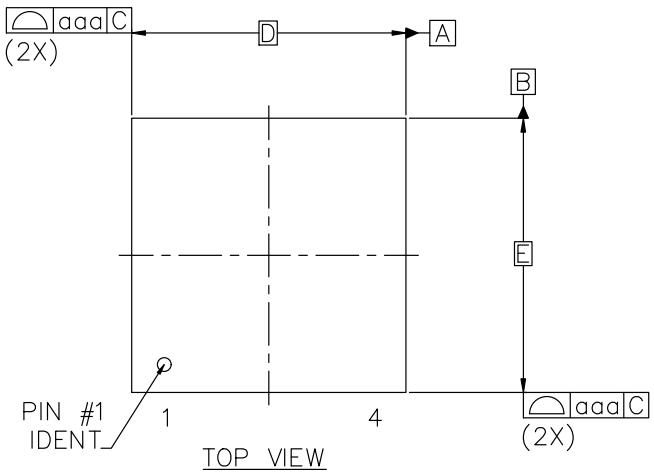
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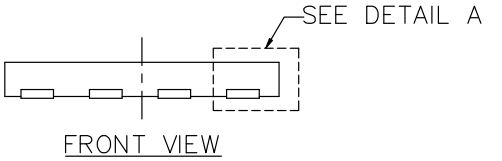
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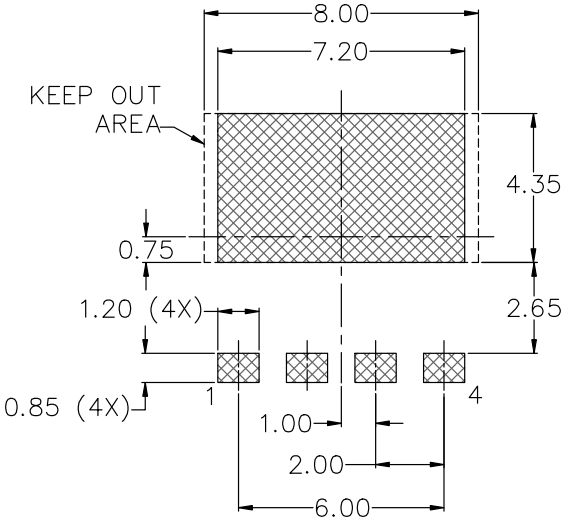


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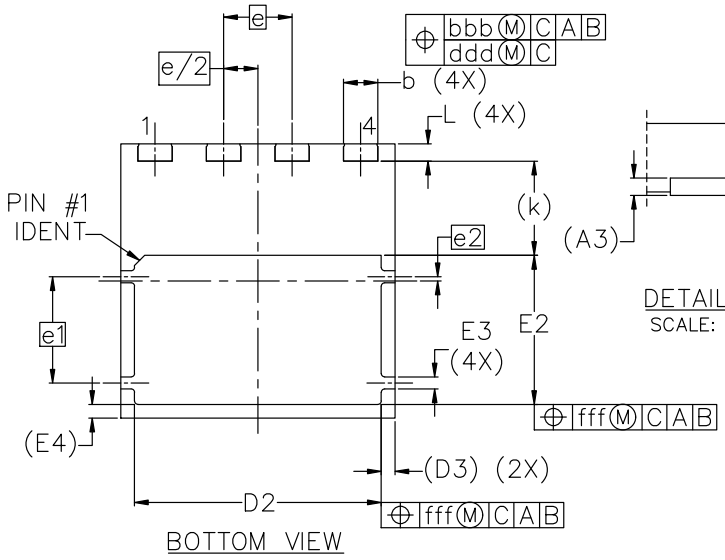
DATE 19 JUN 2026

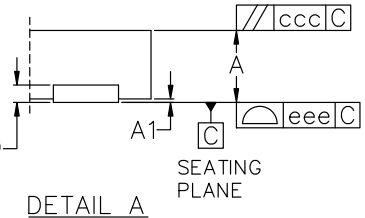






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DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	–	0.05
A3		0.20 REF	
b	0.90	1.00	1.10
D		8.00 BSC	
D2	7.10	7.20	7.30
D3		0.40 REF	
E		8.00 BSC	
E2	4.25	4.35	4.45
E3	0.25	0.35	0.45
E4		0.40 REF	
e		2.00 BSC	
e/2		1.00 BSC	
e1		3.10 BSC	
e2		0.125 BSC	
k		2.75 REF	
L	0.40	0.50	0.60
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5−2018.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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