# FDC2x1x-Q1 Multi-Channel, High Resolution Capacitance-to-Digital Converter for Capacitive Sensing Applications

## 1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C5
- EMI-resistant architecture
- Maximum output rates (one active channel):
  - 13.3kSPS (FDC2112-Q1, FDC2114-Q1)
  - 4.08kSPS (FDC2212-Q1, FDC2214-Q1)
- Maximum input capacitance: 250nF (at 10kHz with 1mH inductor)
- Sensor excitation frequency: 10kHz to 10MHz
- Number of channels: 2, 4
- Resolution: up to 28 bits
- RMS noise: 0.3fF at 100SPS and $f_{SENSOR}$ = 5MHz
- Supply voltage: 2.7V to 3.6V
- power consumption: active: 2.1mA
- Low-power sleep mode: 35µA
- Shutdown: 200nA
- Interface: $I^2C$
- Temperature range: –40°C to +125°C

## 2 Applications

- Proximity sensor
- Gesture recognition
- Automotive door / kick sensors
- Level sensor for conductive liquids

## 3 Description

Capacitive sensing is a low-power, high-resolution contactless sensing technique that can be applied to a variety of applications ranging from proximity detection to gesture recognition. The sensor in a capacitive sensing system is any metal or conductor, allowing for highly flexible system design.

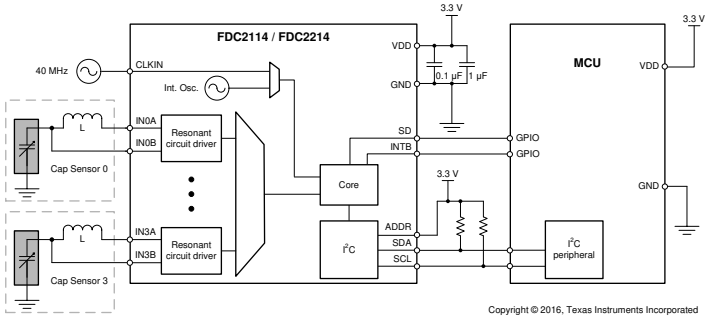
The main challenge limiting sensitivity in capacitive sensing applications is noise susceptibility of the sensors. With the FDC2x1x-Q1 resonant sensing architecture, performance can be maintained even in presence of fluorescent light.

The FDC2x1x-Q1 is a multi-channel family of high-resolution, high-speed capacitance-to-digital converters for implementing capacitive sensing solutions. The devices employ an innovative narrow-band based architecture to offer high rejection of noise while providing high resolution at high speed. The devices support a wide excitation frequency range, offering flexibility in system design.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| FDC2112-Q1 | DNT (WSON, 12) | 4mm × 4mm |
| FDC2114-Q1 | RGH (WQFN, 16) | 4mm × 4mm |
| FDC2212-Q1 | DNT (WSON, 12) | 4mm × 4mm |
| FDC2214-Q1 | RGH (WQFN, 16) | 4mm × 4mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Simplified Schematic**

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# 4 Pin Configuration and Functions

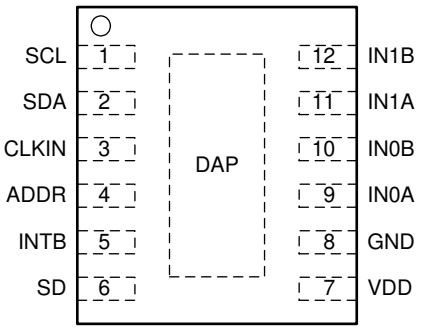



**Figure 4-1. FDC2112/FDC2212 DNT Package 12-Pin WSON Top View**

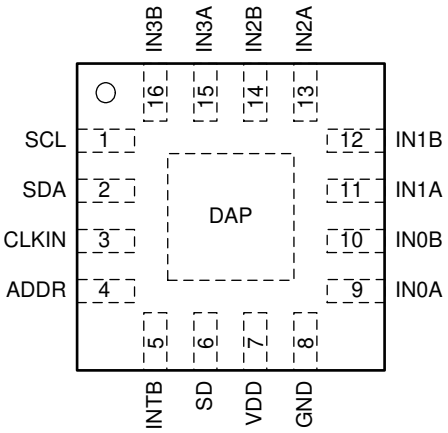



**Figure 4-2. FDC2114/FDC2214 RGH Package 16-Pin WQFN Top View**

**Table 4-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | SCL | I | $I^2C$ clock input |
| 2 | SDA | I/O | 12C data input/output |
| 3 | CLKIN | I | Controller Clock input. Tie this pin to GND if internal oscillator is selected |
| 4 | ADDR | I | $I^2C$ Address selection pin: when ADDR=L, $I^2C$ address = 0x2A, when ADDR=H, $I^2C$ address = 0x2B. |
| 5 | INTB | O | Configurable Interrupt output pin |
| 6 | SD | I | Shutdown input |
| 7 | VDD | P | Power Supply |
| 8 | GND | G | Ground |
| 9 | IN0A | A | Capacitive sensor input 0 |
| 10 | IN0B | A | Capacitive sensor input 0 |
| 11 | IN1A | A | Capacitive sensor input 1 |
| 12 | IN1B | A | Capacitive sensor input 1 |
| 13 | IN2A | A | Capacitive sensor input 2 (FDC2114 / FDC2214 only) |
| 14 | IN2B | A | Capacitive sensor input 2 (FDC2114 / FDC2214 only) |
| 15 | IN3A | A | Capacitive sensor input 3 (FDC2114 / FDC2214 only) |
| 16 | IN3B | A | Capacitive sensor input 3 (FDC2114 / FDC2214 only) |
| DAP | DAP[2] | N/A | Connect to ground |

(1) I = Input, O = Output, P=Power, G=Ground, A=Analog
(2) There is an internal electrical connection between the exposed Die Attach Pad (DAP) and the GND pin of the device. Although the DAP can be left floating, connect the DAP to the same potential as the GND pin of the device for best performance. Do not use the DAP as the primary ground for the device. The device GND pin must always be connected to ground.

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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| VDD | Supply voltage | | 5 | V |
| Vi | Voltage on any pin | –0.3 | VDD + 0.3 | V |
| IA | Input current on any INx pin | –8 | 8 | mA |
| ID | Input current on any digital pin | –5 | 5 | mA |
| $T_J$ | Junction temperature | –55 | 150 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011 | ±750 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

Unless otherwise specified, all limits ensured for $T_A$ = 25°C, VDD = 3.3V

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VDD | Supply voltage | 2.7 | | 3.6 | V |
| $T_A$ | Operating temperature | –40 | | 125 | °C |

## 5.4 Thermal Information

| THERMAL METRIC(1) | | FDC2112 / FDC2212 | FDC2214 / FDC2214 | UNIT |
|---|---|---|---|---|
| | | DNT (WSON) | RGH (WQFN) | |
| | | 12 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 36.7 | 35.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 36.2 | 36.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 14 | 13.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.4 | 0.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 14.2 | 13.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 3.5 | 3.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.


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## 5.5 Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_A$ = 25°C, VDD = 3.3V[1]

| PARAMETER | | TEST CONDITIONS[2] | MIN[3] | TYP[4] | MAX[3] | UNIT |
|---|---|---|---|---|---|---|
| **POWER** | | | | | | |
| $V_{DD}$ | Supply voltage | $T_A$ = –40°C to 125°C | 2.7 | | 3.6 | V |
| $I_{DD}$ | Supply current (not including sensor current)[5] | CLKIN = 10MHz[6] | | 2.1 | | mA |
| $I_{DDSL}$ | Sleep mode supply current[5] | | | 35 | 60 | µA |
| $I_{SD}$ | Shutdown mode supply current[5] | | | 0.2 | 1 | µA |
| **CAPACITIVE SENSOR** | | | | | | |
| $C_{SENSORMAX}$ | Maximum sensor capacitance | 1-mH inductor, 10kHz oscillation | | 250 | | nF |
| $C_{IN}$ | Sensor pin parasitic capacitance | | | 4 | | pF |
| $N_{BITS}$ | Number of bits | FDC2112, FDC2114<br>RCOUNT ≥ 0x0400 | | | 12 | bits |
| | | FDC2212, FDC2214<br>RCOUNT = 0xFFFF | | | 28 | bits |
| $f_{CS}$ | Maximum channel sample rate | FDC2112, FDC2114<br>single active channel continuous conversion, SCL = 400kHz | | | 13.3 | kSPS |
| | | FDC2212, FDC2214<br>single active channel continuous conversion, SCL= 400kHz | | | 4.08 | kSPS |
| **EXCITATION** | | | | | | |
| $f_{SENSOR}$ | Sensor excitation frequency | $T_A$ = –40°C to 125°C | 0.01 | | 10 | MHz |
| $V_{SENSORMIN}$ | Minimum sensor oscillation amplitude (pk)[7] | | | 1.2 | | V |
| $V_{SENSORMAX}$ | Maximum sensor oscillation amplitude (pk) | | | 1.8 | | V |
| $I_{SENSORMAX}$ | Sensor maximum current drive | HIGH_CURRENT_DRV = b0<br>DRIVE_CURRENT_CH0 = 0xF800 | | 1.5 | | mA |
| | | HIGH_CURRENT_DRV = b1<br>DRIVE_CURRENT_CH0 = 0xF800<br>Channel 0 only | | 6 | | mA |

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Unless otherwise specified, all limits ensured for $T_A$ = 25°C, VDD = 3.3V(1)

| PARAMETER | | TEST CONDITIONS(2) | MIN(3) | TYP(4) | MAX(3) | UNIT |
|---|---|---|---|---|---|---|
| **CONTROLLER CLOCK** | | | | | | |
| $f_{CLKIN}$ | External controller clock input frequency (CLKIN) | $T_A$ = –40°C to 125°C | 2 | | 40 | MHz |
| $CLKIN_{DUTY_MIN}$ | External controller clock minimum acceptable duty cycle (CLKIN) | | | 40% | | |
| $CLKIN_{DUTY_MAX}$ | External controller clock maximum acceptable duty cycle (CLKIN) | | | 60% | | |
| $V_{CLKIN_LO}$ | CLKIN low voltage threshold | | | | $0.3V_{DD}$ | V |
| $V_{CLKIN_HI}$ | CLKIN high voltage threshold | | $0.7 \times V_{DD}$ | | | V |
| $f_{INTCLK}$ | Internal controller clock frequency range | | 35 | 43.4 | 55 | MHz |
| $T_{Cf_int_\mu}$ | Internal controller clock temperature coefficient mean | | | –13 | | ppm/°C |

(1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device can be permanently degraded, either mechanically or electrically.
(2) Register values are represented as either binary (b is the prefix to the digits), or hexadecimal (0x is the prefix to the digits). Decimal values have no prefix.
(3) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values can vary over time and also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(5) $I^2C$ read/write communication and pullup resistors current through SCL, SDA not included.
(6) Sensor capacitor: 1 layer, 20.9 × 13.9mm, Bourns CMH322522-180KL sensor inductor with L=18µH and 33pF 1% COG/NP0 Target: Grounded aluminum plate (176 × 123mm), Channel = Channel 0 (continuous mode) CLKIN = 40MHz, CHx_FIN_SEL = b10, CHx_FREF_DIVIDER = b00 0000 0001 CH0_RCOUNT = 0xFFFF, SETTLECOUNT_CH0 = 0x0100, DRIVE_CURRENT_CH0 = 0x7800.
(7) Lower $V_{SENSORMIN}$ oscillation amplitudes can be used, but will result in lower SNR.

## 5.6 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{SDWAKEUP}$ | Wake-up time from SD high-low transition to $I^2C$ readback | | | 2 | ms |
| $t_{SLEEPWAKEUP}$ | Wake-up time from sleep mode | | | 0.05 | ms |
| $t_{WD-TIMEOUT}$ | Sensor recovery time (after watchdog timeout) | | 5.2 | | ms |
| **$I^2C$ TIMING CHARACTERISTICS** | | | | | |
| $f_{SCL}$ | Clock frequency | 10 | | 400 | kHz |
| $t_{LOW}$ | Clock low time | 1.3 | | | µs |
| $t_{HIGH}$ | Clock high time | 0.6 | | | µs |
| $t_{HD;STA}$ | Hold time (repeated) START condition: after this period, the first clock pulse is generated | 0.6 | | | µs |
| $t_{SU;STA}$ | Setup time for a repeated START condition | 0.6 | | | µs |
| $t_{HD;DAT}$ | Data hold time | 0 | | | µs |
| $t_{SU;DAT}$ | Data setup time | 100 | | | ns |
| $t_{SU;STO}$ | Setup time for STOP condition | 0.6 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 1.3 | | | µs |
| $t_{VD;DAT}$ | Data valid time | | | 0.9 | µs |
| $t_{VD;ACK}$ | Data valid acknowledge time | | | 0.9 | µs |
| $t_{SP}$ | Pulse width of spikes that must be suppressed by the input filter(1) | | | 50 | ns |


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## 5.7 Switching Characteristics - I²C

Unless otherwise specified, all limits ensured for $T_A$ = 25°C, VDD = 3.3V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VOLTAGE LEVELS** | | | | | | |
| $V_{IH}$ | Input high voltage | | 0.7 × $V_{DD}$ | | | V |
| $V_{IL}$ | Input low voltage | | | | 0.3 × $V_{DD}$ | V |
| $V_{OL}$ | Output low voltage (3mA sink current) | | | | 0.4 | V |
| HYS | Hysteresis | | | 0.1 × $V_{DD}$ | | V |

(1) This parameter is specified by design and/or characterization and is not tested in production.

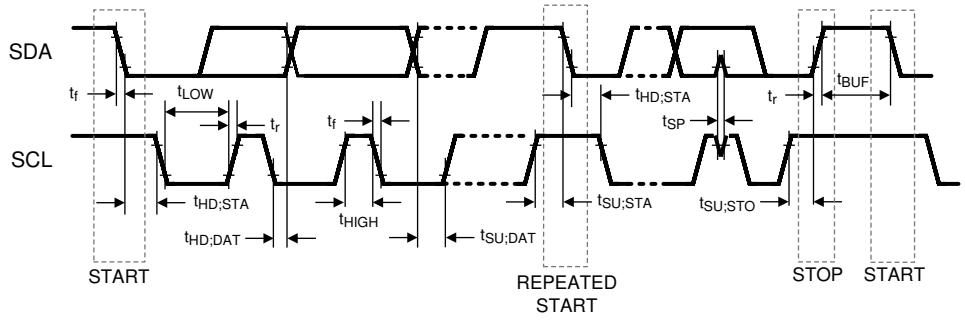
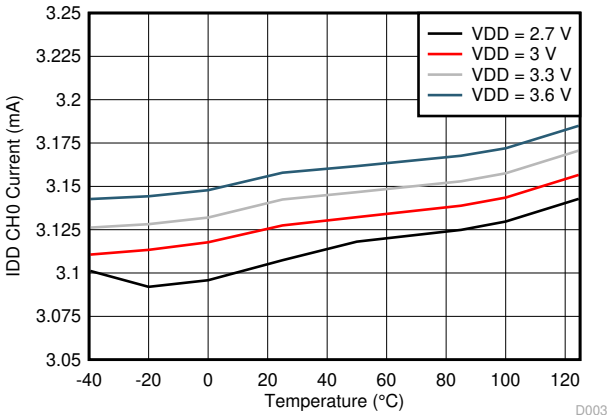



**Figure 5-1. I²C Timing**

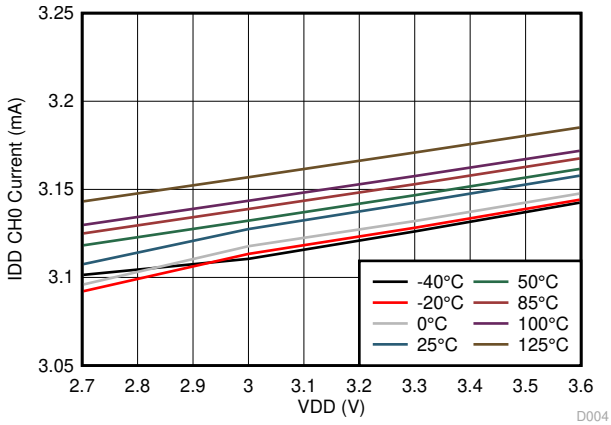
## 5.8 Typical Characteristics

*Common test conditions (unless specified otherwise):* Sensor capacitor: 1 layer, 20.9mm × 13.9mm, Bourns CMH322522-180KL sensor inductor with L = 18µH and 33pF 1% COG/NP0 Target: Grounded aluminum plate (176mm × 123mm), Channel = Channel 0 (continuous mode) CLKIN = 40MHz, CHx_FIN_SEL = b01, CHx_FREF_DIVIDER = b00 0000 0001 CH0_RCOUNT = 0xFFFF, SETTLECOUNT_CH0 = 0x0100, DRIVE_CURRENT_CH0 = 0x7800.



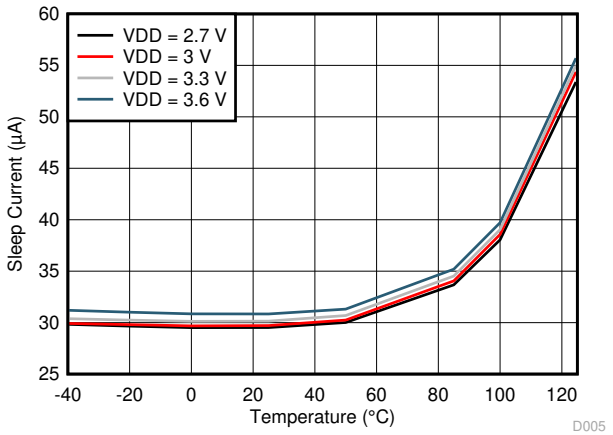

Includes 1.57mA sensor current
–40°C to +125°C

**Figure 5-2. Active Mode $I_{DD}$ vs Temperature**




Includes 1.57mA sensor current

**Figure 5-3. Active Mode $I_{DD}$ vs $V_{DD}$**




–40°C to +125°C

**Figure 5-4. Sleep Mode $I_{DD}$ vs Temperature**

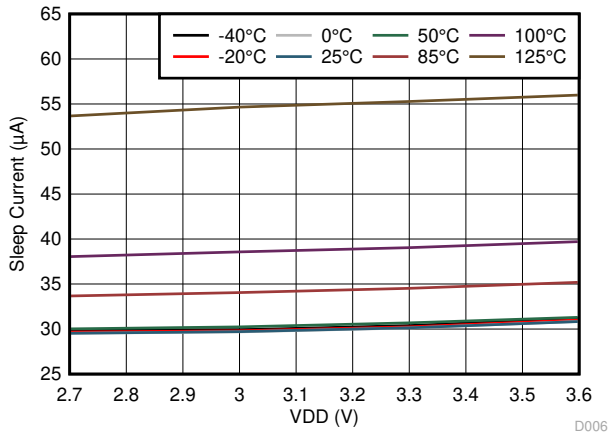
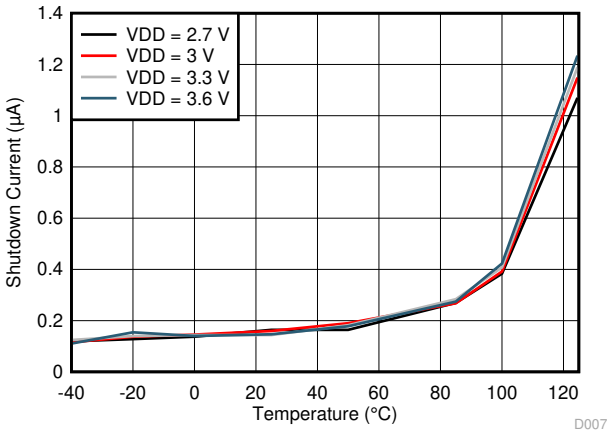



**Figure 5-5. Sleep Mode $I_{DD}$ vs $V_{DD}$**


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## 5.8 Typical Characteristics (continued)

*Common test conditions (unless specified otherwise):* Sensor capacitor: 1 layer, 20.9mm × 13.9mm, Bourns CMH322522-180KL sensor inductor with L = 18µH and 33pF 1% COG/NP0 Target: Grounded aluminum plate (176mm × 123mm), Channel = Channel 0 (continuous mode) CLKIN = 40MHz, CHx_FIN_SEL = b01, CHx_FREF_DIVIDER = b00 0000 0001 CH0_RCOUNT = 0xFFFF, SETTLECOUNT_CH0 = 0x0100, DRIVE_CURRENT_CH0 = 0x7800.




–40°C to +125°C

**Figure 5-6. Shutdown Mode $I_{DD}$ vs Temperature**

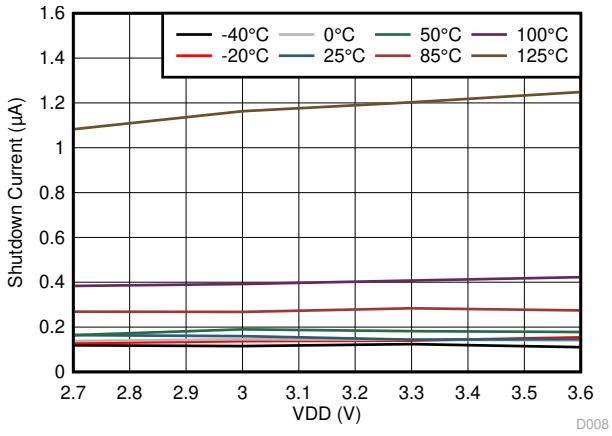
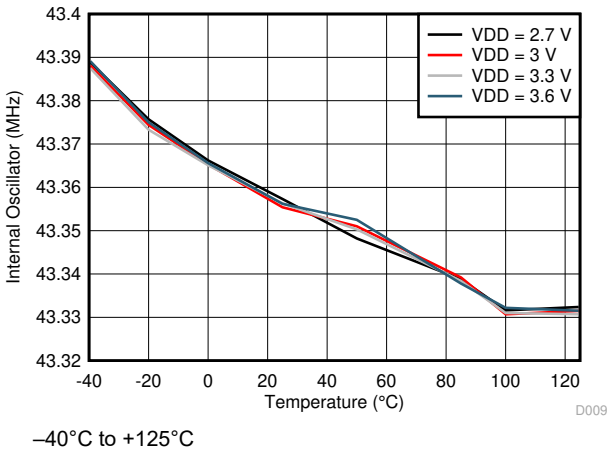
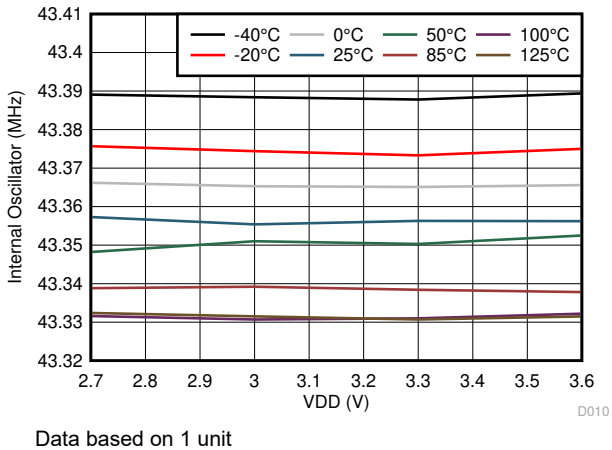



**Figure 5-7. Shutdown Mode $I_{DD}$ vs $V_{DD}$**




–40°C to +125°C

**Figure 5-8. Internal Oscillator Frequency vs Temperature**




Data based on 1 unit

**Figure 5-9. Internal Oscillator Frequency vs $V_{DD}$**

# 6 Detailed Description

## 6.1 Overview

The FDC2112, FDC2114, FDC2212, and FDC2214 are high-resolution, multichannel capacitance-to-digital converters for implementing capacitive sensing solutions. In contrast to traditional switched-capacitance architectures, the FDC2112, FDC2114, FDC2212, and FDC2214 employ an L-C resonator, also known as L-C tank, as a sensor. The narrow-band architecture allows unprecedented EMI immunity and greatly reduced noise floor when compared to other capacitive sensing solutions.

Using this approach, a change in capacitance of the L-C tank can be observed as a shift in the resonant frequency. Using this principle, the FDC is a capacitance-to-digital converter (FDC) that measures the oscillation frequency of an LC resonator. The device outputs a digital value that is proportional to frequency. This frequency measurement can be converted to an equivalent capacitance

## 6.2 Functional Block Diagrams

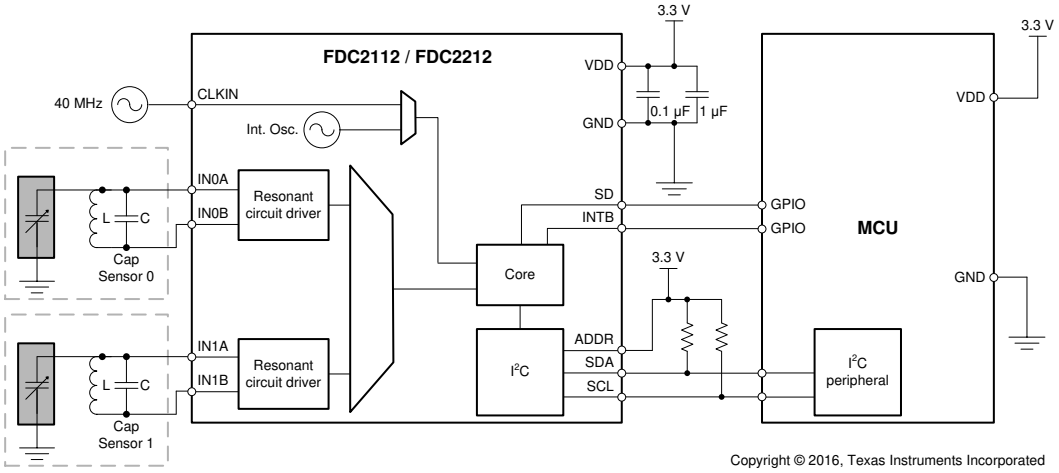



**Figure 6-1. Block Diagram for the FDC2112 and FDC2212**

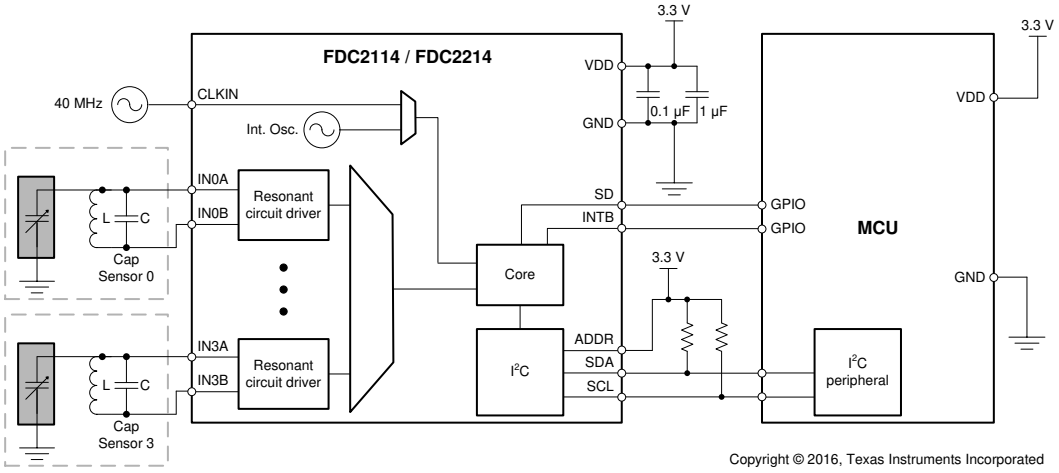



**Figure 6-2. Block Diagram for the FDC2114 and FDC2214**

The FDC is composed of front-end resonant circuit drivers, followed by a multiplexer that sequences through the active channels, connecting them to the core that measures and digitizes the sensor frequency ($f_{SENSOR}$). The core uses a reference frequency ($f_{REF}$) to measure the sensor frequency. $f_{REF}$ is derived from either an internal reference clock (oscillator), or an externally supplied clock. The digitized output for each channel is proportional to the ratio of $f_{SENSOR}/f_{REF}$. The $I^2C$ interface is used to support device configuration and to transmit the digitized

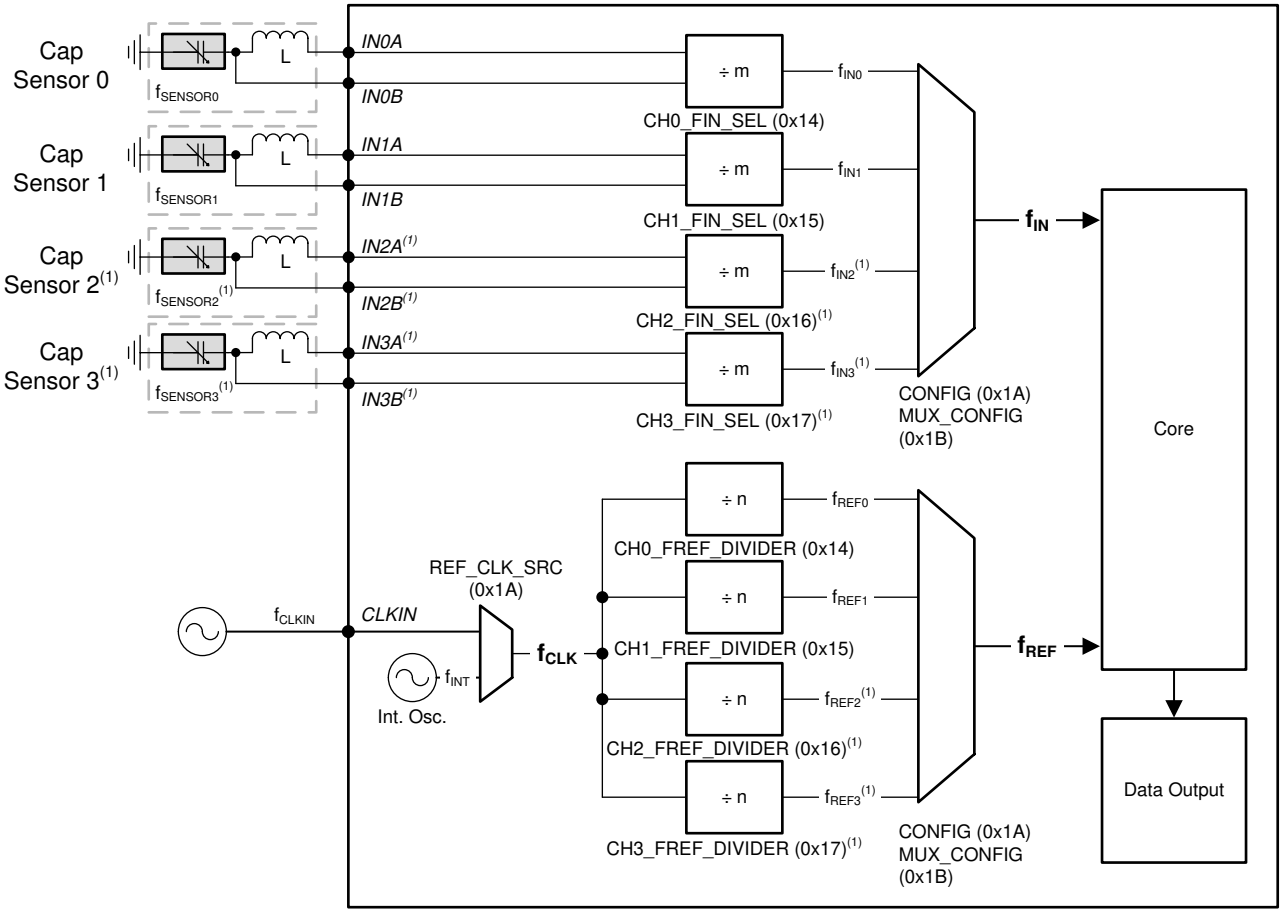

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frequency values to a host processor. The FDC can be placed in shutdown mode, saving current, using the SD pin. The INTB pin may be configured to notify the host of changes in system status.

## 6.3 Feature Description

### *6.3.1 Clocking Architecture*

Figure 6-3 shows the clock dividers and multiplexers of the FDC.




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A. FDC2114 / FDC2214 only

**Figure 6-3. Clocking Diagram**

In Figure 6-3, the key clocks are $f_{IN}$, $f_{REF}$, and $f_{CLK}$. $f_{CLK}$ is selected from either the internal clock source or external clock source (CLKIN). The frequency measurement reference clock, $f_{REF}$, is derived from the $f_{CLK}$ source. TI recommends that precision applications use an external controller clock that offers the stability and accuracy requirements needed for the application. The internal oscillator may be used in applications that require low cost and do not require high precision. The $f_{INx}$ clock is derived from sensor frequency for a channel x, $f_{SENSORx}$. $f_{REFx}$ and $f_{INx}$ must meet the requirements listed in Table 6-1, depending on whether $f_{CLK}$ (controller clock) is the internal or external clock.

**Table 6-1. Clock Configuration Requirements**

| MODE[1] | CLKIN SOURCE | VALID $f_{REFx}$ RANGE (MHz) | VALID $f_{INx}$ RANGE | SET CHx_FIN_SEL to [2] | SET CHx_SETTLECOUNT to | SET CHx_RCOUNT to |
|---|---|---|---|---|---|---|
| Multi-channel | Internal | $f_{REFx} \leq 55$ | $< f_{REFx}/4$ | Differential sensor configuration: b01: 0.01MHz to 8.75MHz (divide by 1) b10: 5MHz to 10MHz (divide by 2) Single-ended sensor configuration b10: 0.01MHz to 10MHz (divide by 2) | > 3 | > 8 |
| | External | $f_{REFx} \leq 40$ | | | | |
| Single-channel | Either external or internal | $f_{REFx} \leq 35$ | | | | |

(1) Channels 2 and 3 are only available for FDC2114 and FDC2214.
(2) Refer to *Sensor Configuration* for information on differential and single-ended sensor configurations.

Table 6-2 shows the clock configuration registers for all channels.

**Table 6-2. Clock Configuration Registers**

| CHANNEL[1] | CLOCK | REGISTER | FIELD [ BIT(S) ] | VALUE |
|---|---|---|---|---|
| All | $f_{CLK}$ = Controller Clock Source | CONFIG, addr 0x1A | REF_CLK_SRC [9] | b0 = internal oscillator is used as the controller clock<br>b1 = external clock source is used as the controller clock |
| 0 | $f_{REF0}$ | CLOCK_DIVIDERS_CH0, addr 0x14 | CH0_FREF_DIVIDER [9:0] | $f_{REF0} = f_{CLK}$ / CH0_FREF_DIVIDER |
| 1 | $f_{REF1}$ | CLOCK_DIVIDERS_CH1, addr 0x15 | CH1_FREF_DIVIDER [9:0] | $f_{REF1} = f_{CLK}$ / CH1_FREF_DIVIDER |
| 2 | $f_{REF2}$ | CLOCK_DIVIDERS_CH2, addr 0x16 | CH2_FREF_DIVIDER [9:0] | $f_{REF2} = f_{CLK}$ / CH2_FREF_DIVIDER |
| 3 | $f_{REF3}$ | CLOCK_DIVIDERS_CH3, addr 0x17 | CH3_FREF_DIVIDER [9:0] | $f_{REF3} = f_{CLK}$ / CH3_FREF_DIVIDER |
| 0 | $f_{IN0}$ | CLOCK_DIVIDERS_CH0, addr 0x14 | CH0_FIN_SEL [13:12] | $f_{IN0} = f_{SENSOR0}$ / CH0_FIN_SEL |
| 1 | $f_{IN1}$ | CLOCK_DIVIDERS_CH1, addr 0x15 | CH1_FIN_SEL [13:12] | $f_{IN1} = f_{SENSOR1}$ / CH1_FIN_SEL |
| 2 | $f_{IN2}$ | CLOCK_DIVIDERS_CH2, addr 0x16 | CH2_FIN_SEL [13:12] | $f_{IN2} = f_{SENSOR2}$ / CH2_FIN_SEL |
| 3 | $f_{IN3}$ | CLOCK_DIVIDERS_CH3, addr 0x17 | CH3_FIN_SEL [13:12] | $f_{IN3} = f_{SENSOR3}$ / CH3_FIN_SEL |

(1) Channels 2 and 3 are only available for FDC2114 and FDC2214

### *6.3.2 Multi-Channel and Single-Channel Operation*

The multi-channel package of the FDC enables the user to save board space and support flexible system design. For example, temperature drift can often cause a shift in component values, resulting in a shift in resonant frequency of the sensor. Using a second sensor as a reference provides the capability to cancel out a temperature shift. When operated in multi-channel mode, the FDC sequentially samples the active channels. In single-channel mode, the FDC samples a single channel, which is selectable. Table 6-3 shows the registers and values that are used to configure either multi-channel or single-channel modes.


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**Table 6-3. Single- and Multi-Channel Configuration Registers**

| MODE | REGISTER | FIELD [ BIT(S) ] | VALUE |
|---|---|---|---|
| Single channel | CONFIG, addr 0x1A | ACTIVE_CHAN [15:14] | 00 = chan 0 |
| | | | 01 = chan 1 |
| | | | 10 = chan 2 |
| | | | 11 = chan 3 |
| | MUX_CONFIG addr 0x1B | AUTOSCAN_EN [15] | 0 = continuous conversion on a single channel (default) |
| Multi-channel | MUX_CONFIG addr 0x1B | AUTOSCAN_EN [15] | 1 = continuous conversion on multiple channels |
| | MUX_CONFIG addr 0x1B | RR_SEQUENCE [14:13] | 00 = Ch0, Ch 1 |
| | | | 01 = Ch0, Ch 1, Ch 2 |
| | | | 10 = Ch0, CH1, Ch2, Ch3 |

The digitized sensor measurement for each channel (DATAx) represents the ratio of the sensor frequency to the reference frequency.

The data output (DATAx) of the FDC2112 and FDC2114 is expressed as the 12 MSBs of a 16-bit result:

$$DATA_x = \frac{f_{SENSORx} * 2^{12}}{f_{REFx}} \quad (1)$$

The data output (DATAx) of the FDC2212 and FDC2214 is expressed as:

$$DATA_x = \frac{f_{SENSORx} * 2^{28}}{f_{REFx}} \quad (2)$$

Table 6-4 lists the registers that contain the fixed point sample values for each channel.

**Table 6-4. Sample Data Registers**

| CHANNEL[2] | REGISTER[1] | FIELD NAME [ BITS(S) ] AND VALUE (FDC2112, FDC2114) | FIELD NAME [ BITS(S) ] AND VALUE (FDC2212, FDC2214) [3] [4] |
|---|---|---|---|
| 0 | DATA_CH0, addr 0x00 | DATA0 [11:0]:<br>12 bits of the 16 bit conversion result.<br>0x000 = under range<br>0xfff = over range | DATA0 [27:16]:<br>12 MSBs of the 28 bit conversion result |
| | DATA_LSB_CH0, addr 0x01 | Not applicable | DATA0 [15:0]:<br>16 LSBs of the 28 bit conversion result |
| 1 | DATA_CH1, addr 0x02 | DATA1 [11:0]:<br>12 bits of the 16 bit conversion result.<br>0x000 = under range<br>0xfff = over range | DATA1 [27:16]:<br>12 MSBs of the 28 bit conversion result |
| | DATA_LSB_CH1, addr 0x03 | Not applicable | DATA1 [15:0]:<br>16 LSBs of the 28 bit conversion result |
| 2 | DATA_CH2, addr 0x04 | DATA2 [11:0]:<br>12 bits of the 16 bit conversion result.<br>0x000 = under range<br>0xfff = over range | DATA2 [27:16]:<br>12 MSBs of the 28 bit conversion result |
| | DATA_LSB_CH2, addr 0x05 | Not applicable | DATA2 [15:0]:<br>16 LSBs of the 28 bit conversion result |

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**Table 6-4. Sample Data Registers (continued)**

| CHANNEL(2) | REGISTER(1) | FIELD NAME [ BITS(S) ] AND VALUE (FDC2112, FDC2114) | FIELD NAME [ BITS(S) ] AND VALUE (FDC2212, FDC2214) (3) (4) |
|---|---|---|---|
| 3 | DATA_CH3, addr 0x06 | DATA3 [11:0]:<br>12 bits of the 16 bit conversion result.<br>0x000 = under range<br>0xfff = over range | DATA3 [27:16]:<br>12 MSBs of the 28 bit conversion result |
| | DATA_LSB_CH3, addr 0x07 | Not applicable | DATA3 [15:0]:<br>16 LSBs of the 28 bit conversion result |

(1) The DATA_CHx.DATAx register must always be read first, followed by the DATA_LSB_ CHx.DATAx register of the same channel to ensure data coherency.
(2) Channels 2 and 3 are only available for FDC2114 and FDC2214.
(3) A DATA value of 0x0000000 = under range for FDC2212/FDC2214.
(4) A DATA value of 0xFFFFFFF = over range for FDC2212/FDC2214.

When the FDC sequences through the channels in multi-channel mode, the dwell time interval for each channel is the sum of three parts:

1. sensor activation time
2. conversion time
3. channel switch delay

The sensor activation time is the amount of settling time required for the sensor oscillation to stabilize, as shown in Figure 6-4. The settling wait time is programmable, and TI recommends setting the wait time to a value that is long enough to allow stable oscillation. The settling wait time for channel x is given by:

$$t_{Sx} = (CHX_SETTLECOUNT \times 16)/f_{REFx} \quad (3)$$

Table 6-5 illustrates the registers and values for configuring the settling time for each channel.

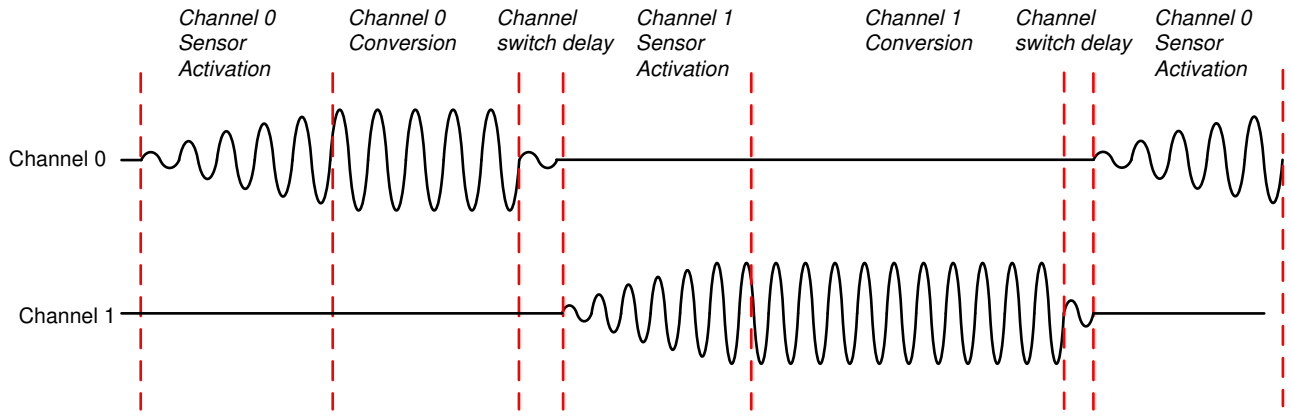



**Figure 6-4. Multi-Channel Mode Sequencing**

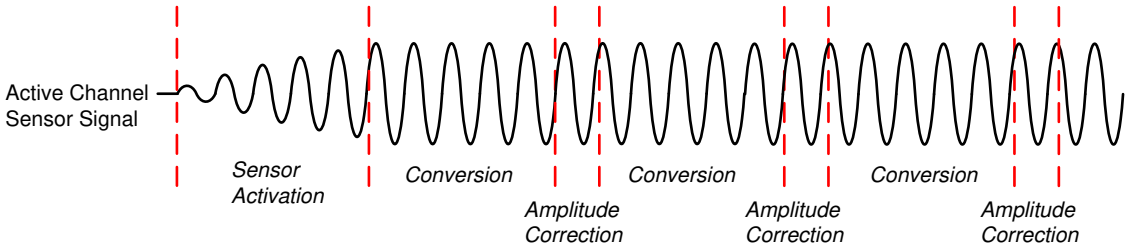



**Figure 6-5. Single-Channel Mode Sequencing**

**Table 6-5. Settling Time Register Configuration**

| CHANNEL(1) | REGISTER | FIELD | CONVERSION TIME(2) |
|---|---|---|---|
| 0 | SETTLECOUNT_CH0, addr 0x10 | CH0_SETTLECOUNT [15:0] | (CH0_SETTLECOUNT*16)/$f_{REF0}$ |


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**Table 6-5. Settling Time Register Configuration (continued)**

| CHANNEL(1) | REGISTER | FIELD | CONVERSION TIME(2) |
|---|---|---|---|
| 1 | SETTLECOUNT_CH1, addr 0x11 | CH1_SETTLECOUNT [15:0] | (CH1_SETTLECOUNT*16)/$f_{REF1}$ |
| 2 | SETTLECOUNT_CH2, addr 0x12 | CH2_SETTLECOUNT [15:0] | (CH2_SETTLECOUNT*16)/$f_{REF2}$ |
| 3 | SETTLECOUNT_CH3, addr 0x13 | CH3_SETTLECOUNT [15:0] | (CH3_SETTLECOUNT*16)/$f_{REF3}$ |

(1) Channels 2 and 3 are available only in the FDC2114 and FDC2214.
(2) $f_{REFx}$ is the reference frequency configured for the channel.

The SETTLECOUNT for any channel x must satisfy:

- $CHx_SETTLECOUNT > V_{pk} \times f_{REFx} \times C \times \pi^2 / (32 \times IDRIVE_X)$ (4)
- – where
  – $V_{pk}$ = Peak oscillation amplitude at the programmed IDRIVE setting
  – $f_{REFx}$ = Reference frequency for Channel x
  – C = sensor capacitance including parasitic PCB capacitance
  – $IDRIVE_X$ = setting programmed into the IDRIVE register in amps
- Round the result to the next highest integer (for example, if Equation 4 recommends a minimum value of 6.08, program the register to 7 or higher).
- The conversion time represents the number of reference clock cycles used to measure the sensor frequency and is set by the CHx_RCOUNT register for the channel. The conversion time for any channel x is:
- $t_{Cx} = (CHx_RCOUNT \times 16 + 4) / f_{REFx}$ (5)
- The reference count value must be chosen to support the required number of effective bits (ENOB). For example, if an ENOB of 13 bits is required, then a minimum conversion time of $2^{13}$ = 8192 clock cycles is required. 8192 clock cycles correspond to a CHx_RCOUNT value of 0x0200.

**Table 6-6. Conversion Time Configuration Registers, Channels 0 - 3 (1)**

| CHANNEL | REGISTER | FIELD [ BIT(S) ] | CONVERSION TIME |
|---|---|---|---|
| 0 | RCOUNT_CH0, addr 0x08 | CH0_RCOUNT [15:0] | (CH0_RCOUNT × 16)/$f_{REF0}$ |
| 1 | RCOUNT_CH1, addr 0x09 | CH1_RCOUNT [15:0] | (CH1_RCOUNT × 16)/$f_{REF1}$ |
| 2 | RCOUNT_CH2, addr 0x0A | CH2_RCOUNT [15:0] | (CH2_RCOUNT × 16)/$f_{REF2}$ |
| 3 | RCOUNT_CH3, addr 0x0B | CH3_RCOUNT [15:0] | (CH3_RCOUNT × 16)/$f_{REF3}$ |

(1) Channels 2 and 3 are available only for FDC2114 and FDC2214.

The typical channel switch delay time between the end of conversion and the beginning of sensor activation of the subsequent channel is:

$$\text{Channel Switch Delay} = 692\text{ns} + 5 / f_{ref} \quad (6)$$

The deterministic conversion time of the FDC allows data polling at a fixed interval. For example, if the programmed SETTLECOUNT is 128 $F_{REF}$ cycles (SETTLECOUNT = 0x0008) and RCOUNT is 512 $F_{REF}$ cycles (RCOUNT=0x0020), then one conversion takes 3.2ms (sensor-activation time) + 12.8ms (conversion time) + 0.8µs (channel-switch delay) = 16.0ms per channel. If the FDC is configured for dual-channel operation by setting AUTOSCAN_EN = 1 and RR_SEQUENCE = 00, then one full set of conversion results is available from the data registers every 32ms.

A data ready flag (DRDY) is also available for interrupt driven system designs (see the STATUS register description in *Register Maps*.

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### 6.3.3 Current Drive Control Registers

The registers listed in Table 6-7 are used to control the sensor drive current. Follow the recommendations listed in the last column of the table.

**Table 6-7. Current Drive Control Registers**

| CHANNEL(1) | REGISTER | FIELD [ BIT(S) ] | VALUE |
|---|---|---|---|
| All | CONFIG, addr 0x1A | SENSOR_ACTIVATE_SEL [11] | Sets current drive for sensor activation. Recommended value is b0 (full current mode). |
| 0 | CONFIG, addr 0x1A | HIGH_CURRENT_DRV [6] | b0 = normal current drive (1.5mA)<br>b1 = Increased current drive (> 1.5mA) for Ch 0 in single channel mode only. Cannot be used in multi-channel mode. |
| 0 | DRIVE_CURRENT_CH0, addr 0x1E | CH0_IDRIVE [15:11] | Drive current used during the settling and conversion time for Ch. 0. Set such that 1.2V ≤ sensor oscillation amplitude (pk) ≤ 1.8V |
| 1 | DRIVE_CURRENT_CH1, addr 0x1F | CH1_IDRIVE [15:11] | Drive current used during the settling and conversion time for Ch. 1. Set such that 1.2V ≤ sensor oscillation amplitude (pk) ≤ 1.8V |
| 2 | DRIVE_CURRENT_CH2, addr 0x20 | CH2_IDRIVE [15:11] | Drive current used during the settling and conversion time for Ch. 2. Set such that 1.2V ≤ sensor oscillation amplitude (pk) ≤ 1.8V |
| 3 | DRIVE_CURRENT_CH3, addr 0x21 | CH3_IDRIVE [15:11] | Drive current used during the settling and conversion time for Ch. 3 . Set such that 1.2V ≤ sensor oscillation amplitude (pk) ≤ 1.8V |

(1) Channels 2 and 3 are available for FDC2114 and FDC2214 only.

Program the CHx_IDRIVE field such that the sensor oscillates at an amplitude between 1.2Vpk ($V_{SENSORMIN}$) and 1.8Vpk ($V_{SENSORMAX}$). An IDRIVE value of 00000 corresponds to 16µA, and IDRIVE = b11111 corresponds to 1563µA.

A high sensor current drive mode can be enabled to drive sensor coils with > 1.5mA on channel 0, only in single channel mode. This feature can be used when the sensor minimum recommended oscillation amplitude of 1.2V cannot be achieved with the highest IDRIVE setting. Set the HIGH_CURRENT_DRV register bit to b1 to enable this mode.

### 6.3.4 Device Status Registers

The registers listed in Table 6-8 may be used to read device status.

**Table 6-8. Status Registers**

| CHANNEL(1) | REGISTER | FIELDS [ BIT(S) ] | VALUES |
|---|---|---|---|
| All | STATUS, addr 0x18 | 12 fields are available that contain various status bits [ 15:0 ] | Refer to *Register Maps* for a description of the individual status bits. |
| All | STATUS_CONFIG, addr 0x19 | 12 fields are available that are used to configure status reporting [ 15:0 ] | Refer to *Register Maps* for a description of the individual error configuration bits. |

(1) Channels 2 and 3 are available for FDC2114 and FDC2114 only.

See the STATUS and STATUS_CONFIG register description in *Register Maps*. These registers can be configured to trigger an interrupt on the INTB pin for certain events. The following conditions must be met:

1. The error or status register must be unmasked by enabling the appropriate register bit in the STATUS_CONFIG register
2. The INTB function must be enabled by setting CONFIG.INTB_DIS to 0


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When a bit field in the STATUS register is set, the entire STATUS register content is held until read or until the DATA_CHx register is read. Reading also deasserts INTB.

Interrupts are cleared by one of the following events:

1. Entering sleep mode
2. Power-on reset (POR)
3. Device enters shutdown mode (SD is asserted)
4. S/W reset
5. $I^2C$ read of the STATUS register: Reading the STATUS register clears any error status bit set in STATUS along with the ERR_CHAN field and deassert INTB

Setting register CONFIG.INTB_DIS to b1 disables the INTB function and holds the INTB pin high.

#### 6.3.5 Input Deglitch Filter

The input deglitch filter suppresses EMI and ringing above the sensor frequency. The input deglitch filter does not impact the conversion result as long as its bandwidth is configured to be above the maximum sensor frequency. The input deglitch filter can be configured in MUX_CONFIG.DEGLITCH register field as shown in Table 6-9. For optimal performance, TI recommends selection of the lowest setting that exceeds the sensor oscillation frequency. For example, if the maximum sensor frequency is 2MHz, choose MUX_CONFIG.DEGLITCH = b100 (3.3MHz).

**Table 6-9. Input Deglitch Filter Register**

| CHANNEL(1) | MUX_CONFIG.DEGLITCH (addr 0x1B) REGISTER VALUE | DEGLITCH FREQUENCY |
|---|---|---|
| ALL | 001 | 1MHz |
| ALL | 100 | 3.3MHz |
| ALL | 101 | 10MHz |
| ALL | 011 | 33MHz |

(1) Channels 2 and 3 are available for FDC2114 / FDC2214 only.

### 6.4 Device Functional Modes

#### 6.4.1 Start-Up Mode

When the FDC powers up, the FDC enters sleep mode and waits for configuration. When the device is configured, exit sleep mode by setting CONFIG.SLEEP_MODE_EN to b0.

TI recommends configuring the FDC while in sleep mode. If a setting on the FDC needs to be changed, return the device to sleep mode, change the appropriate register, and then exit sleep mode.

#### 6.4.2 Normal (Conversion) Mode

When operating in the normal (conversion) mode, the FDC is periodically sampling the frequency of the sensor(s) and generating sample outputs for the active channel(s).

#### 6.4.3 Sleep Mode

Sleep mode is entered by setting the CONFIG.SLEEP_MODE_EN register field to 1. While in this mode, the device configuration is maintained. To exit sleep mode, set the CONFIG.SLEEP_MODE_EN register field to 0. After setting CONFIG.SLEEP_MODE_EN to b0, sensor activation for the first conversion begins after 16,384 $f_{INT}$ clock cycles. While in sleep mode the $I^2C$ interface is functional so that register reads and writes can be performed. While in sleep mode, no conversions are performed. In addition, entering sleep mode clears conversion results, any error condition, and deassert the INTB pin.

#### 6.4.4 Shutdown Mode

When the SD pin is set to high, the FDC enters shutdown mode. Shutdown mode is the lowest power state. To exit shutdown mode, set the SD pin to low. Entering shutdown mode returns all registers to their default state.

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While in shutdown mode, no conversions are performed. In addition, entering shutdown mode clears any error condition and deassert the INTB pin. While the device is in shutdown mode, is not possible to read to or write from the device via the I²C interface.

#### 6.4.4.1 Reset

The FDC can be reset by writing to RESET_DEV.RESET_DEV. Any active conversion stops, and all register values return to their default value. This register bit always returns 0b when read.

## 6.5 Programming

The FDC device uses an I²C interface to access control and data registers.

### *6.5.1 I²C Interface Specifications*

The FDC uses an extended start sequence with I²C for register access. The maximum speed of the I²C interface is 400 kbit/s. This sequence follows the standard I²C 7-bit target address followed by an 8-bit pointer register byte to set the register address. When the ADDR pin is set low, the FDC I²C address is 0x2A; when the ADDR pin is set high, the FDC I²C address is 0x2B. The ADDR pin must not change state after the FDC exits Shutdown Mode.

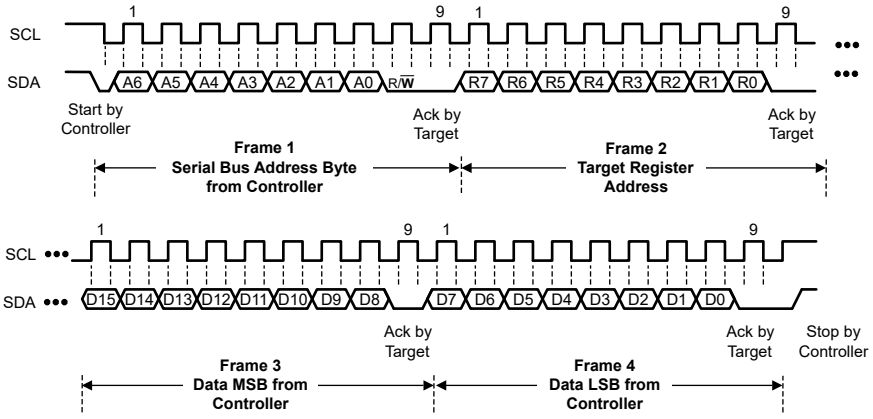



**Figure 6-6. I²C Write Register Sequence**

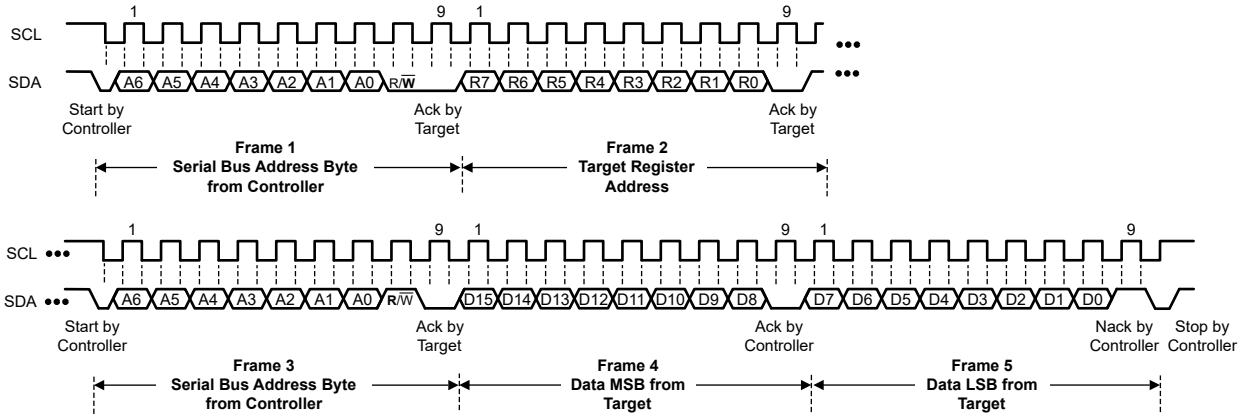



**Figure 6-7. I²C Read Register Sequence**

## 6.6 Register Maps

### *6.6.1 Register List*

Fields indicated with Reserved must be written only with indicated values, otherwise improper device operation may occur. The R/W column indicates the Read-Write status of the corresponding field. A ‘R/W’ entry indicates read and write capability, a ‘R’ indicates read-only, and a ‘W’ indicates write-only.


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**Figure 6-8. Register List**

| ADDRESS | NAME | DEFAULT VALUE | DESCRIPTION |
|---|---|---|---|
| 0x00 | DATA_CH0 | 0x0000 | Channel 0 Conversion Result and status **(FDC2112 / FDC2114 only)** |
| | | 0x0000 | Channel 0 MSB Conversion Result and status **(FDC2212 / FDC2214 only)** |
| 0x01 | DATA_LSB_CH0 | 0x0000 | Channel 0 LSB Conversion Result. Must be read after Register address 0x00 **(FDC2212 / FDC2214 only)** |
| 0x02 | DATA_CH1 | 0x0000 | Channel 1 Conversion Result and status **(FDC2112 / FDC2114 only)** |
| | | 0x0000 | Channel 1 MSB Conversion Result and status **(FDC2212 / FDC2214 only)** |
| 0x03 | DATA_LSB_CH1 | 0x0000 | Channel 1 LSB Conversion Result. Must be read after Register address 0x02 **(FDC2212 / FDC2214 only)** |
| 0x04 | DATA_CH2 | 0x0000 | Channel 2 Conversion Result and status **(FDC2114 only)** |
| | | 0x0000 | Channel 2 MSB Conversion Result and status **(FDC2214 only)** |
| 0x05 | DATA_LSB_CH2 | 0x0000 | Channel 2 LSB Conversion Result. Must be read after Register address 0x04 **(FDC2214 only)** |
| 0x06 | DATA_CH3 | 0x0000 | Channel 3 Conversion Result and status **(FDC2114 only)** |
| | | 0x0000 | Channel 3 MSB Conversion Result and status **(FDC2214 only)** |
| 0x07 | DATA_LSB_CH3 | 0x0000 | Channel 3 LSB Conversion Result. Must be read after Register address 0x06 **(FDC2214 only)** |
| 0x08 | RCOUNT_CH0 | 0x0080 | Reference Count setting for Channel 0 |
| 0x09 | RCOUNT_CH1 | 0x0080 | Reference Count setting for Channel 1 |
| 0x0A | RCOUNT_CH2 | 0x0080 | Reference Count setting for Channel 2 **(FDC2114 / FDC2214 only)** |
| 0x0B | RCOUNT_CH3 | 0x0080 | Reference Count setting for Channel 3 **(FDC2114 / FDC2214 only)** |
| 0x0C | OFFSET_CH0 | 0x0000 | Offset value for Channel 0 **(FDC2112 / FDC2114 only)** |
| 0x0D | OFFSET_CH1 | 0x0000 | Offset value for Channel 1 **(FDC2112 / FDC2114 only)** |
| 0x0E | OFFSET_CH2 | 0x0000 | Offset value for Channel 2 **(FDC2114 only)** |
| 0x0F | OFFSET_CH3 | 0x0000 | Offset value for Channel 3 **(FDC2114 only)** |
| 0x10 | SETTLECOUNT_CH0 | 0x0000 | Channel 0 Settling Reference Count |
| 0x11 | SETTLECOUNT_CH1 | 0x0000 | Channel 1 Settling Reference Count |
| 0x12 | SETTLECOUNT_CH2 | 0x0000 | Channel 2 Settling Reference Count **(FDC2114 / FDC2214 only)** |
| 0x13 | SETTLECOUNT_CH3 | 0x0000 | Channel 3 Settling Reference Count **(FDC2114 / FDC2214 only)** |
| 0x14 | CLOCK_DIVIDERS_CH0 | 0x0000 | Reference divider settings for Channel 0 |
| 0x15 | CLOCK_DIVIDERS_CH1 | 0x0000 | Reference divider settings for Channel 1 |
| 0x16 | CLOCK_DIVIDERS_CH2 | 0x0000 | Reference divider settings for Channel 2 **(FDC2114 / FDC2214 only)** |
| 0x17 | CLOCK_DIVIDERS_CH3 | 0x0000 | Reference divider settings for Channel 3 **(FDC2114 / FDC2214 only)** |
| 0x18 | STATUS | 0x0000 | Device Status Reporting |
| 0x19 | STATUS_CONFIG | 0x0000 | Device Status Reporting Configuration |
| 0x1A | CONFIG | 0x2801 | Conversion Configuration |
| 0x1B | MUX_CONFIG | 0x020F | Channel Multiplexing Configuration |
| 0x1C | RESET_DEV | 0x0000 | Reset Device |
| 0x1E | DRIVE_CURRENT_CH0 | 0x0000 | Channel 0 sensor current drive configuration |
| 0x1F | DRIVE_CURRENT_CH1 | 0x0000 | Channel 1 sensor current drive configuration |
| 0x20 | DRIVE_CURRENT_CH2 | 0x0000 | Channel 2 sensor current drive configuration **(FDC2114 / FDC2214 only)** |
| 0x21 | DRIVE_CURRENT_CH3 | 0x0000 | Channel 3 sensor current drive configuration **(FDC2114 / FDC2214 only)** |
| 0x7E | MANUFACTURER_ID | 0x5449 | Manufacturer ID |
| 0x7F | DEVICE_ID | 0x3054 | Device ID **(FDC2112, FDC2114 only)** |
| | | 0x3055 | Device ID **(FDC2212, FDC2214 only)** |

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### 6.6.2 Address 0x00, DATA_CH0

**Figure 6-9. Address 0x00, DATA_CH0**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | CH0_ERR_WD | CH0_ERR_AW | DATA0 | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA0 | | | | | | | |

**Table 6-10. Address 0x00, DATA_CH0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:14 | RESERVED | R | 00 | Reserved. |
| 13 | CH0_ERR_WD | R | 0 | Channel 0 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit. |
| 12 | CH0_ERR_AW | R | 0 | Channel 0 Amplitude Warning. Cleared by reading the bit. |
| 11:0 | DATA0 (FDC2112 / FDC2114 only)<br>DATA0[27:16] (FDC2212 / FDC2214 only) | R | 0000 0000 0000 | Channel 0 Conversion Result |

### 6.6.3 Address 0x01, DATA_LSB_CH0 (FDC2212 / FDC2214 only)

**Figure 6-10. Address 0x01, DATA_LSB_CH0**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| DATA0 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA0 | | | | | | | |

**Table 6-11. Address 0x01, DATA_CH0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | DATA0[15:0] | R | 0000 0000 0000 | Channel 0 Conversion Result |

### 6.6.4 Address 0x02, DATA_CH1

**Figure 6-11. Address 0x02, DATA_CH1**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | CH1_ERR_WD | CH1_ERR_AW | DATA1 | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA1 | | | | | | | |

**Table 6-12. Address 0x02, DATA_CH1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:14 | RESERVED | R | 00 | Reserved. |
| 13 | CH1_ERR_WD | R | 0 | Channel 1 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit. |
| 12 | CH1_ERR_AW | R | 0 | Channel 1 Amplitude Warning. Cleared by reading the bit. |
| 11:0 | DATA1 (FDC2112 / FDC2114 only)<br>DATA1[27:16] (FDC2212 / FDC2214 only) | R | 0000 0000 0000 | Channel 1 Conversion Result |


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### 6.6.5 Address 0x03, DATA_LSB_CH1 (FDC2212 / FDC2214 only)

**Figure 6-12. Address 0x03, DATA_LSB_CH1**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| DATA1 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA1 | | | | | | | |

**Table 6-13. Address 0x03, DATA_CH1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | DATA1[15:0] | R | 0000 0000 0000 | Channel 1 Conversion Result |

### 6.6.6 Address 0x04, DATA_CH2 (FDC2114, FDC2214 only)

**Figure 6-13. Address 0x04, DATA_CH2**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | CH2_ERR_WD | CH2_ERR_AW | DATA2 | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA2 | | | | | | | |

**Table 6-14. Address 0x04, DATA_CH2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:14 | RESERVED | R | 00 | Reserved. |
| 13 | CH2_ERR_WD | R | 0 | Channel 2 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit. |
| 12 | CH2_ERR_AW | R | 0 | Channel 2 Amplitude Warning. Cleared by reading the bit. |
| 11:0 | DATA2 (FDC2112 / FDC2114 only)<br>DATA2[27:16] (FDC2212 / FDC2214 only) | R | 0000 0000 0000 | Channel 2 Conversion Result |

### 6.6.7 Address 0x05, DATA_LSB_CH2 (FDC2214 only)

**Figure 6-14. Address 0x05, DATA_LSB_CH2**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| DATA2 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA2 | | | | | | | |

**Table 6-15. Address 0x05, DATA_CH2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | DATA2[15:0] | R | 0000 0000 0000 | Channel 2 Conversion Result |

### 6.6.8 Address 0x06, DATA_CH3 (FDC2114, FDC2214 only)

**Figure 6-15. Address 0x06, DATA_CH3**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | CH3_ERR_WD | CH3_ERR_AW | DATA3 | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

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**Figure 6-15. Address 0x06, DATA_CH3 (continued)**

| DATA3 |
|---|

**Table 6-16. Address 0x06, DATA_CH3 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:14 | RESERVED | R | 00 | Reserved. |
| 13 | CH3_ERR_WD | R | 0 | Channel 3 Conversion Watchdog Timeout Error Flag. Cleared by reading the bit. |
| 12 | CH3_ERR_AW | R | 0 | Channel 3 Amplitude Warning. Cleared by reading the bit. |
| 11:0 | DATA3 (FDC2112 / FDC2114 only)<br>DATA3[27:16] (FDC2212 / FDC2214 only) | R | 0000 0000 0000 | Channel 3 Conversion Result |

### *6.6.9 Address 0x07, DATA_LSB_CH3 (FDC2214 only)*

**Figure 6-16. Address 0x07, DATA_LSB_CH3**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| DATA3 | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DATA3 | | | | | | | |

**Table 6-17. Address 0x07, DATA_CH3 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | DATA3[15:0] | R | 0000 0000 0000 | Channel 3 Conversion Result |

### *6.6.10 Address 0x08, RCOUNT_CH0*

**Figure 6-17. Address 0x08, RCOUNT_CH0**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CH0_RCOUNT | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH0_RCOUNT | | | | | | | |

**Table 6-18. Address 0x08, RCOUNT_CH0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | CH0_RCOUNT | R/W | 0000 0000 1000 0000 | Channel 0 Reference Count Conversion Interval Time<br>0x0000-0x00FF: Reserved<br>0x0100-0xFFFF: Conversion Time ($t_{C0}$) = (CH0_RCOUNT×16)/ $f_{REF0}$ |


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### 6.6.11 Address 0x09, RCOUNT_CH1

**Figure 6-18. Address 0x09, RCOUNT_CH1**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CH1_RCOUNT | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH1_RCOUNT | | | | | | | |

**Table 6-19. Address 0x09, RCOUNT_CH1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | CH1_RCOUNT | R/W | 0000 0000<br>1000 0000 | Channel 1 Reference Count Conversion Interval Time<br>0x0000-0x00FF: Reserved<br>0x0100-0xFFFF: Conversion Time ($t_{C1}$)= (CH1_RCOUNT×16)/ $f_{REF1}$ |

### 6.6.12 Address 0x0A, RCOUNT_CH2 (FDC2114, FDC2214 only)

**Figure 6-19. Address 0x0A, RCOUNT_CH2**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CH2_RCOUNT | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH2_RCOUNT | | | | | | | |

**Table 6-20. Address 0x0A, RCOUNT_CH2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | CH2_RCOUNT | R/W | 0000 0000<br>1000 0000 | Channel 2 Reference Count Conversion Interval Time<br>0x0000-0x00FF: Reserved<br>0x0100-0xFFFF: Conversion Time ($t_{C2}$)= (CH2_RCOUNT×16)/ $f_{REF2}$ |

### 6.6.13 Address 0x0B, RCOUNT_CH3 (FDC2114, FDC2214 only)

**Figure 6-20. Address 0x0B, RCOUNT_CH3**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CH3_RCOUNT | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH3_RCOUNT | | | | | | | |

**Table 6-21. Address 0x0B, RCOUNT_CH3 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | CH3_RCOUNT | R/W | 0000 0000<br>1000 0000 | Channel 3 Reference Count Conversion Interval Time<br>0x0000-0x00FF: Reserved<br>0x0100-0xFFFF: Conversion Time ($t_{C3}$)= (CH3_RCOUNT×16)/ $f_{REF3}$ |

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### 6.6.14 Address 0x0C, OFFSET_CH0 (FDC21112 / FDC2114 only)

**Figure 6-21. Address 0x0C, CH0_OFFSET**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CH0_OFFSET | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH0_OFFSET | | | | | | | |

**Table 6-22. CH0_OFFSET Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | CH0_OFFSET | R/W | 0000 0000<br>0000 0000 | Channel 0 Conversion Offset. $f_{OFFSET_0}$ = (CH0_OFFSET/ $2^{16}$)*$f_{REF0}$ |

### 6.6.15 Address 0x0D, OFFSET_CH1 (FDC21112 / FDC2114 only)

**Figure 6-22. Address 0x0D, OFFSET_CH1**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CH1_OFFSET | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH1_OFFSET | | | | | | | |

**Table 6-23. Address 0x0D, OFFSET_CH1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | CH1_OFFSET | R/W | 0000 0000<br>0000 0000 | Channel 1 Conversion Offset. $f_{OFFSET_1}$ = (CH1_OFFSET/ $2^{16}$)*$f_{REF1}$ |

### 6.6.16 Address 0x0E, OFFSET_CH2 (FDC2114 only)

**Figure 6-23. Address 0x0E, OFFSET_CH2**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CH2_OFFSET | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH2_OFFSET | | | | | | | |

**Table 6-24. Address 0x0E, OFFSET_CH2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | CH2_OFFSET | R/W | 0000 0000<br>0000 0000 | Channel 2 Conversion Offset. $f_{OFFSET_2}$ = (CH2_OFFSET/ $2^{16}$)*$f_{REF2}$ |


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### 6.6.17 Address 0x0F, OFFSET_CH3 (FDC2114 only)

**Figure 6-24. Address 0x0F, OFFSET_CH3**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CH3_OFFSET | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH3_OFFSET | | | | | | | |

**Table 6-25. Address 0x0F, OFFSET_CH3 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | CH3_OFFSET | R/W | 0000 0000<br>0000 0000 | Channel 3 Conversion Offset. $f_{OFFSET_3}$ = (CH3_OFFSET/ $2^{16}$)*$f_{REF3}$ |

### 6.6.18 Address 0x10, SETTLECOUNT_CH0

**Figure 6-25. Address 0x10, SETTLECOUNT_CH0**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CH0_SETTLECOUNT | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH0_SETTLECOUNT | | | | | | | |

**Table 6-26. Address 0x11, SETTLECOUNT_CH0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | CH0_SETTLECOUNT | R/W | 0000 0000<br>0000 0000 | Channel 0 Conversion Settling<br>The FDC uses this settling time to allow the LC sensor to stabilize before initiation of a conversion on Channel 0.<br>If the amplitude has not settled prior to the conversion start, an Amplitude warning is generated if reporting of this type of warning is enabled.<br>0x0000: Settle Time ($t_{S0}$)= 32 ÷ $f_{REF0}$<br>0x0001: Settle Time ($t_{S0}$)= 32 ÷ $f_{REF0}$<br>0x0002 - 0xFFFF: Settle Time ($t_{S0}$)= (CH0_SETTLECOUNT×16) ÷ $f_{REF0}$ |

### 6.6.19 Address 0x11, SETTLECOUNT_CH1

**Figure 6-26. Address 0x11, SETTLECOUNT_CH1**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CH1_SETTLECOUNT | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH1_SETTLECOUNT | | | | | | | |

**Table 6-27. Address 0x12, SETTLECOUNT_CH1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | CH1_SETTLECOUNT | R/W | 0000 0000<br>0000 0000 | Channel 1 Conversion Settling<br>The FDC uses this settling time to allow the LC sensor to stabilize before initiation of a conversion on a Channel 1.<br>If the amplitude has not settled prior to the conversion start, an Amplitude warning is generated if reporting of this type of warning is enabled.<br>0x0000: Settle Time ($t_{S1}$)= 32 ÷ $f_{REF1}$<br>0x0001: Settle Time ($t_{S1}$)= 32 ÷ $f_{REF1}$<br>0x0002 - 0xFFFF: Settle Time ($t_{S1}$)= (CH1_SETTLECOUNT×16) ÷ $f_{REF1}$ |

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### 6.6.20 Address 0x12, SETTLECOUNT_CH2 (FDC2114, FDC2214 only)

**Figure 6-27. Address 0x12, SETTLECOUNT_CH2**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CH2_SETTLECOUNT | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH2_SETTLECOUNT | | | | | | | |

**Table 6-28. Address 0x12, SETTLECOUNT_CH2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | CH2_SETTLECOUNT | R/W | 0000 0000<br>0000 0000 | Channel 2 Conversion Settling<br>The FDC uses this settling time to allow the LC sensor to stabilize before initiation of a conversion on Channel 2.<br>If the amplitude has not settled prior to the conversion start, an Amplitude warning is generated if reporting of this type of warning is enabled.<br>0x0000: Settle Time ($t_{S2}$) = 32 ÷ $f_{REF2}$<br>0x0001: Settle Time ($t_{S2}$) = 32 ÷ $f_{REF2}$<br>0x0002 - 0xFFFF: Settle Time ($t_{S2}$)= (CH2_SETTLECOUNT×16) ÷ $f_{REF2}$ |

### 6.6.21 Address 0x13, SETTLECOUNT_CH3 (FDC2114, FDC2214 only)

**Figure 6-28. Address 0x13, SETTLECOUNT_CH3**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CH3_SETTLECOUNT | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH3_SETTLECOUNT | | | | | | | |

**Table 6-29. Address 0x13, SETTLECOUNT_CH3 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | CH3_SETTLECOUNT | R/W | 0000 0000<br>0000 0000 | Channel 3 Conversion Settling<br>The FDC uses this settling time to allow the LC sensor to stabilize before initiation of a conversion on Channel 3.<br>If the amplitude has not settled prior to the conversion start, an Amplitude warning is generated if reporting of this type of warning is enabled<br>0x0000: Settle Time ($t_{S3}$) = 32 ÷ $f_{REF3}$<br>0x0001: Settle Time ($t_{S3}$) = 32 ÷ $f_{REF3}$<br>0x0002 - 0xFFFF: Settle Time ($t_{S3}$)= (CH3_SETTLECOUNT×16) ÷ $f_{REF3}$ |


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### 6.6.22 Address 0x14, CLOCK_DIVIDERS_CH0

**Figure 6-29. Address 0x14, CLOCK_DIVIDERS_CH0**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | CH0_FIN_SEL | | RESERVED | | CH0_FREF_DIVIDER | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH0_FREF_DIVIDER | | | | | | | |

**Table 6-30. Address 0x14, CLOCK_DIVIDERS_CH0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:14 | RESERVED | R/W | 00 | Reserved. Set to b00. |
| 13:12 | CH0_FIN_SEL | R/W | 00 | Channel 0 Sensor frequency select<br>for differential sensor configuration:<br>b01: divide by 1. Choose for sensor frequencies between 0.01MHz and 8.75MHz<br>b10: divide by 2. Choose for sensor frequencies between 5MHz and 10MHz<br>for single-ended sensor configuration:<br>b10: divide by 2. Choose for sensor frequencies between 0.01MHz and 10MHz |
| 11:10 | RESERVED | R/W | 00 | Reserved. Set to b00. |
| 9:0 | CH0_FREF_DIVIDER | R/W | 00 0000 0000 | Channel 0 Reference Divider<br>Sets the divider for Channel 0 reference. Use this to scale the maximum conversion frequency.<br>b00'0000'0000: Reserved. Do not use.<br>CH0_FREF_DIVIDER≥b00'0000'0001: $f_{REF0} = f_{CLK}$/ CH0_FREF_DIVIDER |

### 6.6.23 Address 0x15, CLOCK_DIVIDERS_CH1

**Figure 6-30. Address 0x15, CLOCK_DIVIDERS_CH1**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | CH1_FIN_SEL | | RESERVED | | CH1_FREF_DIVIDER | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH1_FREF_DIVIDER | | | | | | | |

**Table 6-31. Address 0x15, CLOCK_DIVIDERS_CH1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:14 | RESERVED | R/W | 00 | Reserved. Set to b00. |
| 13:12 | CH1_FIN_SEL | R/W | 0000 | Channel 1 Sensor frequency select<br>for differential sensor configuration:<br>b01: divide by 1. Choose for sensor frequencies between 0.01MHz and 8.75MHz<br>b10: divide by 2. Choose for sensor frequencies between 5MHz and 10MHz<br>for single-ended sensor configuration:<br>b10: divide by 2. Choose for sensor frequencies between 0.01MHz and 10MHz |
| 11:10 | RESERVED | R/W | 00 | Reserved. Set to b00. |
| 9:0 | CH1_FREF_DIVIDER | R/W | 00 0000 0000 | Channel 1 Reference Divider<br>Sets the divider for Channel 1 reference. Use this to scale the maximum conversion frequency.<br>b00'0000'0000: Reserved. Do not use.<br>CH1_FREF_DIVIDER≥ b00'0000'0001: $f_{REF1} = f_{CLK}$/ CH1_FREF_DIVIDER |

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### 6.6.24 Address 0x16, CLOCK_DIVIDERS_CH2 (FDC2114, FDC2214 only)

**Figure 6-31. Address 0x16, CLOCK_DIVIDERS_CH2**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | CH2_FIN_SEL | | RESERVED | | CH2_FREF_DIVIDER | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH2_FREF_DIVIDER | | | | | | | |

**Table 6-32. Address 0x16, CLOCK_DIVIDERS_CH2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:14 | RESERVED | R/W | 00 | Reserved. Set to b00. |
| 13:12 | CH2_FIN_SEL | R/W | 0000 | Channel 2 Sensor frequency select<br>for differential sensor configuration:<br>b01: divide by 1. Choose for sensor frequencies between 0.01MHz and 8.75MHz<br>b10: divide by 2. Choose for sensor frequencies between 5MHz and 10MHz<br>for single-ended sensor configuration:<br>b10: divide by 2. Choose for sensor frequencies between 0.01MHz and 10MHz |
| 11:10 | RESERVED | R/W | 00 | Reserved. Set to b00. |
| 9:0 | CH2_FREF_DIVIDER | R/W | 00 0000 0000 | Channel 2 Reference Divider<br>Sets the divider for Channel 2 reference. Use this to scale the maximum conversion frequency.<br>b00'0000'0000: Reserved. Do not use.<br>CH2_FREF_DIVIDER ≥ b00'0000'0001: $f_{REF2} = f_{CLK}$/ CH2_FREF_DIVIDER |

### 6.6.25 Address 0x17, CLOCK_DIVIDERS_CH3 (FDC2114, FDC2214 only)

**Figure 6-32. Address 0x17, CLOCK_DIVIDERS_CH3**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | CH3_FIN_SEL | | RESERVED | | CH3_FREF_DIVIDER | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CH3_FREF_DIVIDER | | | | | | | |

**Table 6-33. Address 0x17, CLOCK_DIVIDERS_CH3**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:14 | RESERVED | R/W | 00 | Reserved. Set to b00. |
| 13:12 | CH3_FIN_SEL | R/W | 0000 | Channel 3 Sensor frequency select<br>for differential sensor configuration:<br>b01: divide by 1. Choose for sensor frequencies between 0.01MHz and 8.75MHz<br>b10: divide by 2. Choose for sensor frequencies between 5MHz and 10MHz<br>for single-ended sensor configuration:<br>b10: divide by 2. Choose for sensor frequencies between 0.01MHz and 10MHz |
| 11:10 | RESERVED | R/W | 00 | Reserved. Set to b00. |
| 9:0 | CH3_FREF_DIVIDER | R/W | 00 0000 0000 | Channel 3 Reference Divider<br>Sets the divider for Channel 3 reference. Use this to scale the maximum conversion frequency.<br>b00'0000'0000: reserved<br>CH3_FREF_DIVIDER ≥ b00'0000'0001: $f_{REF3} = f_{CLK}$/ CH3_FREF_DIVIDER |


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### 6.6.26 Address 0x18, STATUS

**Figure 6-33. Address 0x18, STATUS**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| ERR_CHAN | | RESERVED | | ERR_WD | RESERVED | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | DRDY | RESERVED | | CH0_UNREAD CONV | CH1_ UNREADCONV | CH2_ UNREADCONV | CH3_ UNREADCONV |

**Table 6-34. Address 0x18, STATUS Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:14 | ERR_CHAN | R | 00 | Error Channel<br>Indicates which channel has generated a Flag or Error. When flagged, any reported error is latched and maintained until either the STATUS register or the DATA_CHx register corresponding to the Error Channel is read.<br>b00: Channel 0 is source of flag or error.<br>b01: Channel 1 is source of flag or error.<br>b10: Channel 2 is source of flag or error (FDC2114, FDC2214 only).<br>b11: Channel 3 is source of flag or error (FDC2114, FDC2214 only). |
| 13:12 | RESERVED | R | 00 | Reserved |
| 11 | ERR_WD | R | 0 | Watchdog Timeout Error<br>b0: No Watchdog Timeout error was recorded since the last read of the STATUS register.<br>b1: An active channel has generated a Watchdog Timeout error. Refer to STATUS.ERR_CHAN field to determine which channel is the source of this error. |
| 10 | ERR_AHW | R | 0 | Amplitude High Warning<br>b0: No Amplitude High warning was recorded since the last read of the STATUS register.<br>b1: An active channel has generated an Amplitude High warning. Refer to STATUS.ERR_CHAN field to determine which channel is the source of this warning. |
| 9 | ERR_ALW | R | 0 | Amplitude Low Warning<br>b0: No Amplitude Low warning was recorded since the last read of the STATUS register.<br>b1: An active channel has generated an Amplitude Low warning. Refer to STATUS.ERR_CHAN field to determine which channel is the source of this warning. |
| 8:7 | RESERVED | R | 00 | Reserved |
| 6 | DRDY | R | 0 | Data Ready Flag.<br>b0: No new conversion result was recorded in the STATUS register.<br>b1: A new conversion result is ready. When in Single Channel Conversion, this indicates a single conversion is available. When in sequential mode, this indicates that a new conversion result for all active channels is now available. |
| 3 | CH0_UNREADCONV | R | 0 | Channel 0 Unread Conversion b0: No unread conversion is present for Channel 0.<br>b1: An unread conversion is present for Channel 0.<br>Read Register DATA_CH0 to retrieve conversion results. |
| 2 | CH1_ UNREADCONV | R | 0 | Channel 1 Unread Conversion b0: No unread conversion is present for Channel 1.<br>b1: An unread conversion is present for Channel 1.<br>Read Register DATA_CH1 to retrieve conversion results. |
| 1 | CH2_ UNREADCONV | R | 0 | Channel 2 Unread Conversion b0: No unread conversion is present for Channel 2.<br>b1: An unread conversion is present for Channel 2.<br>Read Register DATA_CH2 to retrieve conversion results (FDC2114, FDC2214 only) |
| 0 | CH3_ UNREADCONV | R | 0 | Channel 3 Unread Conversion<br>b0: No unread conversion is present for Channel 3.<br>b1: An unread conversion is present for Channel 3.<br>Read Register DATA_CH3 to retrieve conversion results (FDC2114, FDC2214 only) |

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### 6.6.27 Address 0x19, ERROR_CONFIG

**Figure 6-34. Address 0x19, ERROR_CONFIG**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | WD_ ERR2OUT | AH_WARN2OUT | AL_WARN2OUT | RESERVED | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | WD_ERR2INT | RESERVED | | | | DRDY_2INT |

**Table 6-35. Address 0x19, ERROR_CONFIG**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:14 | RESERVED | R/W | 00 | Reserved (set to b000) |
| 13 | WD_ ERR2OUT | R/W | 0 | Watchdog Timeout Error to Output Register<br>b0: Do not report Watchdog Timeout errors in the DATA_CHx registers.<br>b1: Report Watchdog Timeout errors in the DATA_CHx.CHx_ERR_WD register field corresponding to the channel that generated the error. |
| 12 | AH_WARN2OUT | R/W | 0 | Amplitude High Warning to Output Register<br>b0:Do not report Amplitude High warnings in the DATA_CHx registers.<br>b1: Report Amplitude High warnings in the DATA_CHx.CHx_ERR_AW register field corresponding to the channel that generated the warning. |
| 11 | AL_WARN2OUT | R/W | 0 | Amplitude Low Warning to Output Register<br>b0: Do not report Amplitude Low warnings in the DATA_CHx registers.<br>b1: Report Amplitude High warnings in the DATA_CHx.CHx_ERR_AW register field corresponding to the channel that generated the warning. |
| 10:6 | RESERVED | R/W | 0 0000 | Reserved (set to b0 0000) |
| 5 | WD_ERR2INT | R/W | 0 | Watchdog Timeout Error to INTB b0: Do not report Under-range errors by asserting INTB pin and STATUS register.<br>b1: Report Watchdog Timeout errors by asserting INTB pin and updating STATUS.ERR_WD register field. |
| 4:1 | Reserved | R/W | 0000 | Reserved (set to b000) |
| 0 | DRDY_2INT | R/W | 0 | Data Ready Flag to INTB b0: Do not report Data Ready Flag by asserting INTB pin and STATUS register.<br>b1: Report Data Ready Flag by asserting INTB pin and updating STATUS. DRDY register field. |


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### 6.6.28 Address 0x1A, CONFIG

**Figure 6-35. Address 0x1A, CONFIG**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| ACTIVE_CHAN | | SLEEP_MODE_EN | RESERVED | SENSOR_ACTIVATE_SEL | RESERVED | REF_CLK_SRC | RESERVED |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INTB_DIS | HIGH_CURRENT_DRV | RESERVED | | | | | |

**Table 6-36. Address 0x1A, CONFIG Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:14 | ACTIVE_CHAN | R/W | 00 | Active channel selection<br>Selects channel for continuous conversions when MUX_CONFIG.SEQUENTIAL is 0.<br>b00: Perform continuous conversions on Channel 0<br>b01: Perform continuous conversions on Channel 1<br>b10: Perform continuous conversions on Channel 2 (FDC2114, FDC2214 only)<br>b11: Perform continuous conversions on Channel 3 (FDC2114, FDC2214 only) |
| 13 | SLEEP_MODE_EN | R/W | 1 | Sleep mode enable<br>Enter or exit low power sleep mode.<br>b0: Device is active.<br>b1: Device is in sleep mode. |
| 12 | RESERVED | R/W | 0 | Reserved. **Set to b1.** |
| 11 | SENSOR_ACTIVATE_SEL | R/W | 1 | Sensor activation mode selection.<br>Set the mode for sensor initialization.<br>b0: Full current activation mode – the FDC drives the maximum sensor current for a shorter sensor activation time.<br>b1: Low power activation mode – the FDC uses the value programmed in DRIVE_CURRENT_CHx during sensor activation to minimize power consumption. |
| 10 | RESERVED | R/W | 0 | Reserved. **Set to b1.** |
| 9 | REF_CLK_SRC | R/W | 0 | Select Reference Frequency Source<br>b0: Use Internal oscillator as reference frequency<br>b1: Reference frequency is provided from CLKIN pin. |
| 8 | RESERVED | R/W | 0 | Reserved. Set to b0. |
| 7 | INTB_DIS | R/W | 0 | INTB Disable<br>b0: Asserts INTB pin when status register updates.<br>b1: Does not assert INTB pin when status register updates |
| 6 | HIGH_CURRENT_DRV | R/W | 0 | High Current Sensor Drive<br>b0: The FDC drives all channels with normal sensor current (1.5mA maximum).<br>b1: The FDC drives channel 0 with current >1.5mA.<br>This mode is not supported if AUTOSCAN_EN = b1 (multi-channel mode) |
| 5:0 | RESERVED | R/W | 00 0001 | Reserved Set to b00’0001 |

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### 6.6.29 Address 0x1B, MUX_CONFIG

**Figure 6-36. Address 0x1B, MUX_CONFIG**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| AUTOSCAN_EN | RR_SEQUENCE | | RESERVED | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | DEGLITCH | |

**Table 6-37. Address 0x1B, MUX_CONFIG Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15 | AUTOSCAN_EN | R/W | 0 | Auto-Scan mode enable<br>b0: Continuous conversion on the single channel selected by CONFIG.ACTIVE_CHAN register field.<br>b1: Auto-Scan conversions as selected by MUX_CONFIG.RR_SEQUENCE register field. |
| 14:13 | RR_SEQUENCE | R/W | 00 | Auto-Scan sequence configuration<br>Configure multiplexing channel sequence. The FDC performs a single conversion on each channel in the sequence selected, and then restart the sequence continuously.<br>b00: Ch0, Ch1<br>b01: Ch0, Ch1, Ch2 (FDC2114, FDC2214 only)<br>b10: Ch0, Ch1, Ch2, Ch3 (FDC2114, FDC2214 only)<br>b11: Ch0, Ch1 |
| 12:3 | RESERVED | R/W | 00 0100 0001 | Reserved. Must be set to 00 0100 0001 |
| 2:0 | DEGLITCH | R/W | 111 | Input deglitch filter bandwidth.<br>Select the lowest setting that exceeds the oscillation tank oscillation frequency.<br>b001: 1MHz<br>b100: 3.3MHz<br>b101: 10MHz<br>b111: 33MHz |

### 6.6.30 Address 0x1C, RESET_DEV

**Figure 6-37. Address 0x1C, RESET_DEV**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESET_DEV | RESERVED | | | | OUTPUT_GAIN | | RESERVED |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |

**Table 6-38. Address 0x1C, RESET_DEV Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15 | RESET_DEV | R/W | 0 | Device Reset<br>Write b1 to reset the device. Will always readback 0. |
| 14:11 | RESERVED | R/W | 0000 | Reserved. Set to b0000 |
| 10:9 | OUTPUT_GAIN | R/W | 00 | Output gain control (FDC2112, FDC2114 only)<br>00: Gain =1 (0 bits shift)<br>01: Gain = 4 (2 bits shift)<br>10: Gain = 8 (3 bits shift)<br>11: Gain = 16 (4 bits shift) |
| 8:0 | RESERVED | R/W | 0 0000 0000 | Reserved, Set to b0 0000 0000 |


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### 6.6.31 Address 0x1E, DRIVE_CURRENT_CH0

**Figure 6-38. Address 0x1E, DRIVE_CURRENT_CH0**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CH0_IDRIVE | | | | | RESERVED | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |

**Table 6-39. Address 0x1E, DRIVE_CURRENT_CH0 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:11 | CH0_IDRIVE | R/W | 0000 0 | Channel 0 Sensor drive current<br>This field defines the Drive Current used during the settling + conversion time of Channel 0 sensor clock. Set such that 1.2V ≤ sensor oscillation amplitude (pk) ≤ 1.8V<br>00000: 0.016mA<br>00001: 0.018mA<br>00010: 0.021mA<br>00011: 0.025mA<br>00100: 0.028mA<br>00101: 0.033mA<br>00110: 0.038mA<br>00111: 0.044mA<br>01000: 0.052mA<br>01001: 0.060mA<br>01010: 0.069mA<br>01011: 0.081mA<br>01100: 0.093mA<br>01101: 0.108mA<br>01110: 0.126mA<br>01111: 0.146mA<br>10000: 0.169mA<br>10001: 0.196mA<br>10010: 0.228mA<br>10011: 0.264mA<br>10100: 0.307mA<br>10101: 0.356mA<br>10110: 0.413mA<br>10111: 0.479mA<br>11000: 0.555mA<br>11001: 0.644mA<br>11010: 0.747mA<br>11011: 0.867mA<br>11100: 1.006mA<br>11101: 1.167mA<br>11110: 1.354mA<br>11111: 1.571mA |
| 10:0 | RESERVED | – | 000 0000 0000 | Reserved |

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### 6.6.32 Address 0x1F, DRIVE_CURRENT_CH1

**Figure 6-39. Address 0x1F, DRIVE_CURRENT_CH1**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CH1_IDRIVE | | | | | RESERVED | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |

**Table 6-40. Address 0x1F, DRIVE_CURRENT_CH1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:11 | CH1_IDRIVE | R/W | 0000 0 | Channel 1 Sensor drive current<br>This field defines the drive current used during the settling + conversion time of Channel 1 sensor clock. Set such that 1.2V ≤ sensor oscillation amplitude (pk) ≤ 1.8V<br>00000: 0.016mA<br>00001: 0.018mA<br>00010: 0.021mA<br>...<br>11111: 1.571mA |
| 10:0 | RESERVED | - | 000 0000 0000 | Reserved |

### 6.6.33 Address 0x20, DRIVE_CURRENT_CH2 (FDC2114 / FDC2214 only)

**Figure 6-40. Address 0x20, DRIVE_CURRENT_CH2**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CH2_IDRIVE | | | | | RESERVED | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |

**Table 6-41. Address 0x20, DRIVE_CURRENT_CH2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:11 | CH2_IDRIVE | R/W | 0000 0 | Channel 2 Sensor drive current<br>This field defines the drive current to be used during the settling + conversion time of Channel 2 sensor clock. Set such that 1.2V ≤ sensor oscillation amplitude (pk) ≤ 1.8V<br>00000: 0.016mA<br>00001: 0.018mA<br>00010: 0.021mA<br>...<br>11111: 1.571mA |
| 10:0 | RESERVED | – | 000 0000 0000 | Reserved |


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### 6.6.34 Address 0x21, DRIVE_CURRENT_CH3 (FDC2114 / FDC2214 only)

**Figure 6-41. Address 0x21, DRIVE_CURRENT_CH3**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CH3_IDRIVE | | | | | RESERVED | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | | | |

**Table 6-42. DRIVE_CURRENT_CH3 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:11 | CH3_IDRIVE | R/W | 0000 0 | Channel 3 Sensor drive current<br>This field defines the drive current to be used during the settling + conversion time of Channel 3 sensor clock. Set such that 1.2V ≤ sensor oscillation amplitude (pk) ≤ 1.8V<br>00000: 0.016mA<br>00001: 0.018mA<br>00010: 0.021mA<br>...<br>11111: 1.571mA |
| 10:0 | RESERVED | – | 000 0000 0000 | Reserved |

### 6.6.35 Address 0x7E, MANUFACTURER_ID

**Figure 6-42. Address 0x7E, MANUFACTURER_ID**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| MANUFACTURER_ID | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MANUFACTURER_ID | | | | | | | |

**Table 6-43. Address 0x7E, MANUFACTURER_ID Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15:0 | MANUFACTURER_ID | R | 0101 0100 0100 1001 | Manufacturer ID = 0x5449 |

### 6.6.36 Address 0x7F, DEVICE_ID

**Figure 6-43. Address 0x7F, DEVICE_ID**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DEVICE_ID | | | | | | | |

**Table 6-44. Address 0x7F, DEVICE_ID Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | DEVICE_ID | R | 0011 0000 0101 0100 | Device ID<br>0x3054 (FDC2112, FDC2114 only)<br>0x3055 (FDC2212, FDC2214 only) |

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# 7 Application and Implementation

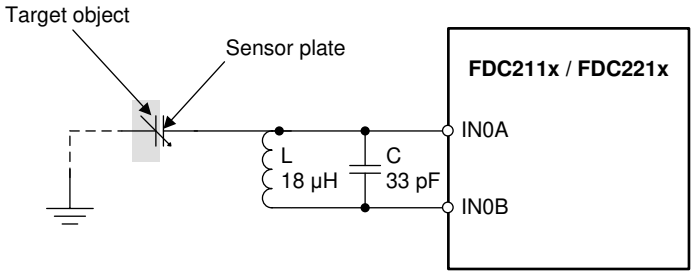
**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

### *7.1.1 Sensor Configuration*

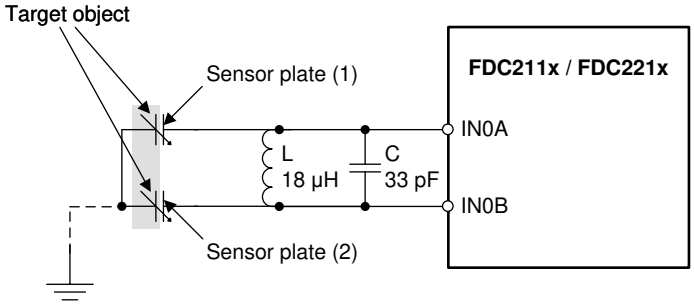
The FDC supports two sensor configurations. Both configurations use an LC tank to set the frequency of oscillation. A typical choice is an 18-µH shielded SMD inductor in parallel with a 33pF capacitor, which result in a 6.5MHz oscillation frequency. In the single-ended configuration in Figure 7-1, a conductive plate is connected IN0A. Together with a target object, the conductive plate forms a variable capacitor.




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**Figure 7-1. Single-Ended Sensor Configuration**

In the differential sensor configuration in Figure 7-2, one conductive plate is connected to IN0A, and a second conductive plate is connected to IN0B. Together, they form a variable capacitor. When using an single-ended sensor configuration, set CHx_FIN_SEL to b10 (divide by 2).




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**Figure 7-2. Differential Sensor Configuration**

The single-ended configuration allows higher sensing range than the differential configuration for a given total sensor plate area. In applications in which high sensitivity at close proximity is desired, the differential configuration performs better than the single-ended configuration.


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### 7.1.2 Shield

in order to minimize interference from external objects, some applications require an additional plate which acts as a shield. The shield can either be:

- actively driven shield: The shield is a buffered signal of the INxA pin. The signal is buffered by an external amplifier with a gain of 1.
- passive shield: The shield is connected to GND. Adding a passive shield decreases sensitivity of the sensor, but is dependent on the distance between the distance between the sensing plate and the shield. Adjust the distance between the sensing plate and the shield to achieve the required sensitivity.

### 7.1.3 Power-Cycled Applications

For applications which do not require high sample rates or maximum conversion resolution, the total active conversion time of the FDC can be minimized to reduce power consumption. This can be done by either by using sleep mode or shutdown mode during times in which conversions are not required (see *Device Functional Modes*).

As an example, for an application which only needs 10 samples per second with a resolution of 16 bits can utilize the low-power modes. The sensor requires SETTLECOUNT = 16 and IDRIVE of 01111b (0.146mA). Given FREF = 40MHz and RCOUNT = 4096 will provide the resolution required. This corresponds to 4096 × 16 × 10 / 40MHz → 16.4ms of active conversion time per second. Start-up time and channel switch delay account for an additional 0.34ms. For the remainder of the time, the device can be in sleep mode: Therefore, the average current is 19.4ms * 3.6mA active current + 980.6ms of 35µA of sleep current, which is approximately 104.6µA of average supply current. Sleep mode retains register settings and therefore requires less $I^2C$ writes to wake up the FDC than shutdown mode.

Greater current savings can be realized by use of shutdown mode during inactive periods. In shutdown mode, device configuration is not retained, so the device must be configured for each sample. For this example, configuring each sample takes approximately 1.2ms (13 registers × 92.5 µs per register). The total active time is 20.6ms. The average current is 20ms × 3.6mA active current + 980ms × 2µA of shutdown current, which is approximately 75µA of average supply current.

For further information on power-cycled applications, refer to *Power Reduction Techniques for the FDC2214/2212/2114/2112 in Capacitive Sensing Applications*.

### 7.1.4 Inductor Self-Resonant Frequency

Every inductor has a distributed parasitic capacitance, which is dependent on construction and geometry. At the self-resonant frequency (SRF), the reactance of the inductor cancels the reactance of the parasitic capacitance. Above the SRF, the inductor electrically appears to be a capacitor. The parasitic capacitance is not well-controlled or stable, therefore TI recommends $f_{SENSOR} < 0.8 \times f_{SR}$.

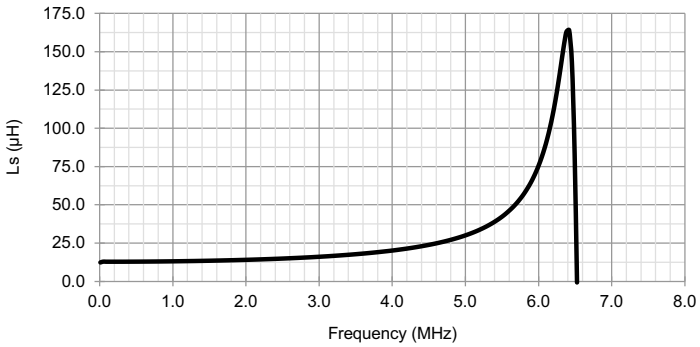



**Figure 7-3. Example Coil Inductance vs Frequency**

The example inductor in Figure 7-3, has a SRF at 6.38MHz; therefore, the inductor must not be operated above 0.8 × 6.38MHz, or 5.1MHz.

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### 7.1.5 Application Curves for Proximity Sensing

*Common test conditions (unless specified otherwise):* Sensor capacitor: 1 layer, 20.9 × 13.9mm, Bourns CMH322522-180KL sensor inductor with L=18µH and 33pF 1% COG/NP0 Target: Grounded aluminum plate (176 × 123mm), Channel = Channel 0 (continuous mode) CLKIN = 40MHz, CHx_FIN_SEL = b10, CHx_FREF_DIVIDER = b00 0000 0001 CH0_RCOUNT = 0xFFFF, SETTLECOUNT_CH0 = 0x0100, DRIVE_CURRENT_CH0 = 0x7800

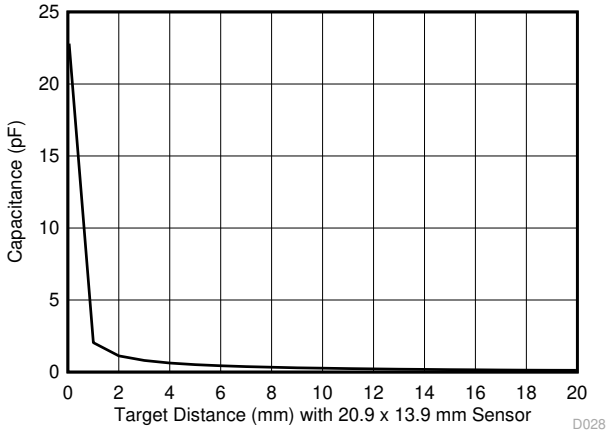



**Figure 7-4. FDC2212 / FDC2214: Capacitance vs Target Distance (0mm to 20mm)**

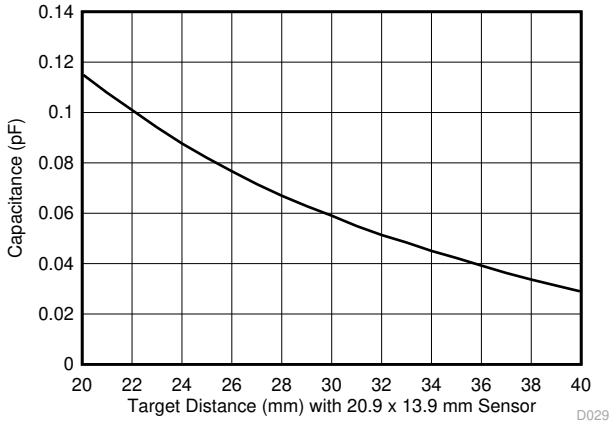



**Figure 7-5. FDC2112 / FDC2114: Capacitance vs Target Distance (20mm to 40mm)**

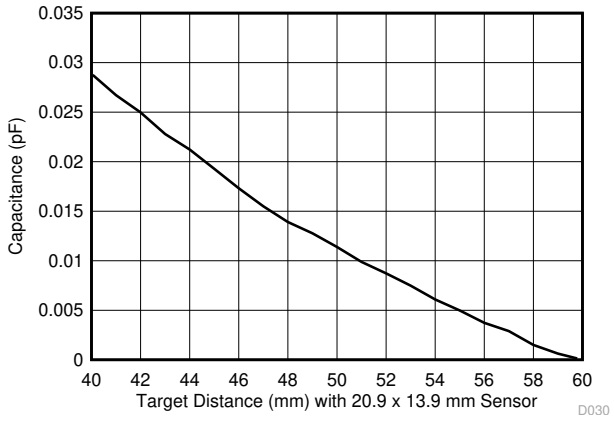



**Figure 7-6. FDC2212 / FDC2214: Capacitance vs Target Distance (40mm to 60mm)**

## 7.2 Typical Application

The FDC can be used to measure liquid level in non-conductive containers. Due to very high excitation rate capability, the FDC is able to measure soapy water, ink, soap, and other conductive liquids. Capacitive sensors can be attached to the outside of the container or be located remotely from the container, allowing for contactless measurements.

The working principle is based on a ratiometric measurement; Figure 7-7 shows a possible system implementation which uses three electrodes. The level electrode provides a capacitance value proportional to the liquid level. The reference environmental electrode and the reference liquid electrode are used as references. The reference liquid electrode accounts for the liquid dielectric constant and its variation, while the reference environmental electrode is used to compensate for any other environmental variations that are not due to the liquid itself. Note that the reference environmental electrode and the reference liquid electrode are the same physical size (hREF).


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For this application, single-ended measurements on the active channels are appropriate, as the tank is grounded. Use Equation 7 to determine the liquid level from the measured capacitances:

$$Level = h_{ref} \frac{C_{Lev} - C_{Lev}(0)}{C_{RL} - C_{RE}} \quad (7)$$

where

- $C_{RE}$ is the capacitance of the reference environmental electrode,
- $C_{RL}$ is the capacitance of the reference liquid electrode,
- $C_{Lev}$ is the current value of the capacitance measured at the level electrode sensor,
- $C_{Lev}(0)$ is the capacitance of the Level electrode when the container is empty, and
- $h_{REF}$ is the height in the desired units of the container or liquid reference electrodes.

The ratio between the capacitance of the level and the reference electrodes allows simple calculation of the liquid level inside the container itself. Very high sensitivity values (that is, many LSB/mm) can be obtained due to the high resolution of the FDC2x1x, even when the sensors are located remotely from the container. Note that this approach assumes that the container has a uniform cross section from top to bottom, so that each incremental increase or decrease in the liquid represents a change in volume that is directly related to the height of the liquid.

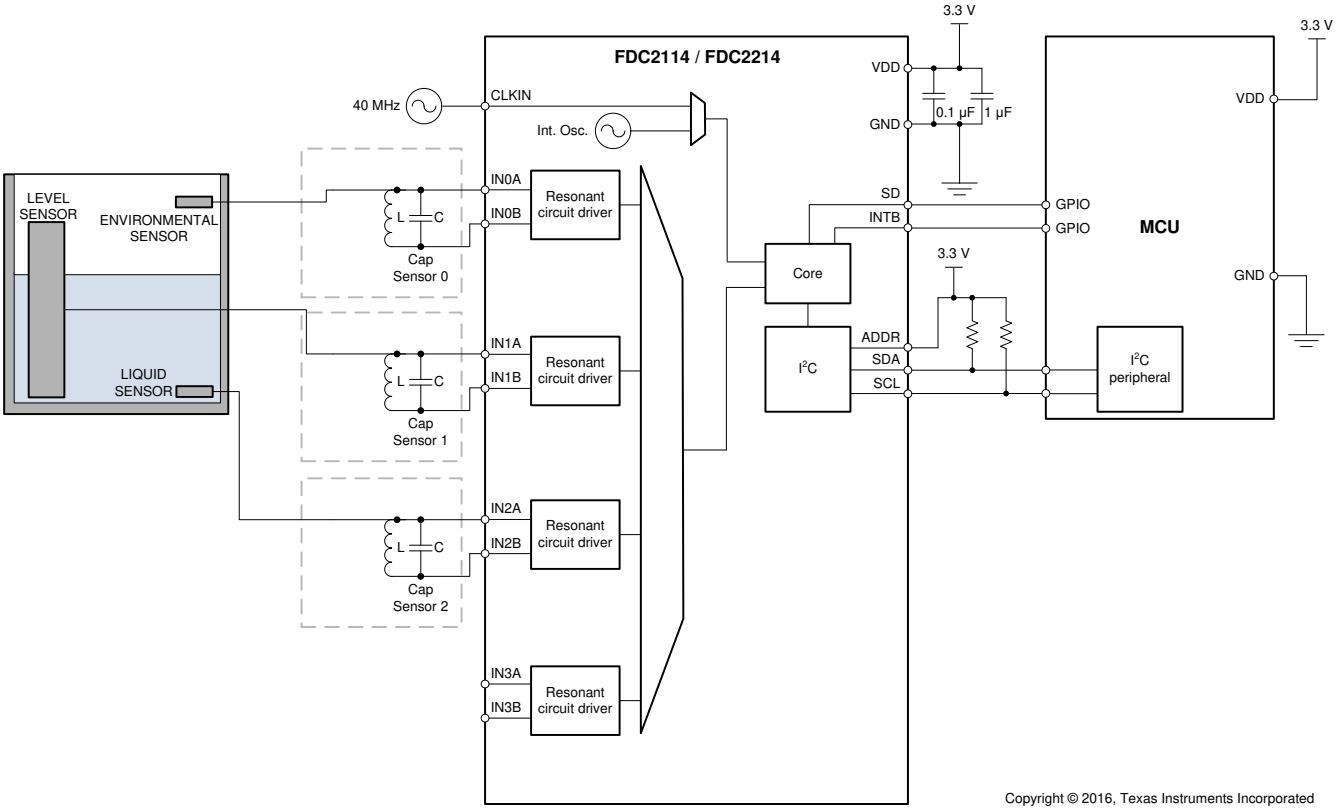



**Figure 7-7. FDC (Liquid Level Measurement)**

### *7.2.1 Design Requirements*

Make sure the liquid level measurement is independent of the liquid, which can be achieved using the 3-electrode design described above. Moreover, isolate the sensor from environmental interferences such as a human body, other objects, or EMI.

### 7.2.2 Detailed Design Procedure

In capacitive sensing systems, the design of the sensor plays an important role in determining system performance and capabilities. In most cases the sensor is simply a metal plate that can be designed on the PCB.

The sensor used in this example is implemented with a two-layer PCB. On the top layer, which faces the tank, there are the 3 electrodes (reference environmental, reference liquid, and level) with a ground plane surrounding the electrodes.

Depending on the shape of the container, the FDC can be located on the sensor PCB to minimize the length of the traces between the input channels and the sensors. In case the shape of the container or other mechanical constraints do not allow having the sensors and the FDC on the same PCB, the traces which connect the channels to the sensor need to be shielded with the appropriate shield.

#### 7.2.2.1 Recommended Initial Register Configuration Values

The application requires 100SPS ($T_{SAMPLE}$ = 10ms). A sensor with an 18-µH inductor and a 33pF capacitor is used. Additional pin, trace, and wire capacitance accounts for 20pF, so the total capacitance is 53pF.

Using L and C, $f_{SENSOR} = 1/2\pi\sqrt{(LC)} = 1/2\pi\sqrt{(18 \times 10^{-6} \times 50 \times 10^{-12})}$ = 5.15MHz. This represents the maximum sensor frequency. When the sensor capacitance is added, the frequency decreases.

Using a system controller clock of 40MHz applied to the CLKIN pin allows flexibility for setting the internal clock frequencies. The sensor coils are connected to channel 0 (IN0A and IN0B pins), channel 1 (IN1A and IN1B pins), and channel 2 (IN2A and IN2B pins).

After powering on the FDC, the FDC enters into Sleep Mode. Program the registers as follows (example sets registers for channel 0 only; channel 1 and channel 2 registers can use equivalent configuration):

1. Set the dividers for channel 0.
   a. The sensor is in an single-ended configuration, therefore set the sensor frequency select register to 2, which means setting field CH0_FIN_SELto b10.
   b. The design constraint for $f_{REF0}$ is > 4 × $f_{SENSOR}$. To satisfy this constraint, $f_{REF0}$ must be greater than 20.6MHz, so set the reference divider to 1. This is done by setting the CH0_FREF_DIVIDER field to 0x01.
   c. The combined value for Chan. 0 divider register (0x14) is 0x2001.
2. Sensor drive current: to ensure that the oscillation amplitude is between 1.2V and 1.8V, measure the oscillation amplitude on an oscilloscope and adjust the IDRIVE value, or use the integrated FDC GUI feature to determine the optimal setting. In this case, set the IDRIVE value to 15 (decimal), which results in an oscillation amplitude of 1.68V(pk). Set the INIT_DRIVE current field to 0x00. The combined value for the DRIVE_CURRENT_CH0 register (addr 0x1E) is 0x7C00.
3. Program the settling time for Channel 0 (see *Multi-Channel and Single-Channel Operation*).
   a. CHx_SETTLECOUNT > $V_{pk} \times f_{REFx} \times C \times \pi^2 / (32 \times IDRIVE_X) \rightarrow 7.5$, rounded up to 8. To provide margin to account for system tolerances, a higher value of 10 is chosen.
   b. Program Register 0x10 to a minimum of 10.
   c. The settle time is: (10 × 16)/40,000,000 = 4µs
   d. The value for Channel 0 SETTLECOUNT register (0x10) is 0x000A.
4. The channel switching delay is approximately 1µs for $f_{REF}$ = 40MHz (see *Multi-Channel and Single-Channel Operation*)
5. Set the conversion time by the programming the reference count for Channel 0. The budget for the conversion time is : 1/N × ($T_{SAMPLE}$ – settling time – channel switching delay) = 1/3 (10,000 – 4 – 1) = 3.33ms
   a. To determine the conversion time register value, use the following equation and solve for CH0_RCOUNT: Conversion Time ($t_{C0}$)= (CH0_RCOUNT × 16)/$f_{REF0}$.
   b. This results in CH0_RCOUNT having a value of 8329 decimal (rounded down). Note that this yields an ENOB > 13 bits.


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c. Set the CH0_RCOUNT register (0x08) to 0x2089.
6. Use the default values for the ERROR_CONFIG register (address 0x19). By default, no interrupts are enabled
7. Program the MUX_CONFIG register
   a. Set the AUTOSCAN_EN to b1 bit to enable sequential mode
   b. Set RR_SEQUENCE to b10 to enable data conversion on three channels (channel 0, channel 1, channel 2)
   c. Set DEGLITCH to b101 to set the input deglitch filter bandwidth to 10MHz, the lowest setting that exceeds the oscillation tank frequency.
   d. The combined value for the MUX_CONFIG register (address 0x1B) is 0xC20D
8. Finally, program the CONFIG register as follows:
   a. Set the ACTIVE_CHAN field to b00 to select channel 0.
   b. Set SLEEP_MODE_EN field to b0 to enable conversion.
   c. Set SENSOR_ACTIVATE_SEL = b0, for full current drive during sensor activation
   d. Set the REF_CLK_SRC field to b1 to use the external clock source.
   e. Set the other fields to their default values.
   f. The combined value for the CONFIG register (address 0x1A) is 0x1601.

We then read the conversion results for channel 0 to channel 2 every 10ms from register addresses 0x00 to 0x05.

Based on the example configuration above, TI recommends the following register write sequence

is recommended:

**Table 7-1. Recommended Initial Register Configuration Values (Multi-Channel Operation)**

| ADDRESS | VALUE | REGISTER NAME | COMMENTS |
|---|---|---|---|
| 0x08 | 0x8329 | RCOUNT_CH0 | Reference count calculated from timing requirements (100SPS) and resolution requirements |
| 0x09 | 0x8329 | RCOUNT_CH1 | Reference count calculated from timing requirements (100SPS) and resolution requirements |
| 0x0A | 0x8329 | RCOUNT_CH2 | Reference count calculated from timing requirements (100SPS) and resolution requirements |
| 0x10 | 0x000A | SETTLECOUNT_CH0 | Minimum settling time for chosen sensor |
| 0x11 | 0x000A | SETTLECOUNT_CH1 | Minimum settling time for chosen sensor |
| 0x12 | 0x000A | SETTLECOUNT_CH2 | Minimum settling time for chosen sensor |
| 0x14 | 0x2002 | CLOCK_DIVIDER_CH0 | CH0_FIN_DIVIDER = 1, CH0_FREF_DIVIDER = 2 |
| 0x15 | 0x2002 | CLOCK_DIVIDER_CH1 | CH1_FIN_DIVIDER = 1, CH1_FREF_DIVIDER = 2 |
| 0x16 | 0x2002 | CLOCK_DIVIDER_CH2 | CH1_FIN_DIVIDER = 1, CH1_FREF_DIVIDER = 2 |
| 0x19 | 0x0000 | ERROR_CONFIG | Can be changed from default to report status and error conditions |
| 0x1B | 0xC20D | MUX_CONFIG | Enable Ch 0 , Ch 1, and Ch 2 (sequential mode), set Input deglitch bandwidth to 10MHz |
| 0x1E | 0x7C00 | DRIVE_CURRENT_CH0 | Sets sensor drive current on ch 0 |
| 0x1F | 0x7C00 | DRIVE_CURRENT_CH1 | Sets sensor drive current on ch 1 |
| 0x20 | 0x7C00 | DRIVE_CURRENT_CH2 | Sets sensor drive current on ch 2 |
| 0x1A | 0x1601 | CONFIG | Enable full current drive during sensor activation, select external clock source, wake up device to start conversion. This register write must occur last because device configuration is not permitted while the FDC is in active mode. |

### *7.2.3 Application Curve*

A liquid level sensor with 3 electrodes like the one shown in the schematic was connected to the EVM. The plot shows the capacitance measured by Level sensor at different levels of liquid in the tank. The capacitance of the Reference Liquid and Reference Environmental sensors have a steady value because they experience

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consistent exposure to liquid and air, while the capacitance of the level sensor (Level) increases linearly with the height of the liquid in the tank.

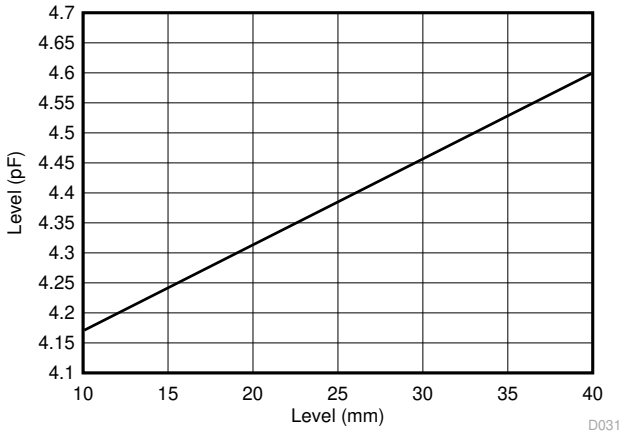



**Figure 7-8. Electrode Capacitance vs Liquid Level**

## 7.3 Best Design Practices

- Do leave a small gap between sensor plates in differential configurations. TI recommends a 2mm to 3mm minimum separation.
- The FDC does not support hot-swapping of the sensors. Do not hot-swap sensors, for example by using external multiplexers.

## 7.4 Power Supply Recommendations

The FDC requires a voltage supply within 2.7V and 3.6V. TI recommends multilayer ceramic bypass X7R capacitors of 0.1µF and 1µF between the VDD and GND pins. If the supply is located more than a few inches from the FDC, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 10µF is a typical choice.

The optimum placement is closest to the VDD and GND pins of the device. Take care to minimize the loop area formed by the bypass capacitor connection, the VDD pin, and the GND pin of the device. See Figure 7-9 and Figure 7-12 for layout examples.

## 7.5 Layout

### *7.5.1 Layout Guidelines*

- Avoid long traces to connect the sensor to the FDC. Short traces reduce parasitic capacitances between sensor inductor and offer higher system performance.
- Systems that require matched channel response need to have matched trace length on all active channels.

### *7.5.2 Layout Examples*

Figure 7-9 to Figure 7-12 show the FDC2114 / FDC2214 evaluation module (EVM) layout.


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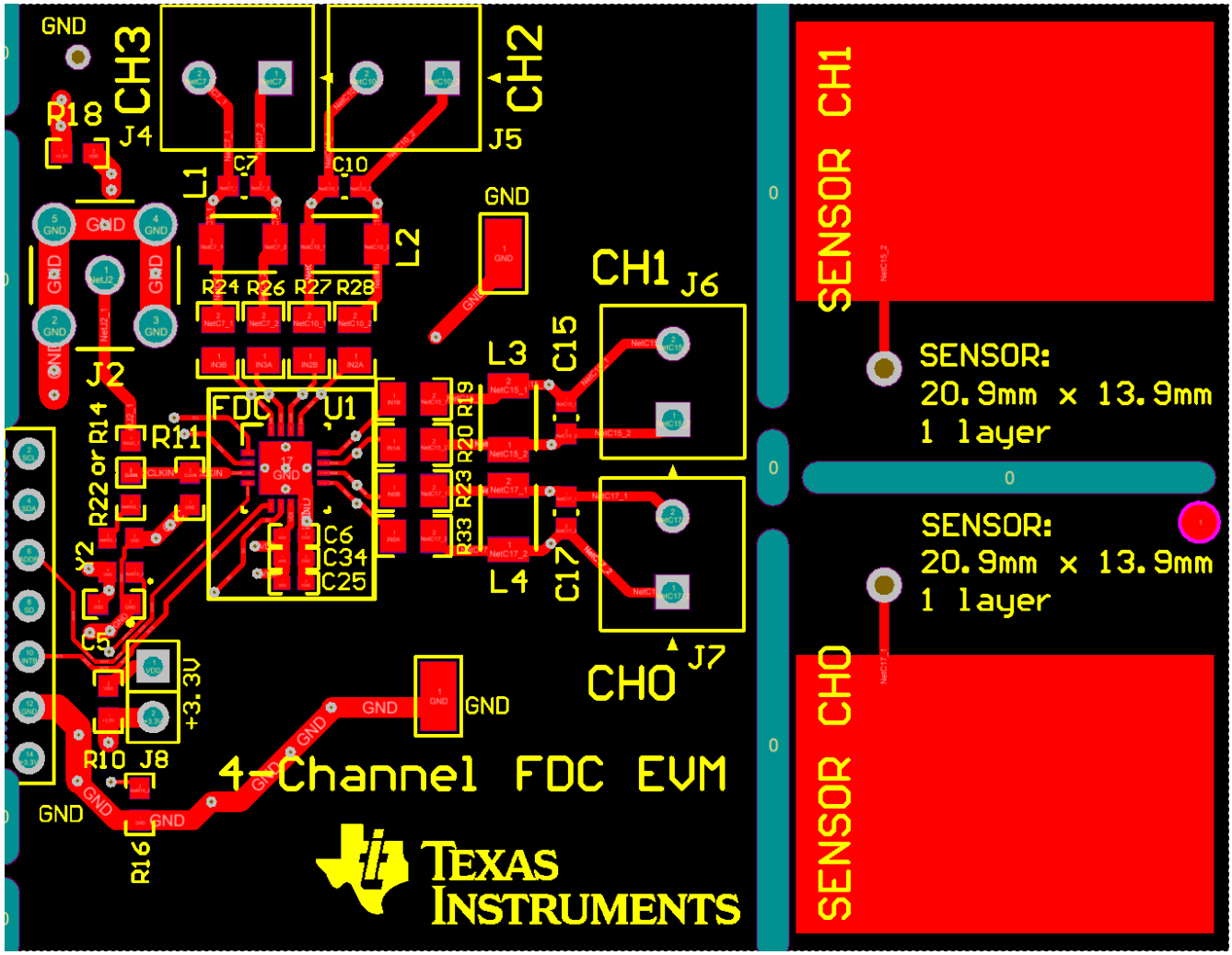



**Figure 7-9. Example PCB Layout: Top Layer (Signal)**

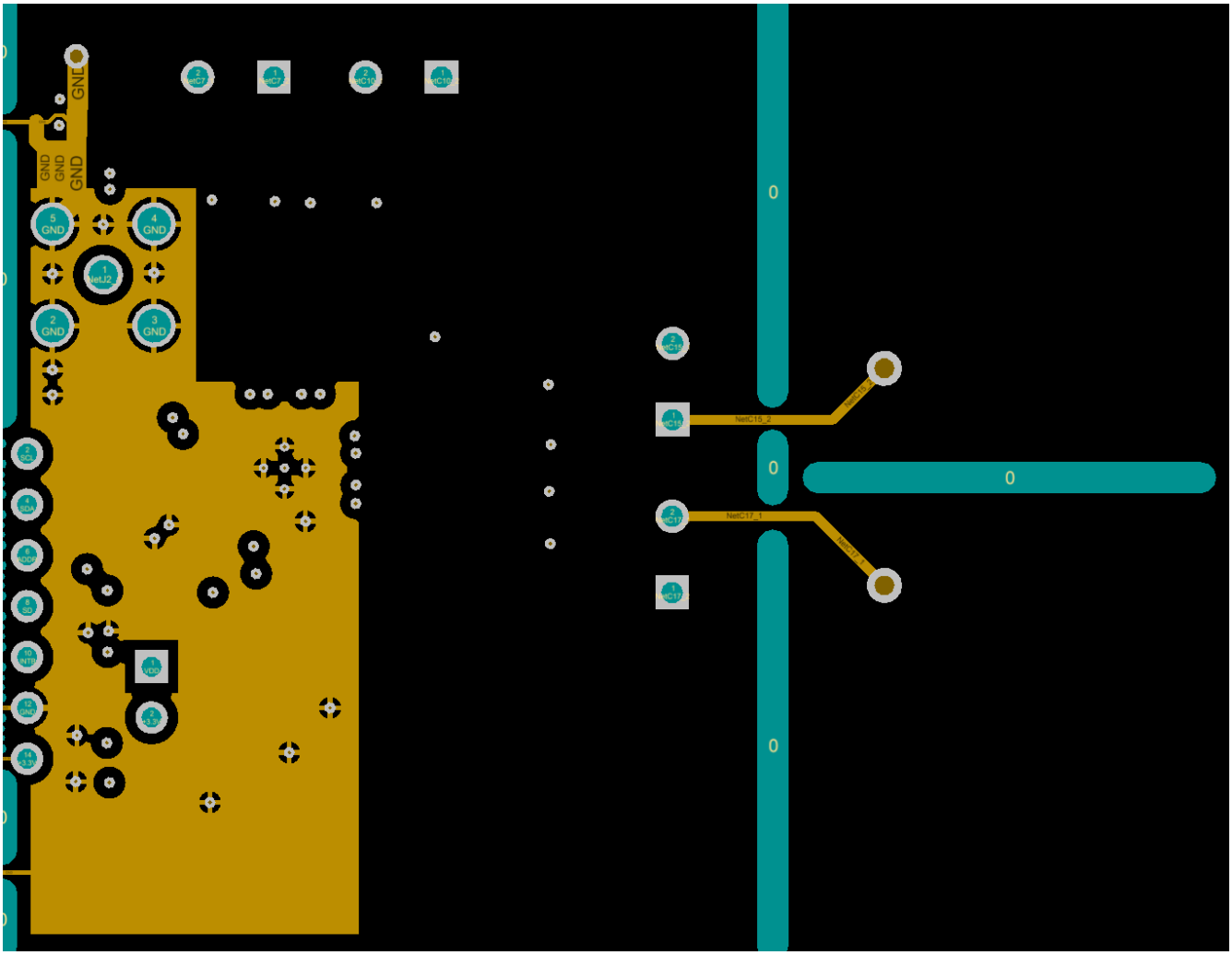



**Figure 7-10. Example PCB Layout: Mid-Layer 1 (GND)**


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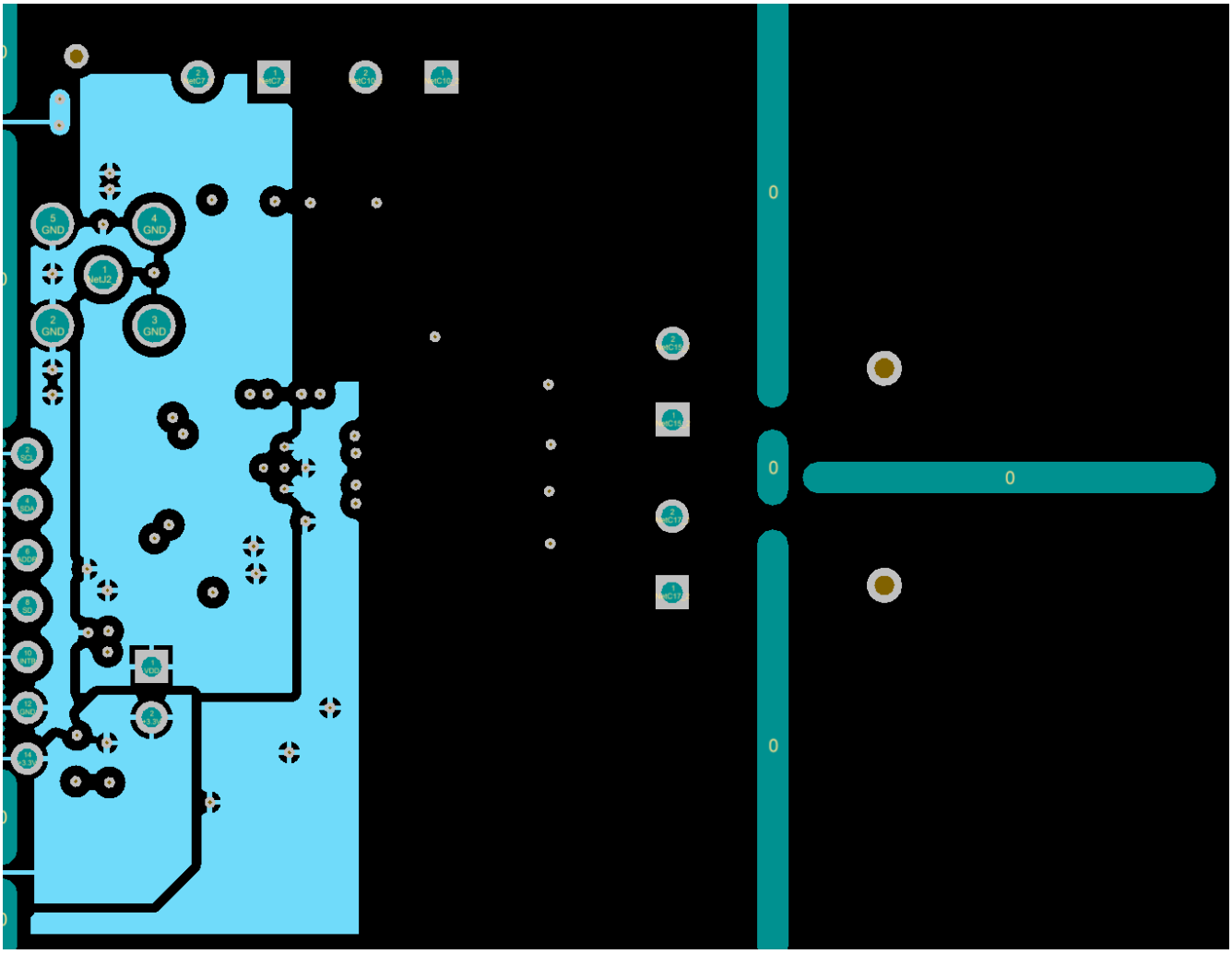



**Figure 7-11. Example PCB Layout: Mid-Layer 2 (Power)**

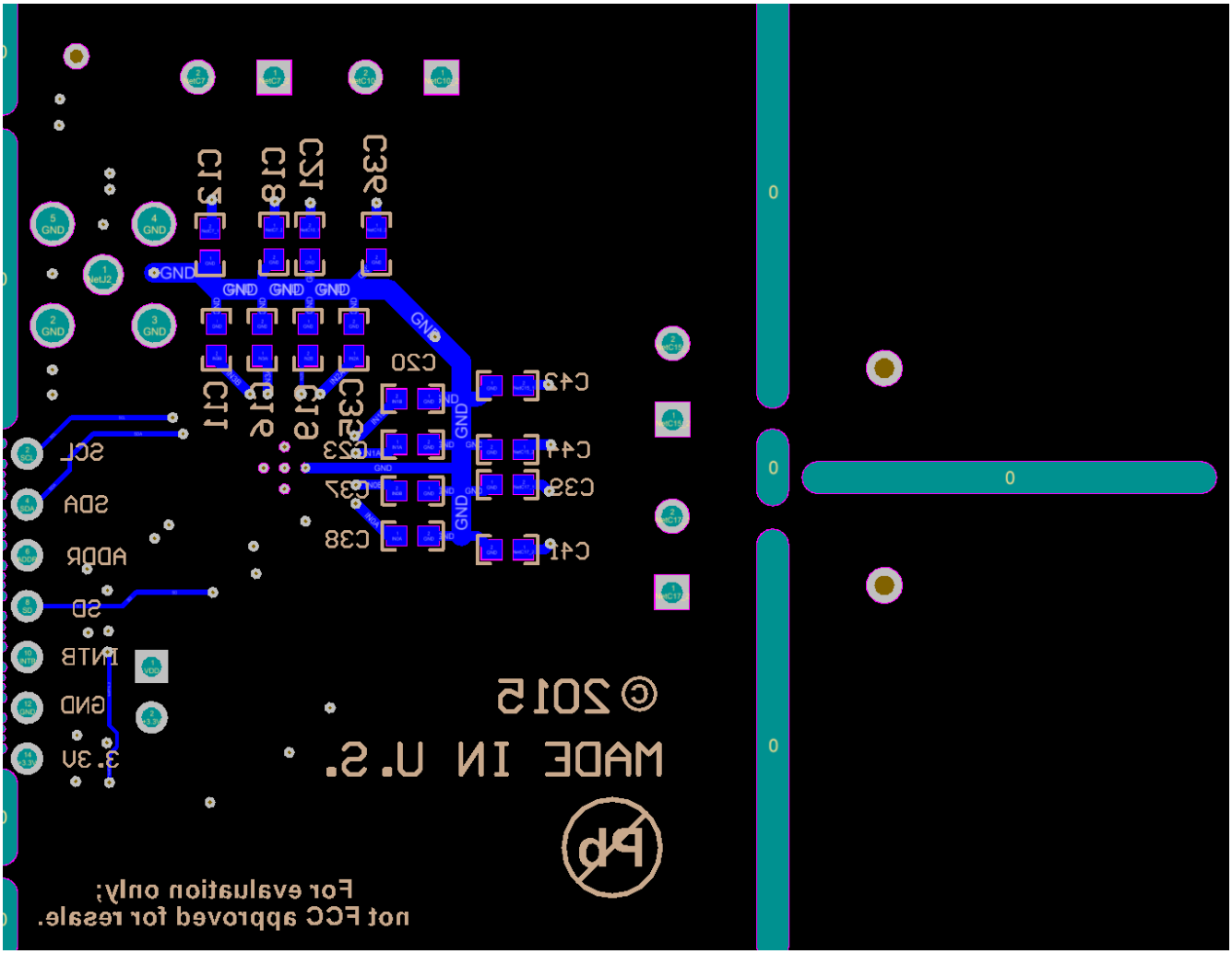



**Figure 7-12. Example PCB Layout: Bottom Layer (Signal)**


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# 8 Device and Documentation Support

## 8.1 Device Support

### *8.1.1 Development Support*

For related links, see the following:

Texas Instruments' WEBENCH® tool: http://www.ti.com/webench

## 8.2 Documentation Support

### *8.2.1 Related Documentation*

For related documentation, refer to the following:

For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953)

## 8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.7 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 9 Revision History

| Changes from Revision * (May 2016) to Revision A (October 2024) | Page |
|---|---|
| • Changed data sheet title from: FDC2112-Q1, FDC2114-Q1, FDC2212-Q1, FDC2214-Q1 Multi-Channel 12-Bit or 28-Bit Capacitance-to-Digital Converter (FDC) for Capacitive Sensing to: FDC2x1x-Q1 Multi-Channel, High Resolution Capacitance-to-Digital Converter for Capacitive Sensing Applications | 1 |
| • Updated the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Changed all instances of legacy terminology to controller and target where $I^2C$ is mentioned | 1 |
| • Changed *Device Information* table to *Package Information* | 1 |

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## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| FDC2112QDNTRQ1 | Active | Production | WSON (DNT) \| 12 | 4500 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 125 | FDC2112 Q1 |
| FDC2112QDNTRQ1.B | Active | Production | WSON (DNT) \| 12 | 4500 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 125 | FDC2112 Q1 |
| FDC2114QRGHRQ1 | Active | Production | WQFN (RGH) \| 16 | 4500 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 125 | FC2114Q |
| FDC2114QRGHRQ1.B | Active | Production | WQFN (RGH) \| 16 | 4500 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 125 | FC2114Q |
| FDC2114QRGHTQ1 | Obsolete | Production | WQFN (RGH) \| 16 | - | - | Call TI | Call TI | -40 to 125 | FC2114Q |
| FDC2212QDNTRQ1 | Active | Production | WSON (DNT) \| 12 | 4500 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 125 | FDC2212 Q1 |
| FDC2212QDNTRQ1.B | Active | Production | WSON (DNT) \| 12 | 4500 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 125 | FDC2212 Q1 |
| FDC2212QDNTTQ1 | Obsolete | Production | WSON (DNT) \| 12 | - | - | Call TI | Call TI | -40 to 125 | FDC2212 Q1 |
| FDC2214QRGHRQ1 | Active | Production | WQFN (RGH) \| 16 | 4500 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 125 | FC2214Q |
| FDC2214QRGHRQ1.B | Active | Production | WQFN (RGH) \| 16 | 4500 \| LARGE T&R | Yes | SN | Level-3-260C-168 HR | -40 to 125 | FC2214Q |
| FDC2214QRGHTQ1 | Obsolete | Production | WQFN (RGH) \| 16 | - | - | Call TI | Call TI | -40 to 125 | FC2214Q |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF FDC2112-Q1, FDC2114-Q1, FDC2212-Q1, FDC2214-Q1 :**

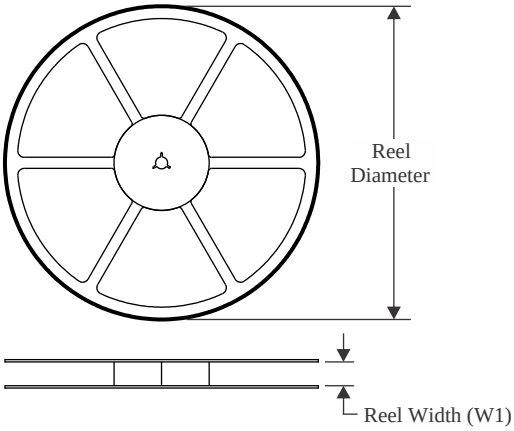
- Catalog : FDC2112, FDC2114, FDC2212, FDC2214

NOTE: Qualified Version Definitions:

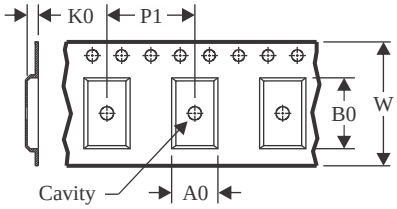
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

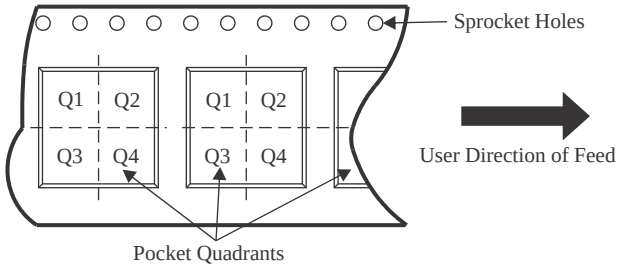



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

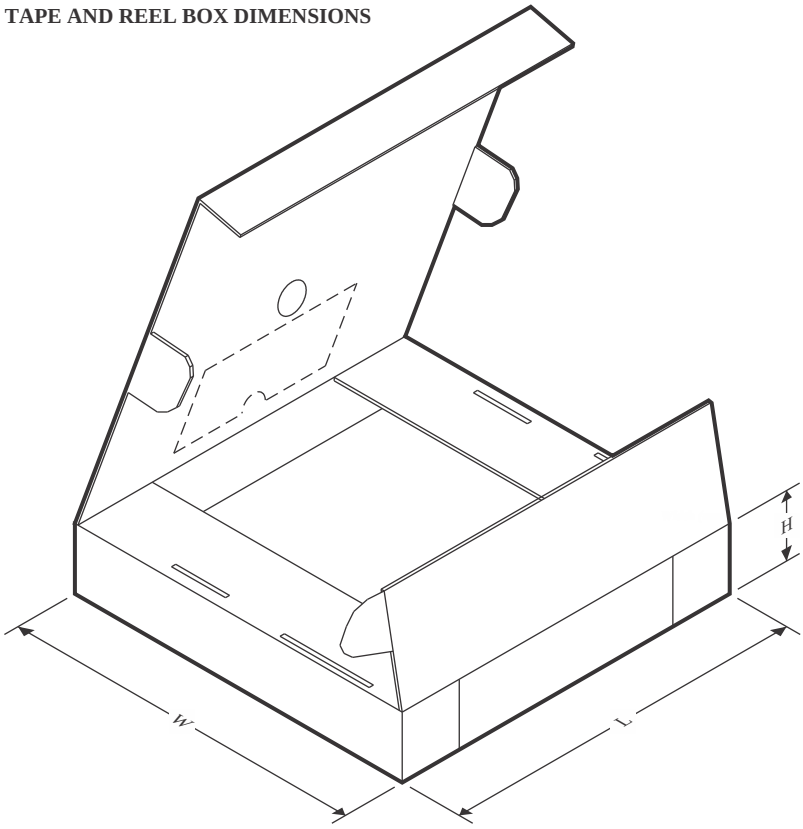
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FDC2112QDNTRQ1 | WSON | DNT | 12 | 4500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| FDC2114QRGHRQ1 | WQFN | RGH | 16 | 4500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| FDC2212QDNTRQ1 | WSON | DNT | 12 | 4500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| FDC2214QRGHRQ1 | WQFN | RGH | 16 | 4500 | 330.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

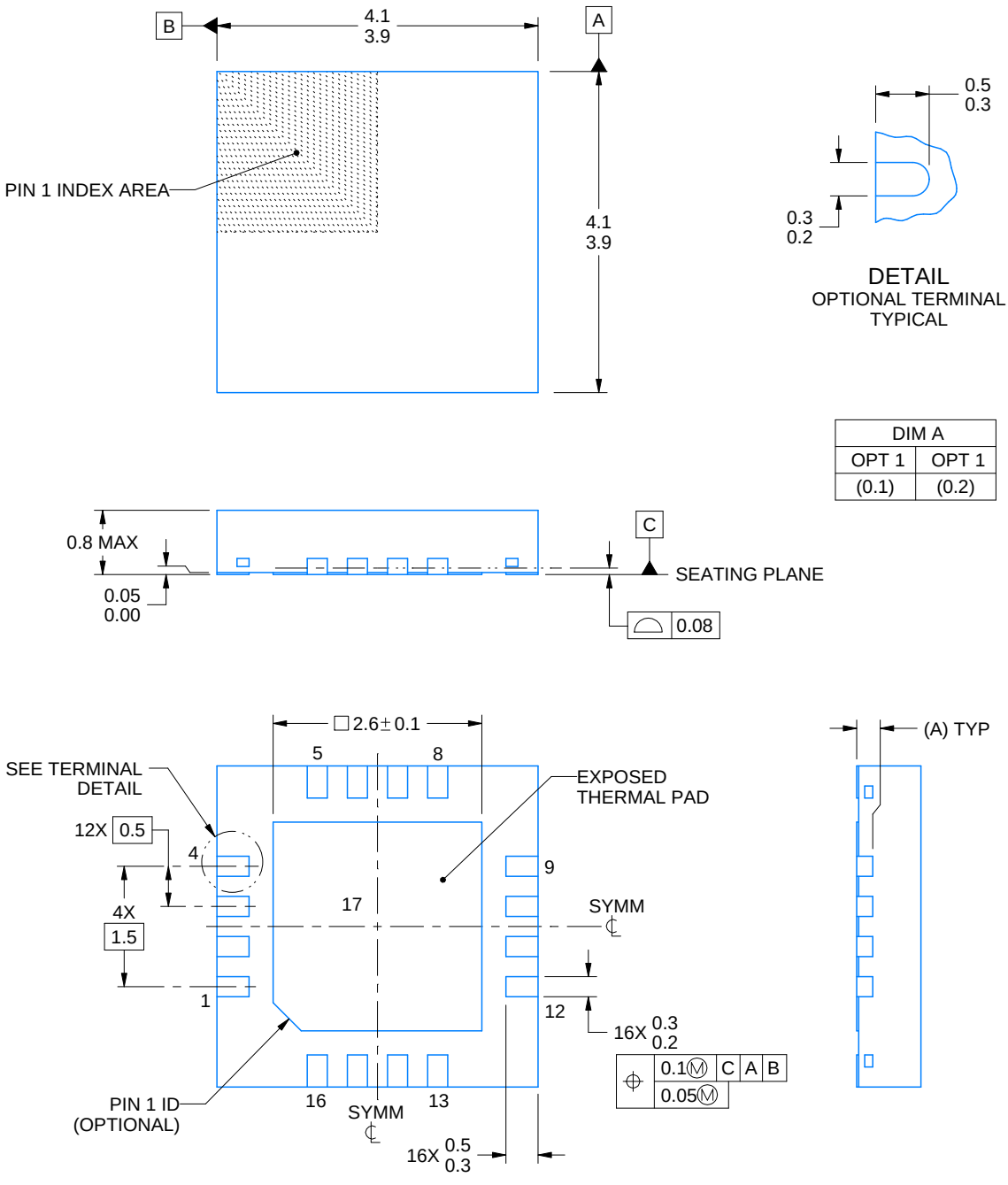
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| FDC2112QDNTRQ1 | WSON | DNT | 12 | 4500 | 356.0 | 356.0 | 36.0 |
| FDC2114QRGHRQ1 | WQFN | RGH | 16 | 4500 | 356.0 | 356.0 | 36.0 |
| FDC2212QDNTRQ1 | WSON | DNT | 12 | 4500 | 356.0 | 356.0 | 36.0 |
| FDC2214QRGHRQ1 | WQFN | RGH | 16 | 4500 | 356.0 | 356.0 | 36.0 |

# PACKAGE OUTLINE

## RGH0016A

## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




NOTES:

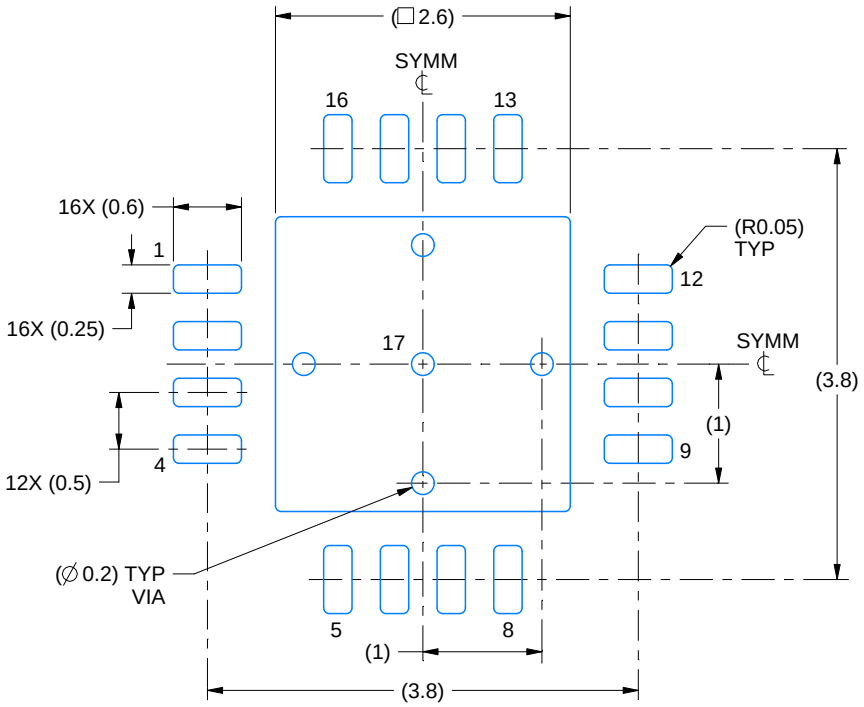
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

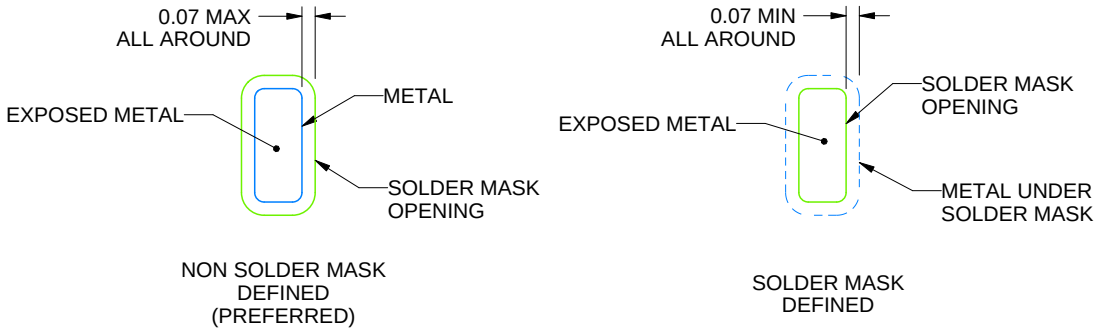
## RGH0016A

## WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

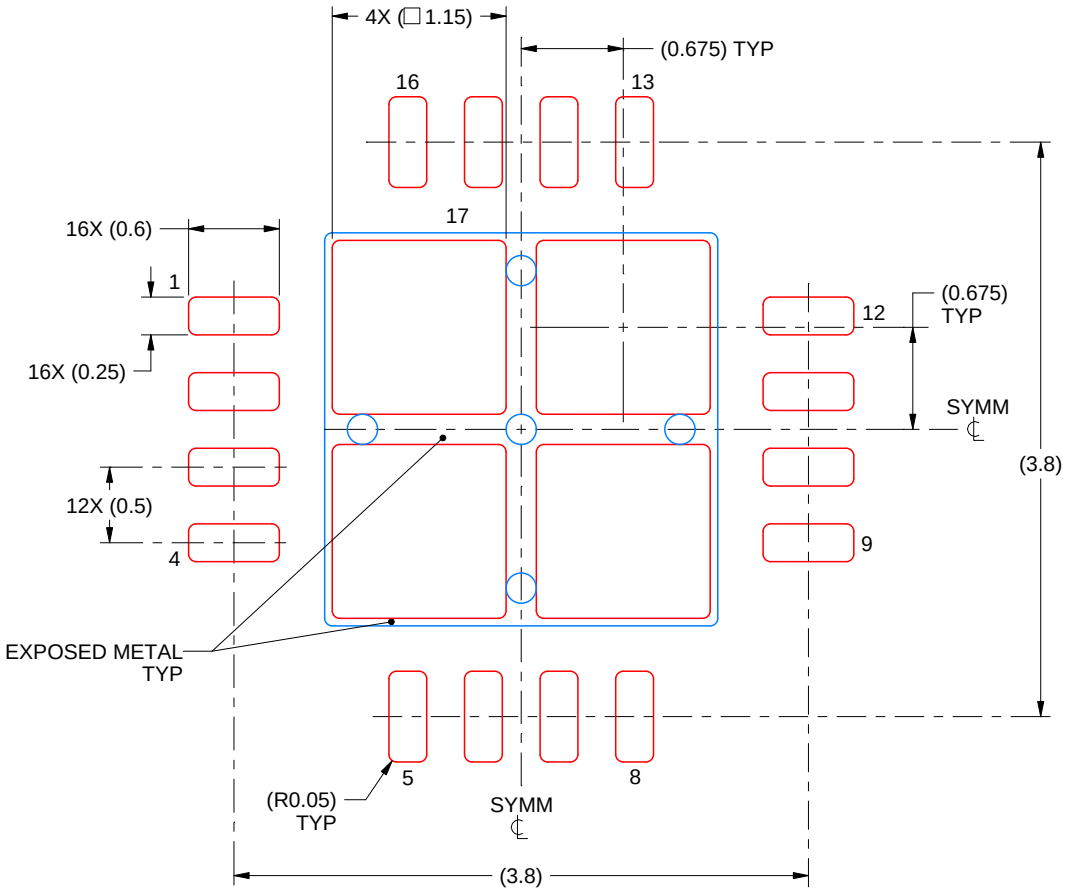



SOLDER MASK DETAILS

4214978/B 01/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214978/B 01/2017

NOTES: (continued)

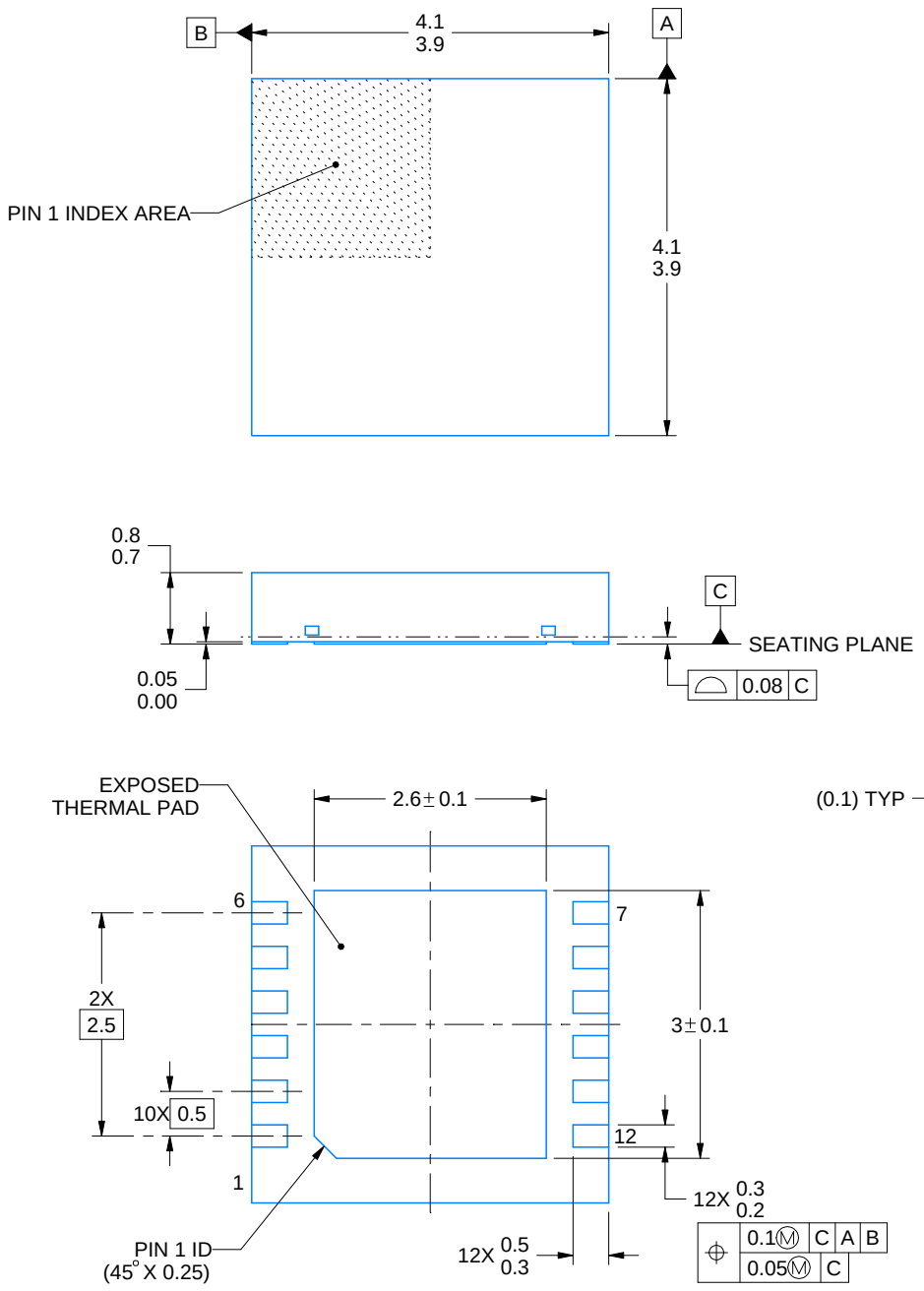
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# DNT0012B

# PACKAGE OUTLINE

## WSON - 0.8 mm max height

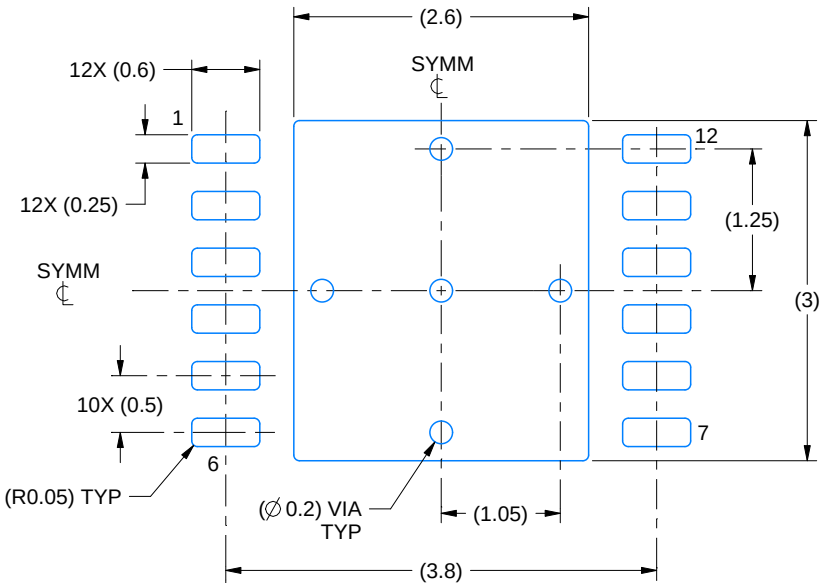
PLASTIC SMALL OUTLINE - NO LEAD



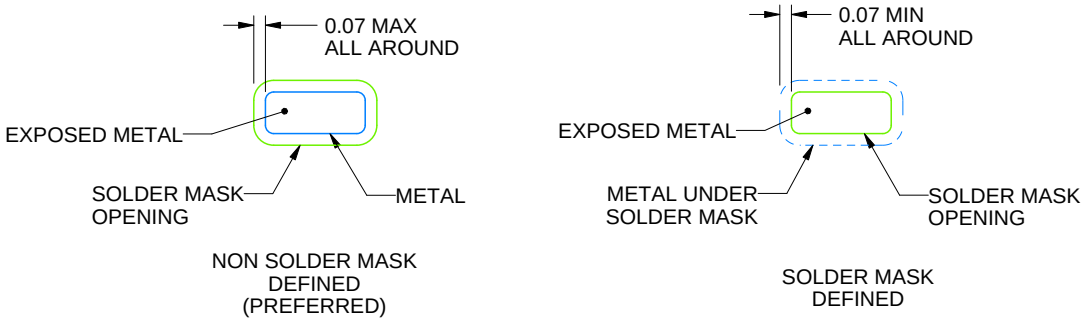

4214928/C 10/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

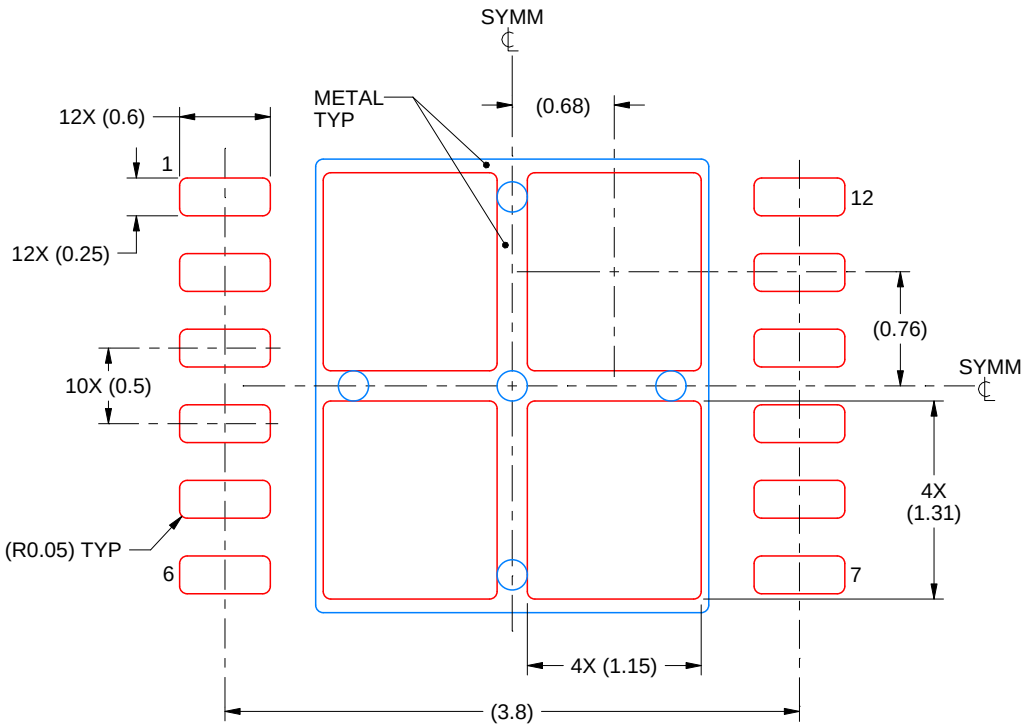



SOLDER MASK DETAILS

4214928/C 10/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4214928/C 10/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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