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June 2016

FDD7N25LZ

N-Channel UniFET™ MOSFET

250 V, 6.2 A, 550 mΩ

Features

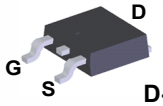
- $R_{DS(on)}$ = 430 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 3.1 A
- Low Gate Charge (Typ. 12 nC)
- Low C_{rss} (Typ. 8 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

Applications

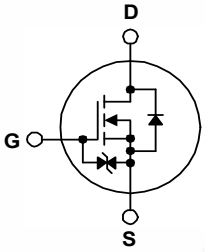
- LCD/LED/PDP TV
- Consumer Appliances
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



D-PAK



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FDD7N25LZTM	Unit
V_{DSS}	Drain to Source Voltage		250	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current	- Continuous (T_C = 25°C)	6.2	A
		- Continuous (T_C = 100°C)	3.7	
I_{DM}	Drain Current	- Pulsed (Note 1)	25	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	115	mJ
I_{AR}	Avalanche Current	(Note 1)	5.5	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	5.6	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	10	V/ns
P_D	Power Dissipation	(T_C = 25°C)	56	W
		- Derate Above 25°C	0.45	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FDD7N25LZTM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	110	

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Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDD7N25LZTM	FDD7N25LZ	DPAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V, T_C = 25°C	250	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	-	0.25	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 250 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 200 V, T_C = 125°C	-	-	10	
I_{GSSF}	Gate to Body Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V	-	-	10	μA
I_{GSSR}	Gate to Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	-	-	-10	μA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.0	-	2.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 3.1 A	-	0.43	0.55	Ω
		V_{GS} = 5 V, I_D = 3.1 A	-	0.45	0.57	
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 3.1 A	-	7	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	-	480	635	pF
C_{oss}	Output Capacitance		-	65	85	pF
C_{rss}	Reverse Transfer Capacitance		-	8	12	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 250 V I_D = 6.2 A, V_{GS} = 10 V (Note 4)	-	12	16	nC
Q_{gs}	Gate to Source Gate Charge		-	1.5	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	4	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 6.2 A, V_{GS} = 10 V, R_G = 25 Ω (Note 4)	-	10	30	ns
t_r	Turn-On Rise Time		-	15	40	ns
$t_{d(off)}$	Turn-Off Delay Time		-	75	160	ns
t_f	Turn-Off Fall Time		-	30	70	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	6.2	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	25	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 6.2 A	-	-	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 6.2 A, dI_F/dt = 100 A/μs	-	130	-	ns
Q_{rr}	Reverse Recovery Charge		-	0.6	-	μC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 6 mH, I_{AS} = 6.2 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \le 6.2$ A, di/dt ≤ 200 A/μs, $V_{DD} \le BV_{DSS}$, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

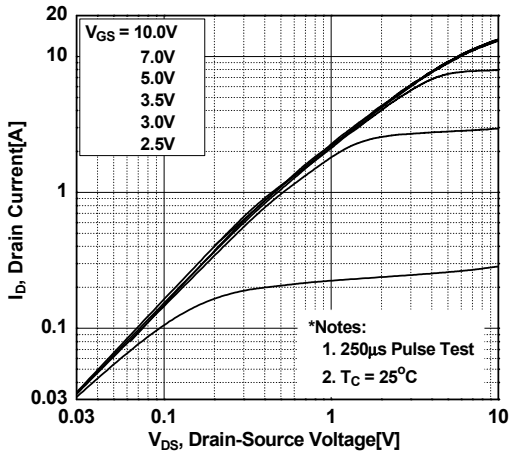


Figure 2. Transfer Characteristics

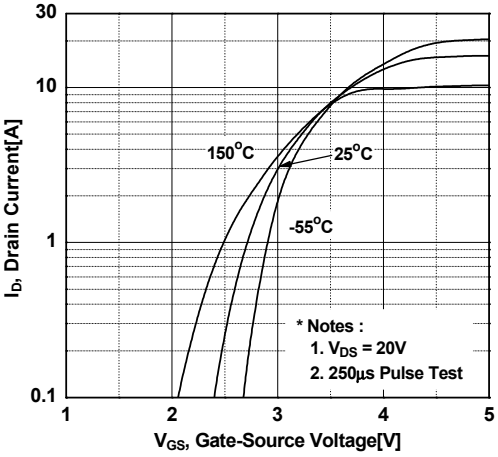


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

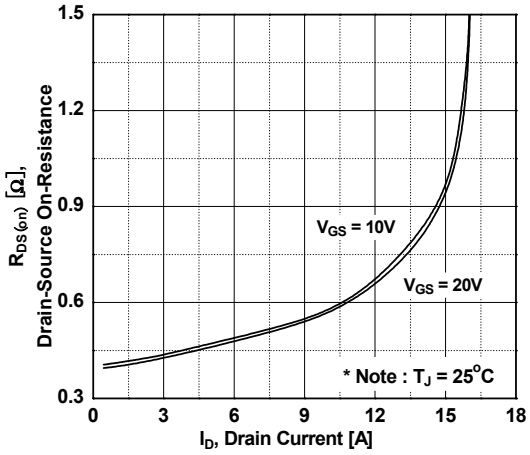


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

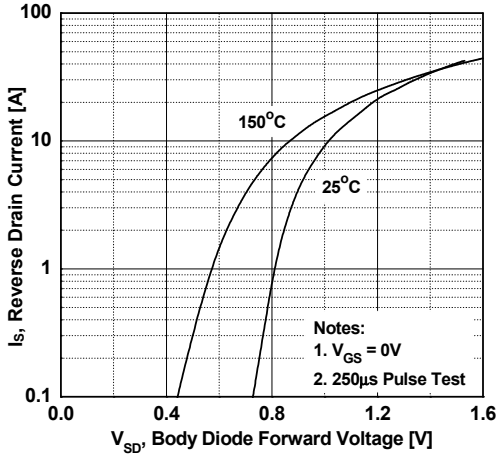


Figure 5. Capacitance Characteristics

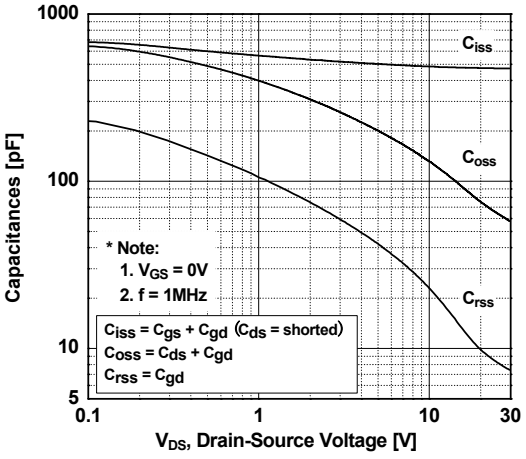
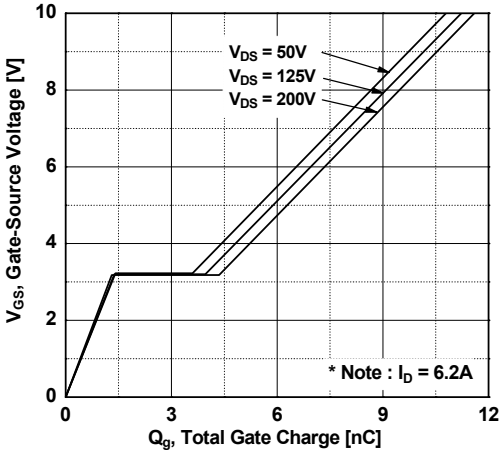


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

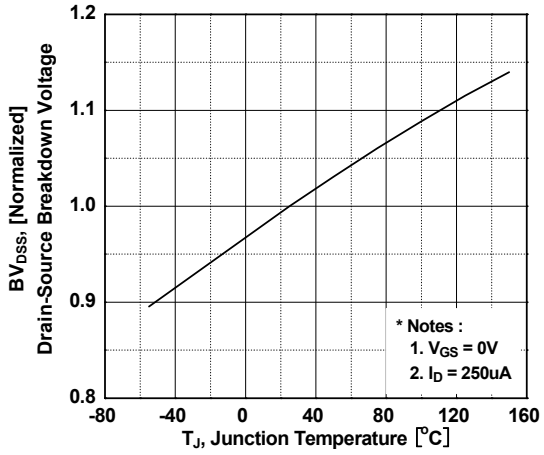


Figure 8. On-Resistance Variation vs. Temperature

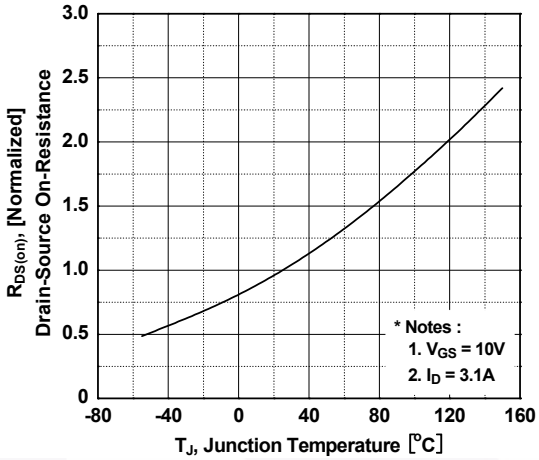


Figure 9. Maximum Safe Operating Area

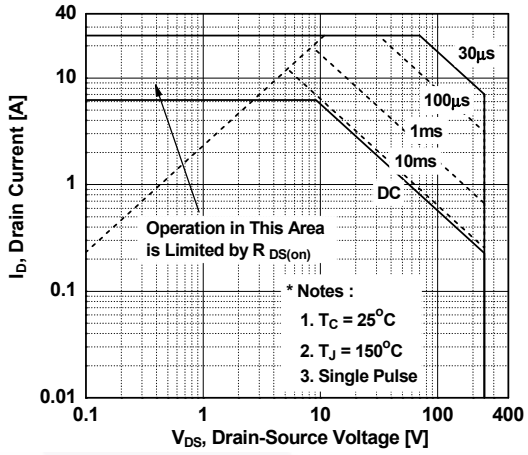


Figure 10. Maximum Drain Current vs. Case Temperature

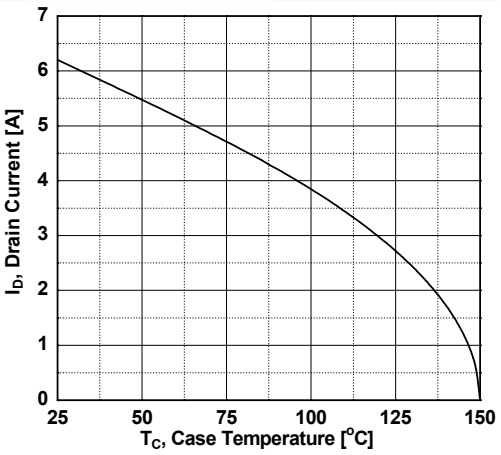
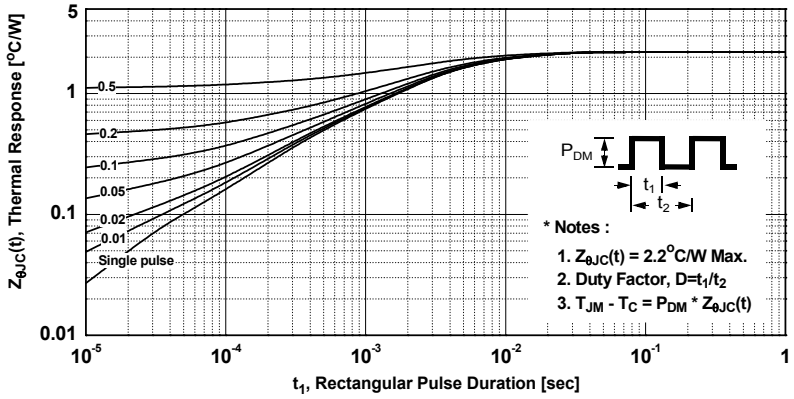


Figure 11. Transient Thermal Response Curve



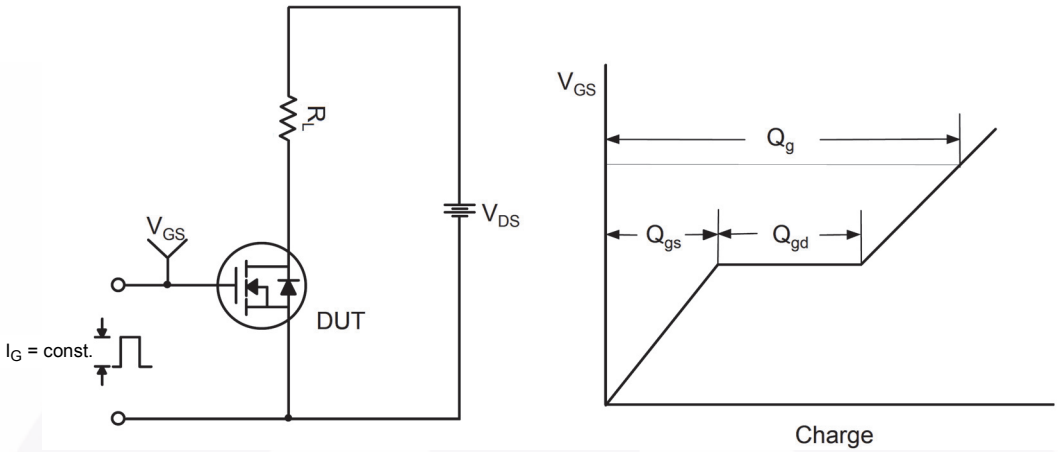


Figure 12. Gate Charge Test Circuit & Waveform

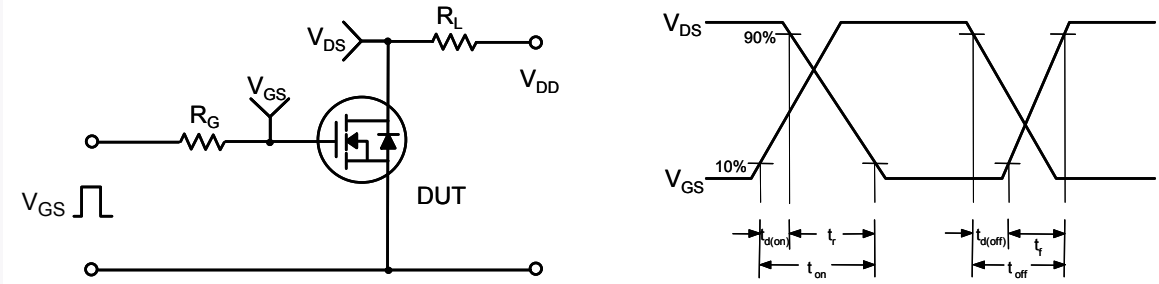


Figure 13. Resistive Switching Test Circuit & Waveforms

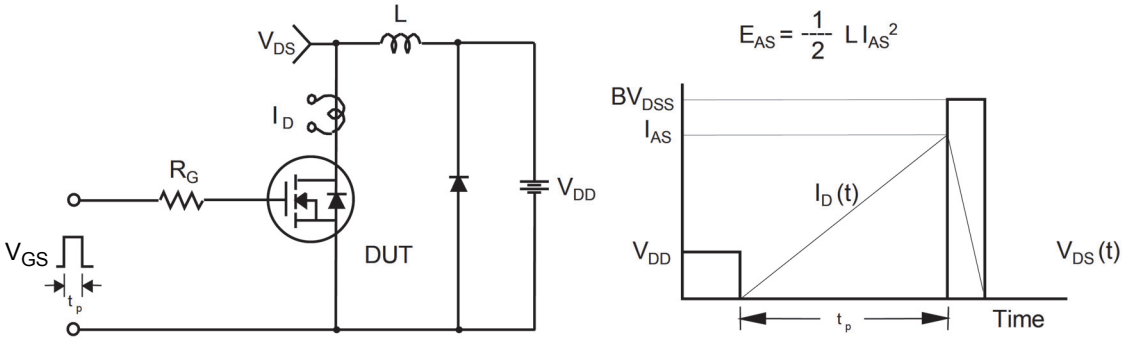


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

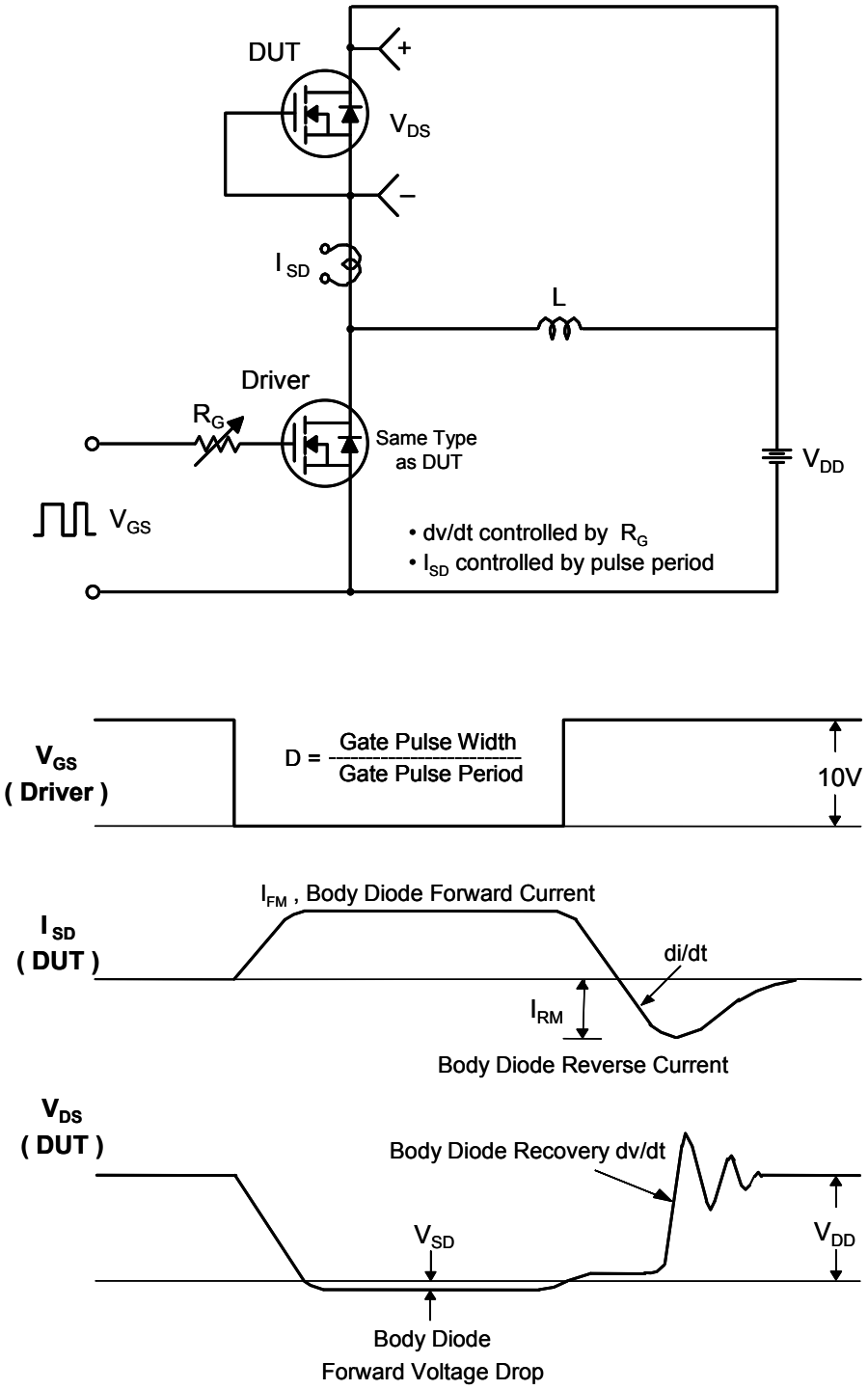
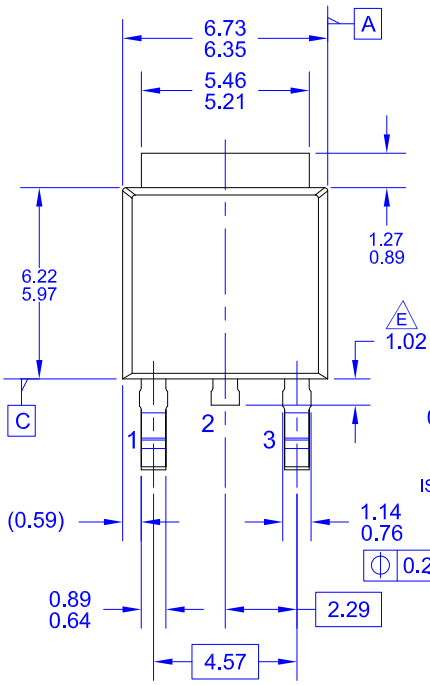
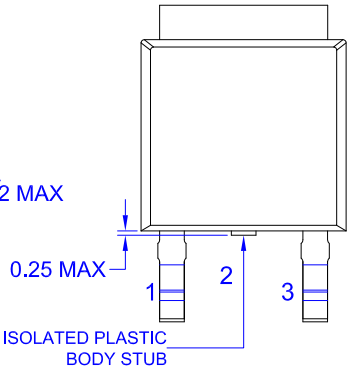


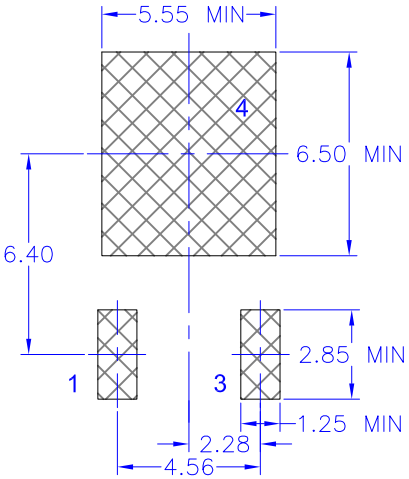
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



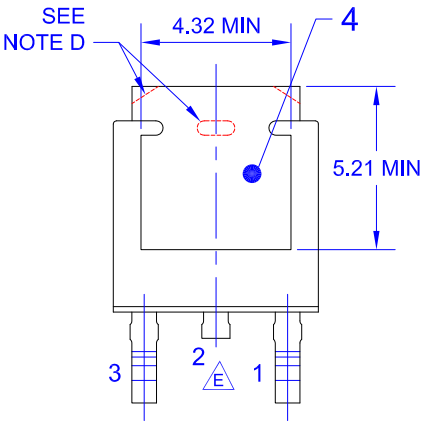
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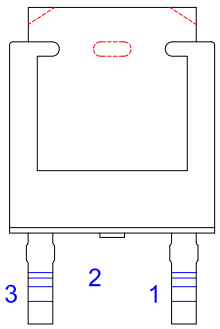
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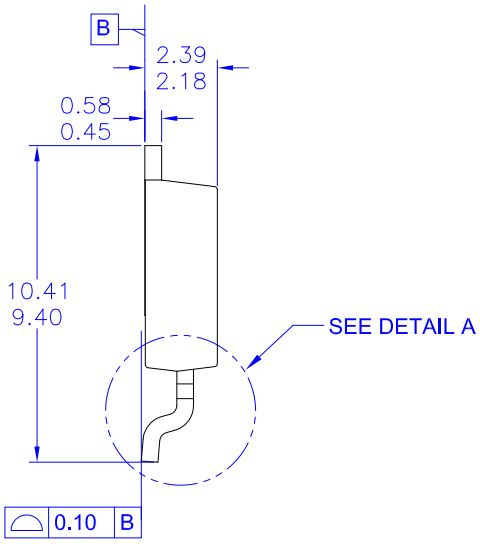
LAND PATTERN RECOMMENDATION



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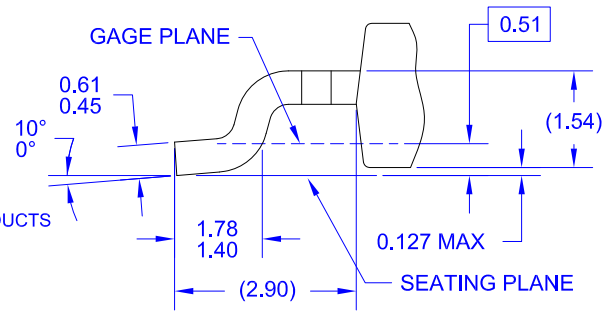


DIODE PRODUCTS VERSION



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B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



DETAIL A
(ROTATED -90°)
SCALE: 12X

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