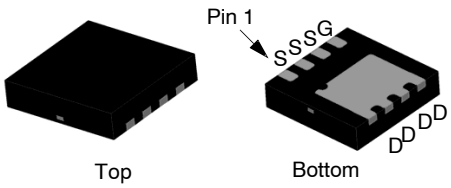
MOSFET – N-Channel, POWERTRENCH®, SyncFET™

30 V, 18 A, 9.3 mΩ

FDMC7692S



WDFN8 3.3x3.3, 0.65P
CASE 511DQ (Option A)

General Description

This FDMC7692S is produced using **onsemi's** advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

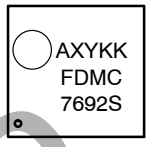
Features

- Max $r_{DS(on)}$ = 9.3 mΩ at V_{GS} = 10 V, I_D = 12.5 A
- Max $r_{DS(on)}$ = 13.6 mΩ at V_{GS} = 4.5 V, I_D = 10.4 A
- High Performance Technology for Extremely Low $r_{DS(on)}$
- These Devices are Pb-Free and are RoHS Compliant

Applications

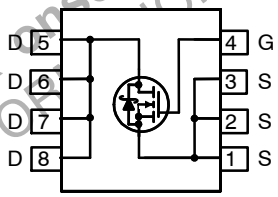
- DC – DC Buck Converters
- Notebook DC – DC Application

MARKING DIAGRAM



FDMC7692S = Specific Device Code
A = Assembly Location
XY = 2-Digit Date Code
KK = 2-Digit Lot Run Traceability Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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MOSFET MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

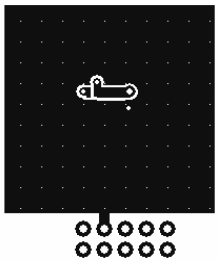
Symbol	Parameter			Rating	Unit
V_{DS}	Drain to Source Voltage			30	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current	Continuous	T_C = 25 °C	18	A
		Continuous (Note 1a)	T_A = 25 °C	12.5	
		Pulsed		45	
E_{AS}	Single Pulse Avalanche Energy (Note 2)			21	mJ
P_D	Power Dissipation		T_C = 25 °C	27	W
	Power Dissipation (Note 1a)		T_A = 25 °C	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			−55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

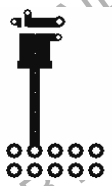
THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.7	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 125 °C/W when mounted on a minimum pad of 2 oz copper

2. E_{AS} of 21 mJ is based on starting T_J = 25 °C; L = 0.3 mH, I_{AS} = 12.0 A, V_{DD} = 27 V, V_{GS} = 10 V. 100% test at L = 3 mH, I_{AS} = 3.2 A.

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V	30	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, referenced to 25 °C	–	16	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	–	–	500	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
ON CHARACTERISTICS (Note 3)						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 1 mA	1.2	2.0	3.0	V
$\Delta V_{GS(th)}$ / ΔT_J	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 10 mA, referenced to 25 °C	–	–5	–	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 12.5 A	–	7.8	9.3	mΩ
		V_{GS} = 4.5 V, I_D = 10.4 A	–	10.8	13.6	
		V_{GS} = 10 V, I_D = 12.5 A, T_J = 125 °C	–	9.6	13.0	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 12.5 A	–	62	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	–	1040	1385	pF
C_{oss}	Output Capacitance		–	445	590	pF
C_{rss}	Reverse Transfer Capacitance		–	40	60	pF
R_g	Gate Resistance	f = 1 MHz	–	1.1	2.9	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 12.5 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	9	17	ns
t_r	Rise Time		–	3	10	ns
$t_{d(off)}$	Turn-Off Delay Time		–	19	34	ns
t_f	Fall Time		–	3	10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 15 V, I_D = 12.5 A	–	16	23	nC
		V_{GS} = 0 V to 4.5 V, V_{DD} = 15 V, I_D = 12.5 A	–	8	10	nC
Q_{gs}	Total Gate Charge	V_{DD} = 15 V, I_D = 12.5 A	–	4	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	2	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 12.5 A (Note 3)	–	0.9	1.3	V
		V_{GS} = 0 V, I_S = 0.9 A (Note 3)	–	0.5	0.7	
t_{rr}	Reverse Recovery Time	I_F = 12.5 A, di/dt = 300 A/μs	–	21	33	ns
Q_{rr}	Reverse Recovery Charge		–	16	29	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

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TYPICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

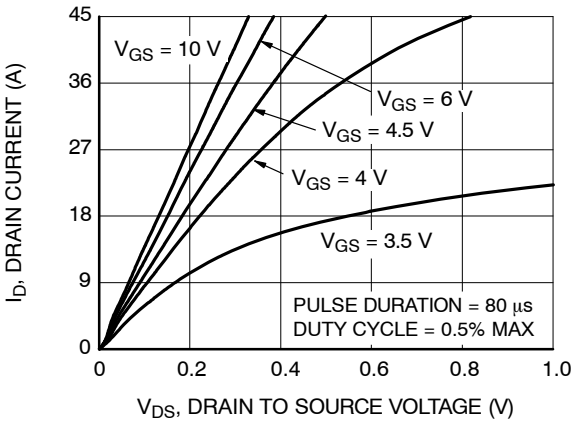

Figure 1. On Region Characteristics

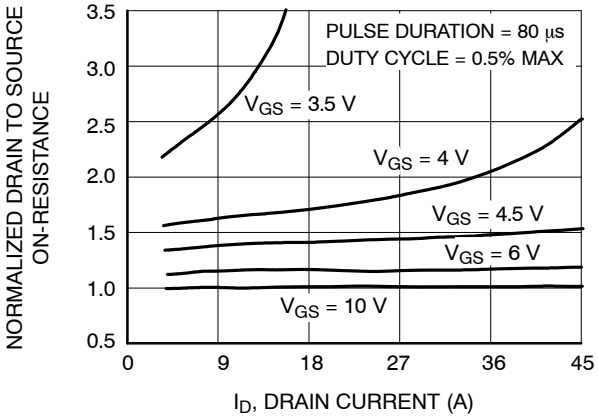

Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

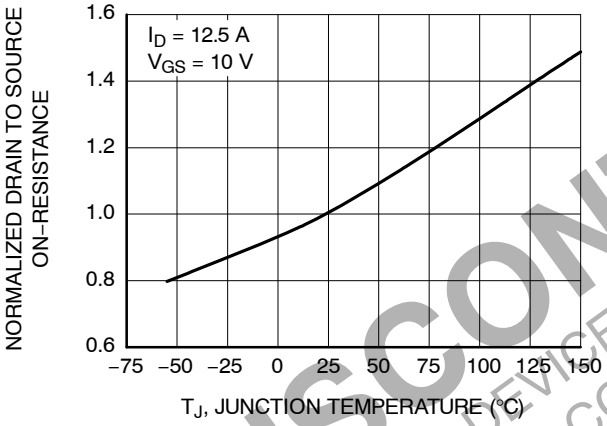

Figure 3. Normalized On Resistance vs. Junction Temperature

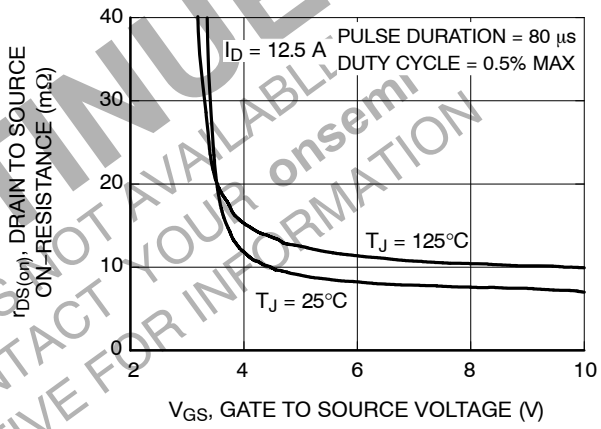

Figure 4. On-Resistance vs. Gate to Source Voltage

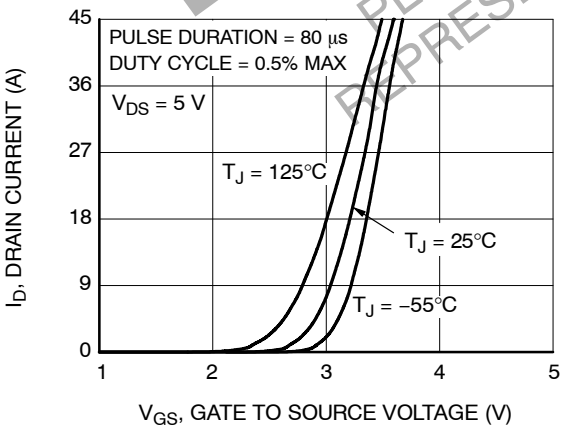

Figure 5. Transfer Characteristics

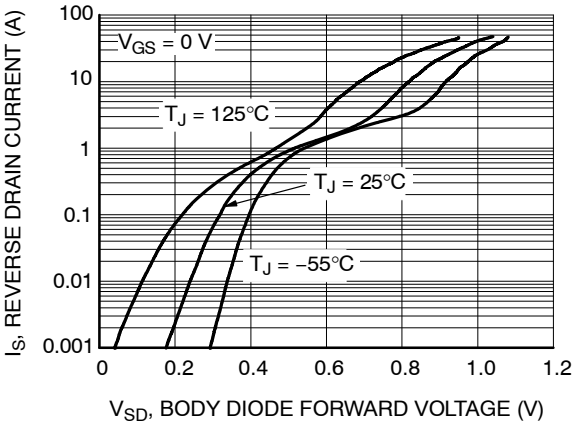

Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

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TYPICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted) (continued)

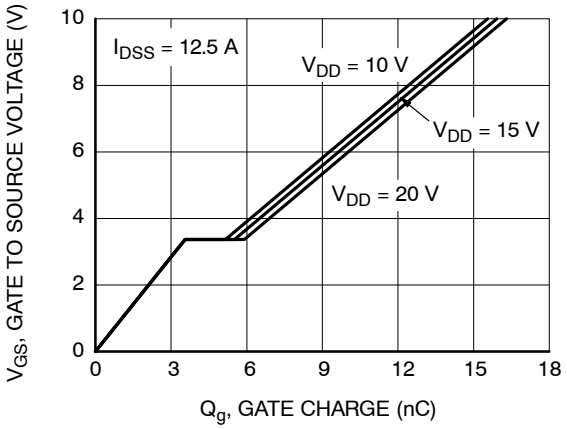

Figure 7. Gate Charge Characteristics

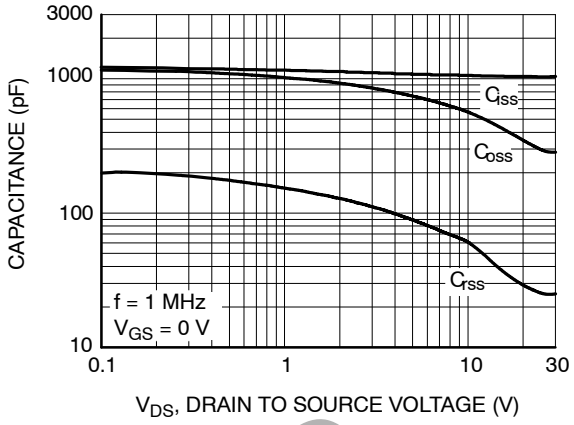

Figure 8. Capacitance vs. Drain to Source Voltage

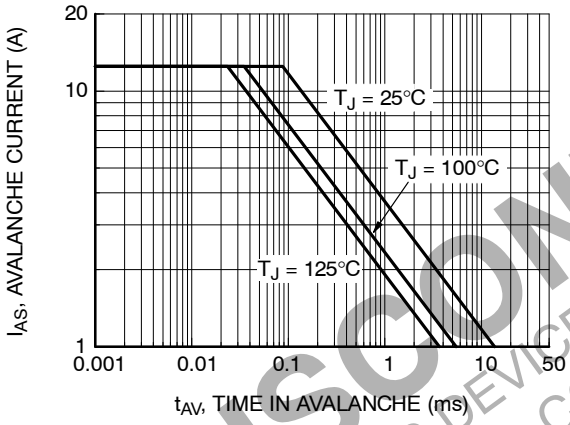

Figure 9. Unclamped Inductive Switching Capability

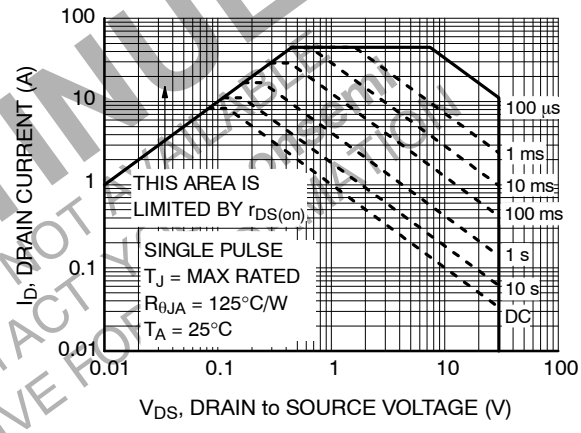

Figure 10. Forward Bias Safe Operating Area

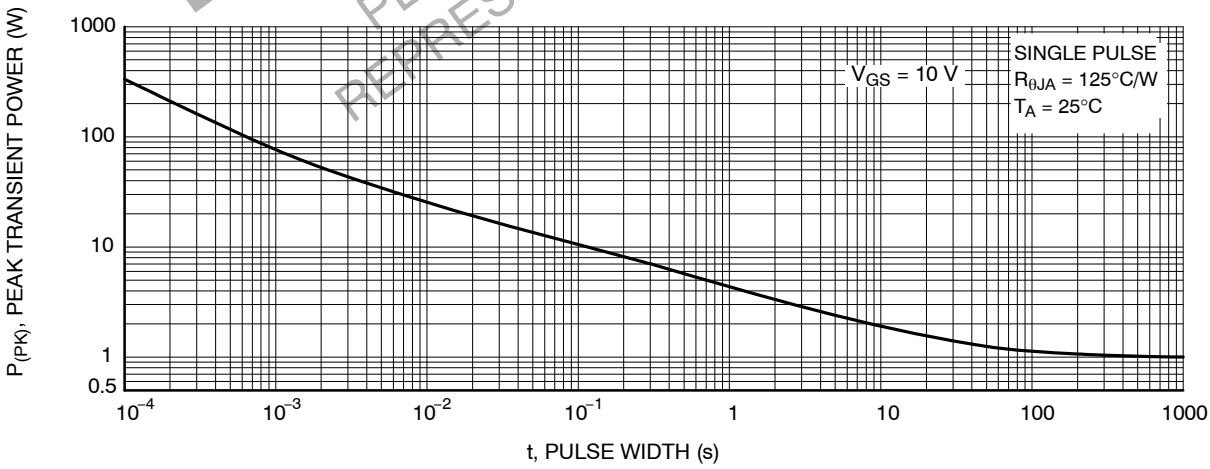

Figure 11. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted) (continued)

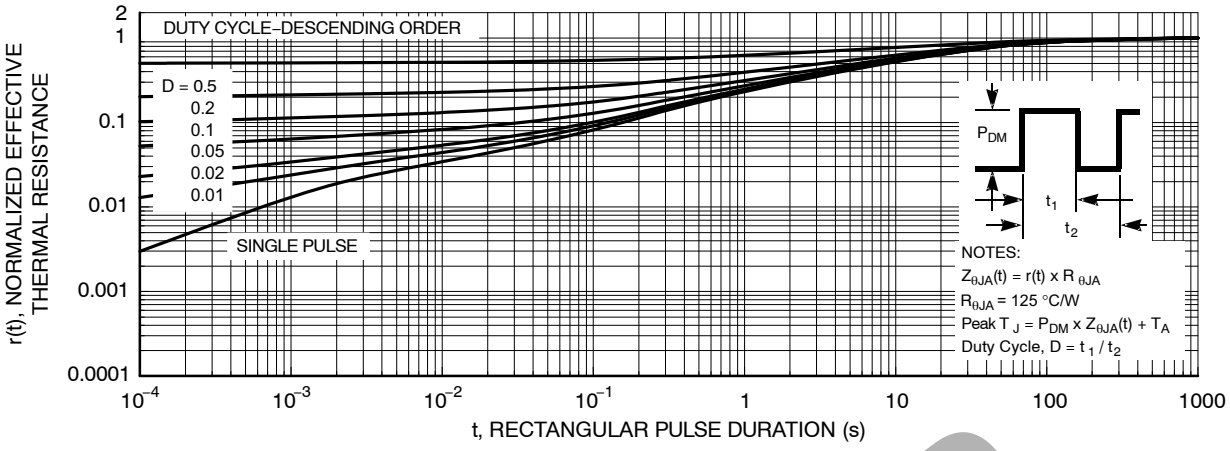

Figure 12. Junction-to-Ambient Transient Thermal Response Curve

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ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping†
FDMC7692S	FDMC7692S	WDFN8 3.3x3.3, 0.65P case 511DQ (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

REVISION HISTORY

Revision	Description of Changes	Date
3	Data Sheet Discontinued.	11/10/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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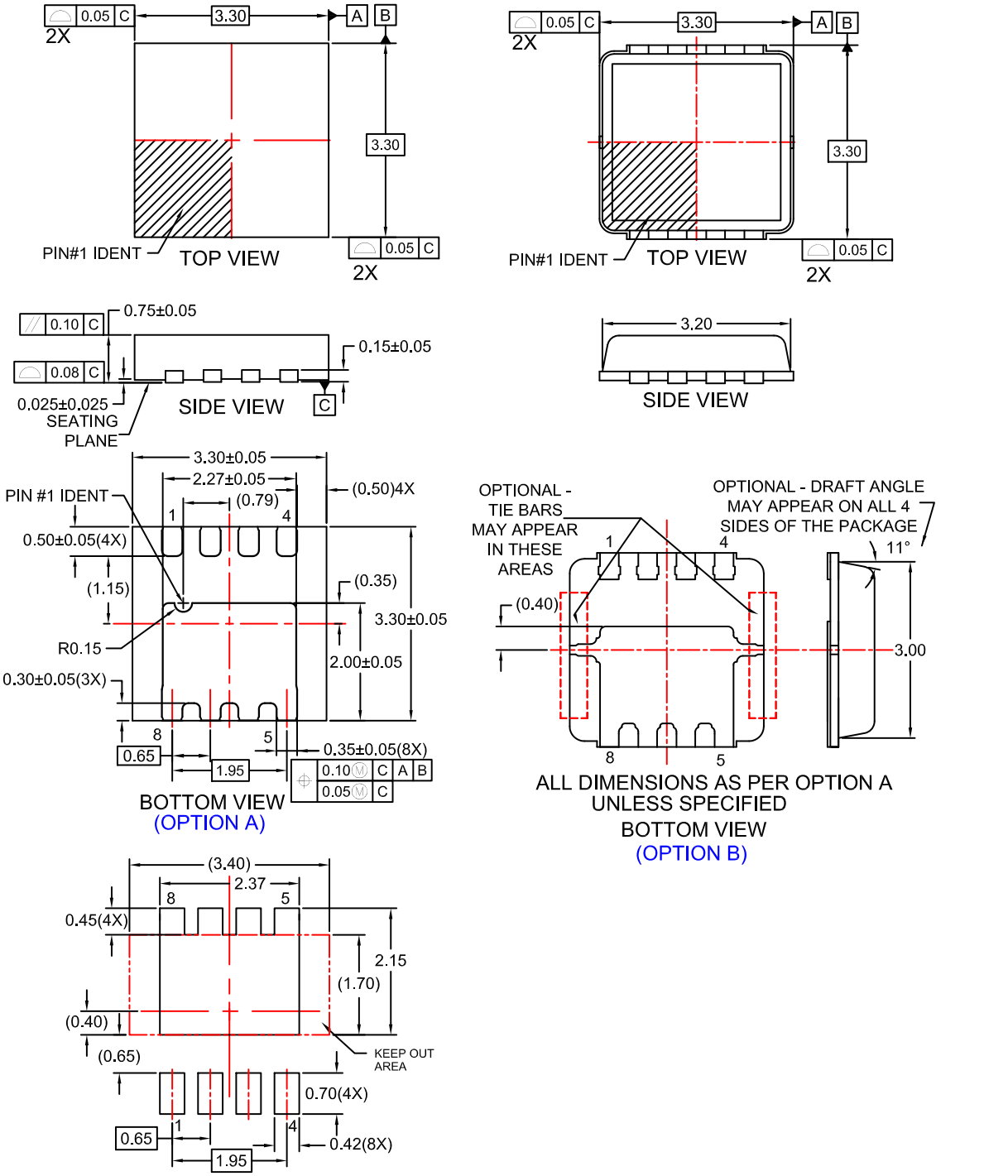
WDFN8 3.3x3.3, 0.65P
CASE 511DQ
ISSUE O

DATE 31 OCT 2016



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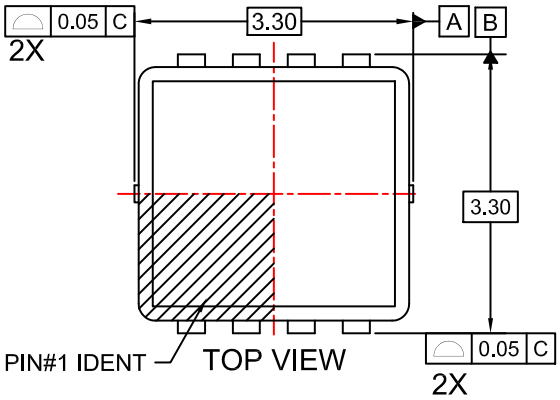
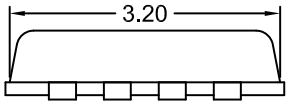
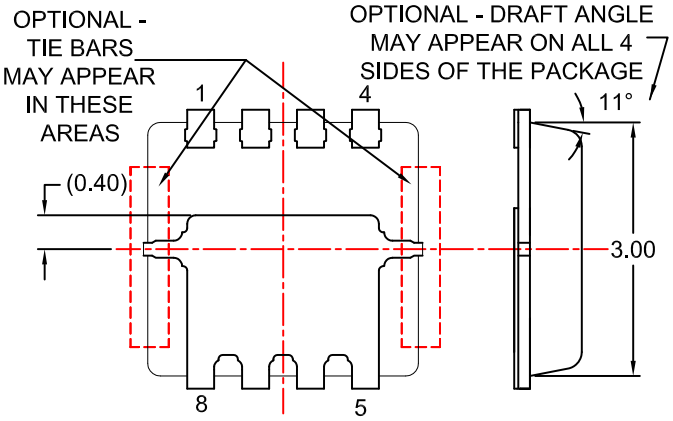
CASE 511DQ
ISSUE O

DATE 31 OCT 2016





SIDE VIEW



ALL DIMENSIONS AS PER OPTION A
UNLESS SPECIFIED

BOTTOM VIEW
(OPTION C)

NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.

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