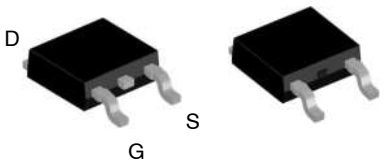
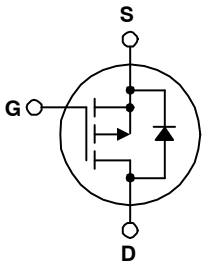
MOSFET – P-Channel, QFET
-400 V, -1.56 A, 6.5 Ω

FQD2P40



DPAK3
CASE 369AS



Description

This P−Channel enhancement mode power MOSFET is produced using **onsemi**'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on−state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

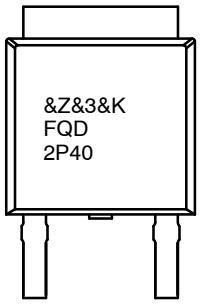
- −1.56 A, −400 V, $R_{DS(on)}$ = 6.5 Ω (Max.) @ V_{GS} = −10 V, I_D = −0.78 A
- Low Gate Charge (Typ. 10 nC)
- Low Crss (Typ. 6.5 pF)
- 100% Avalanche Tested
- RoHS Compliant

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain−Source Voltage	−400	V
I_D	Drain Current – Continuous (T_C = 25°C) – Continuous (T_C = 100°C)	 −1.56 −0.98	A
I_{DM}	Drain Current – Pulsed (Note 1)	−6.24	A
V_{GSS}	Gate−Source Voltage	±30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	120	mJ
I_{AR}	Avalanche Current (Note1)	−1.56	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	3.8	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	−4.5	V/ns
P_D	Power Dissipation (T_A = 25°C)*	2.5	W
	Power Dissipation (T_C = 25°C) – Derate above 25°C	38 0.3	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	−55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM



&Z = Assembly Code
&3 = Date Code (Year and Week)
&K = Lot Code
FQD2P40 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FQD2P40TM	DPAK3 (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.29	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2−oz Copper), Max.	110	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (*1 in2 Pad of 2−oz Copper), Max.	50	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = −250 μA	−400	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C	–	–	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −400 V, V_{GS} = 0 V	–	–	−1	μA
		V_{DS} = −320 V, T_C = 125°C	–	–	−10	μA
I_{GSSF}	Gate−Body Leakage Current, Forward	V_{GS} = −30 V, V_{DS} = 0 V	–	–	−100	nA
I_{GSSR}	Gate−Body Leakage Current, Reverse	V_{GS} = 30 V, V_{DS} = 0 V	–	–	100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = −250 μA	−3.0	–	−5.0	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = −10 V, I_D = −0.78 A	–	5.0	6.5	Ω
g_{FS}	Forward Transconductance	V_{DS} = −50 V, I_D = −0.78 A	–	1.26	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −25 V, V_{GS} = 0 V, f = 1.0 MHz	–	270	350	pF
C_{oss}	Output Capacitance		–	45	60	pF
C_{rss}	Reverse Transfer Capacitance		–	6.5	8.5	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −200 V, I_D = −2.0 A, R_G = 25 Ω (Note 4)	–	9	30	ns
t_r	Turn−On Rise Time		–	33	75	ns
$t_{d(off)}$	Turn−Off Delay Time		–	22	55	ns
t_f	Turn−Off Fall Time		–	25	60	ns
Q_g	Total Gate Charge	V_{DS} = −320 V, I_D = −2.0 A, V_{GS} = −10 V (Note 4)	–	10	13	nC
Q_{gs}	Gate−Source Charge		–	2.1	–	nC
Q_{gd}	Gate−Drain Charge		–	5.5	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	−1.56	A
I_{SM}	Maximum Pulsed Drain−Source Diode Forward Current		–	–	−6.24	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = −1.56 A	–	–	−5.0	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = −2.0 A, dI_F / dt = 100 A/ μs	–	250	–	ns
Q_{rr}	Reverse Recovery Charge		–	0.85	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:
1. Repetitive Rating: Pulse−width limited by maximum junction temperature.
2. L = 86 mH, I_{AS} = −1.56 A, V_{DD} = −50 V, R_G = 25 Ω, Starting T_J = 25°C.
3. I_{SD} ≤ −2.0 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C.
4. Essentially independent of operating temperature.

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TYPICAL CHARACTERISTICS

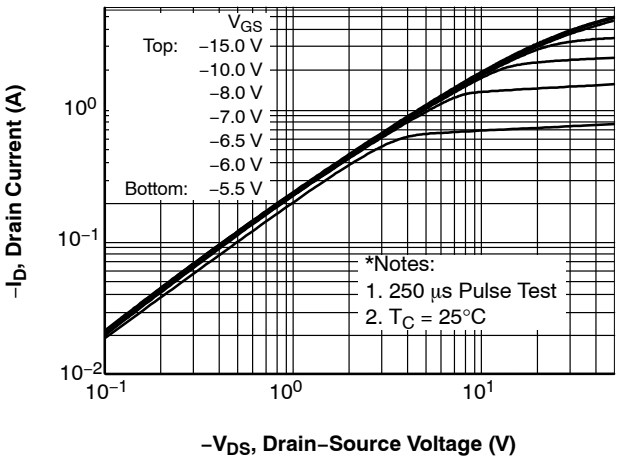


Figure 1. On−Region Characteristics

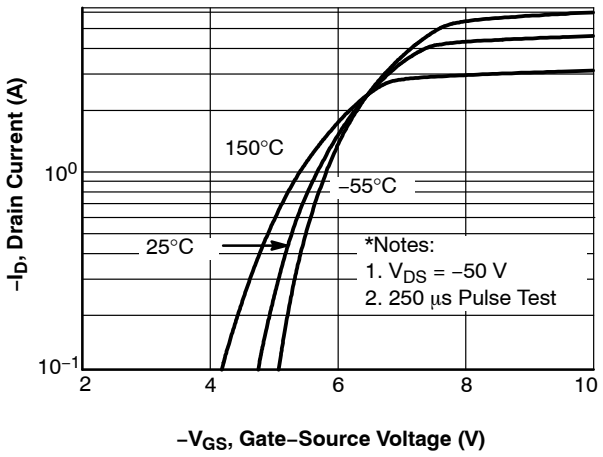


Figure 2. Transfer Characteristics

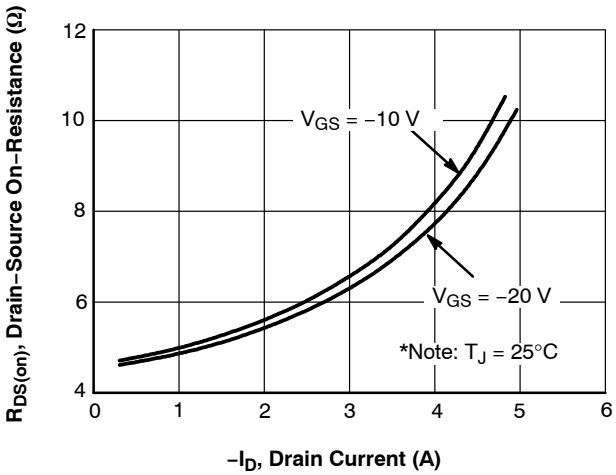


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

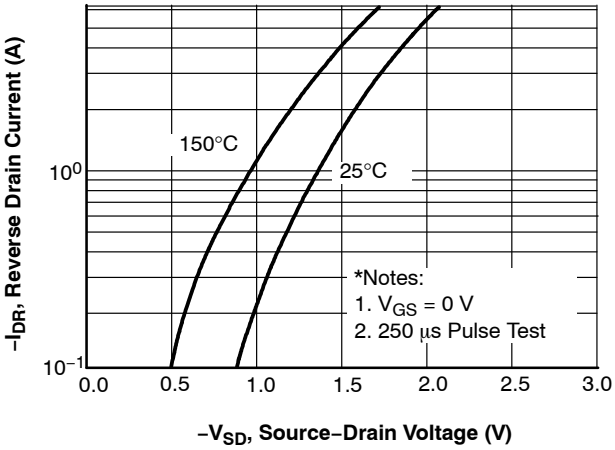


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

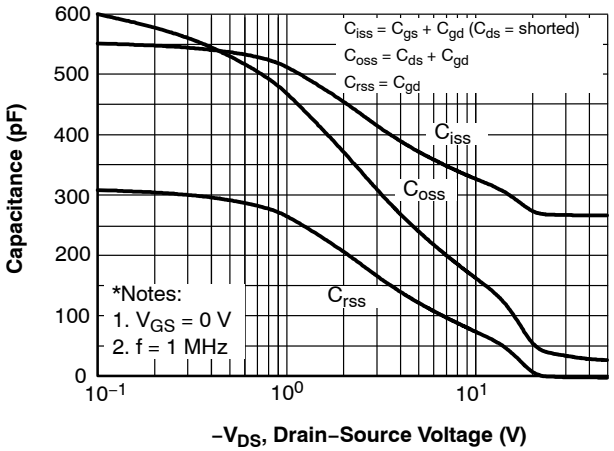


Figure 5. Capacitance Characteristics

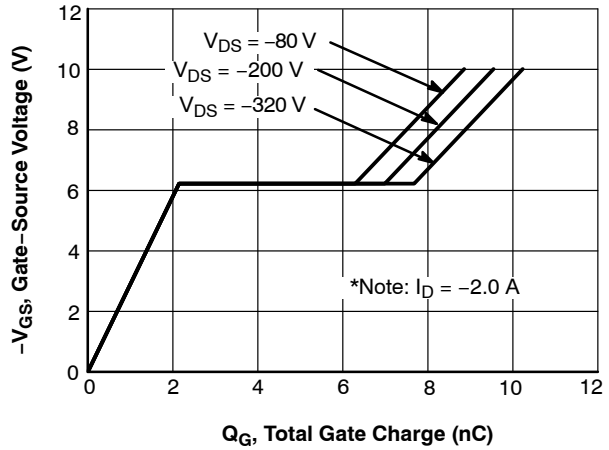


Figure 6. Gate Charge Characteristics

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TYPICAL CHARACTERISTICS (continued)

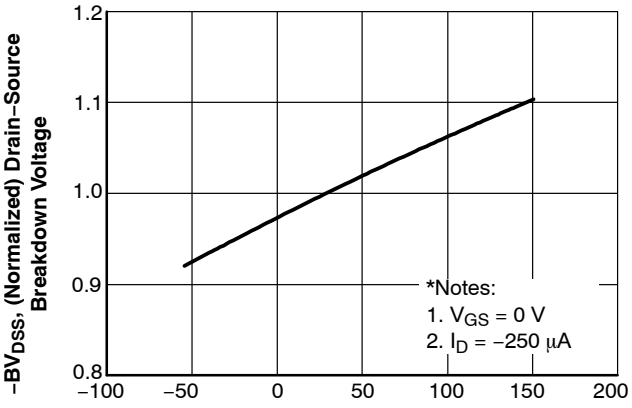


Figure 7. Breakdown Voltage Variation vs. Temperature

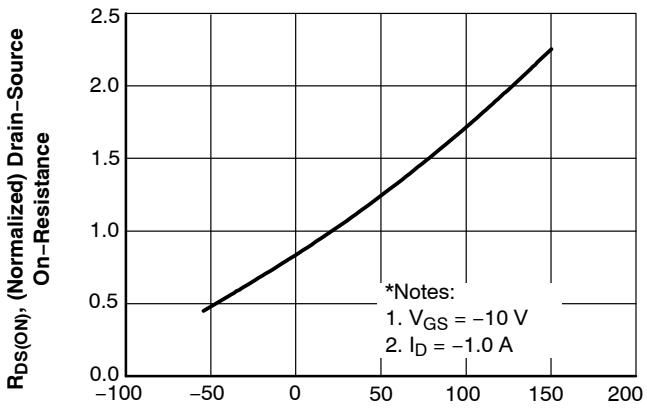


Figure 8. On−Resistance Variation vs. Temperature

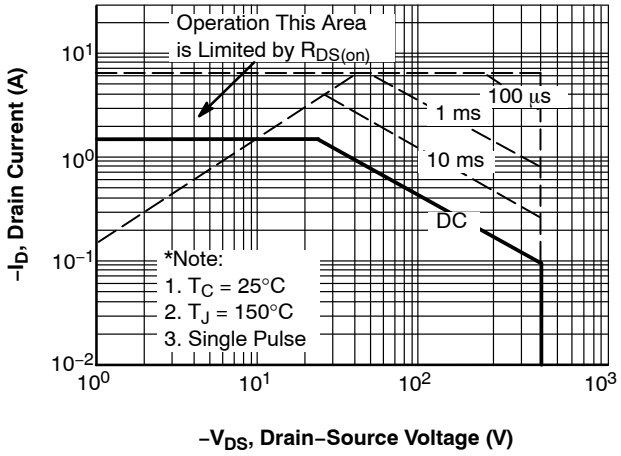


Figure 9. Maximum Safe Operating Area

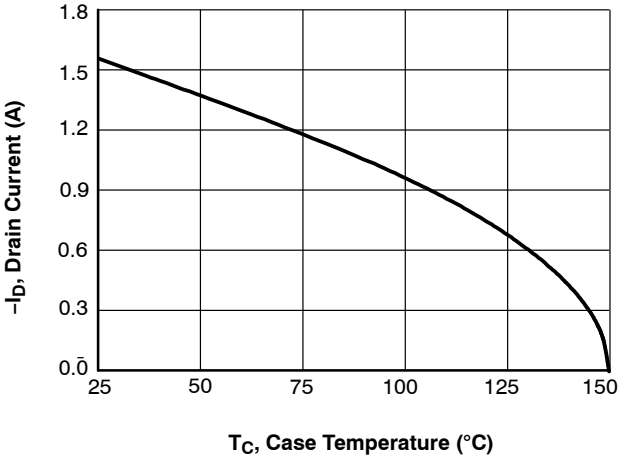


Figure 10. Maximum Drain Current vs. Case Temperature

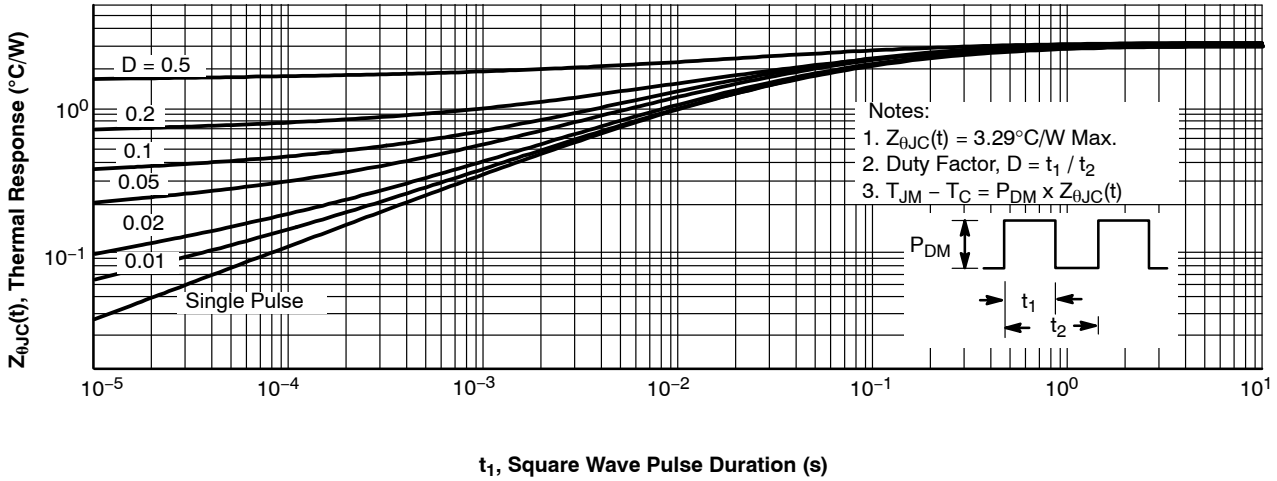


Figure 11. Transient Thermal Response Curve

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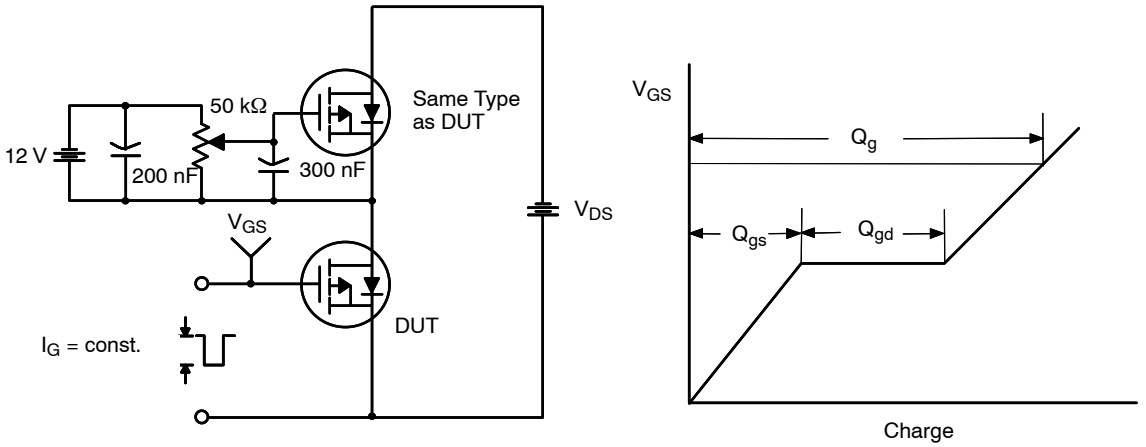


Figure 12. Gate Charge Test Circuit & Waveform

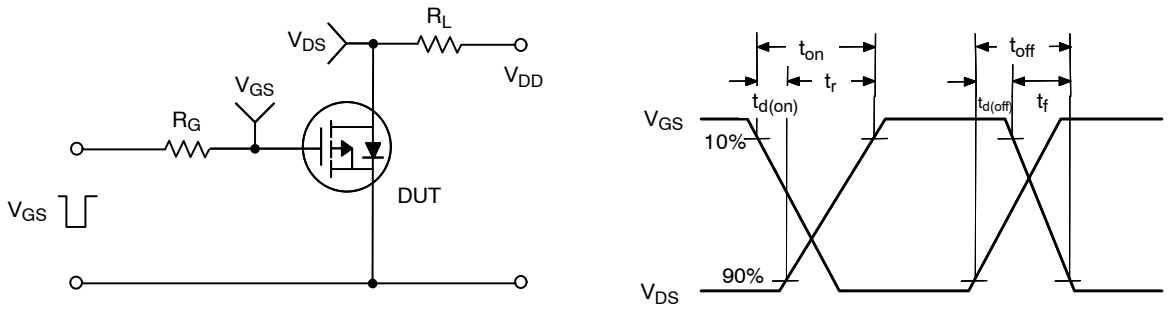


Figure 13. Resistive Switching Test Circuit & Waveforms

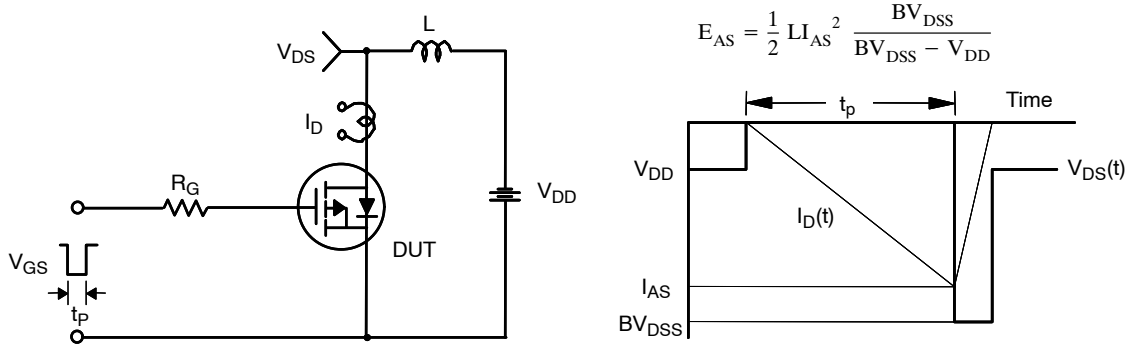


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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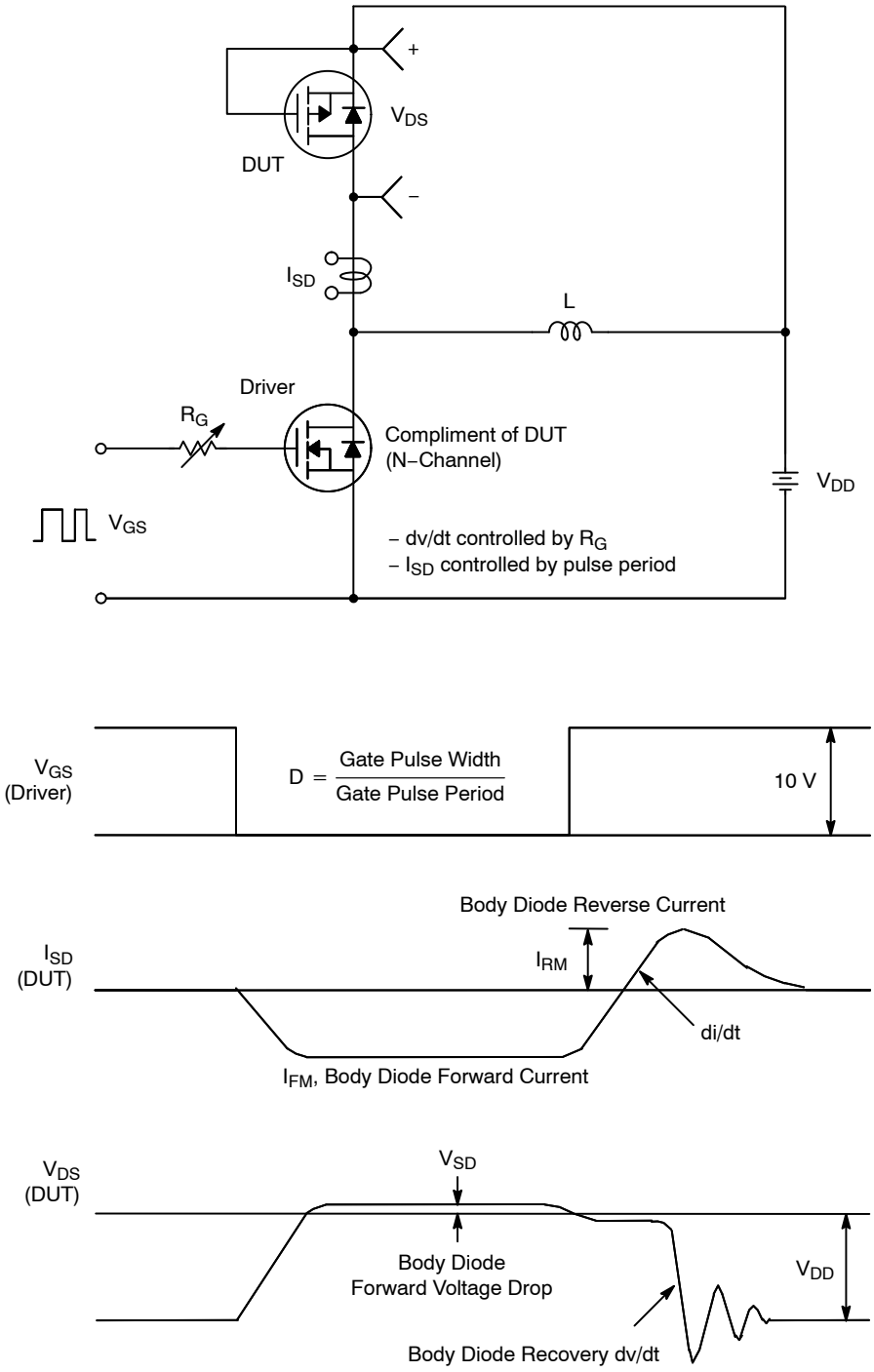
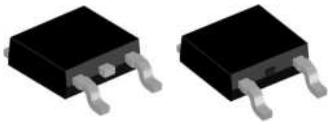


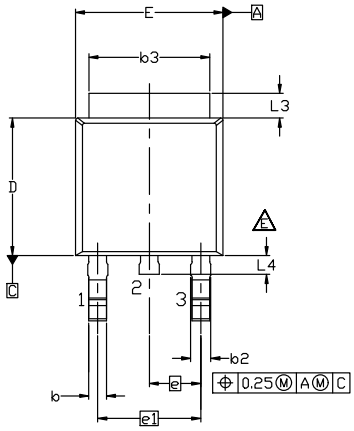
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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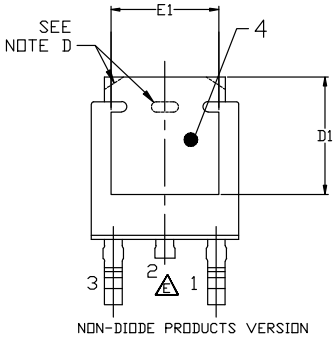


DPAK3 6.10x6.54x2.29, 4.57P
CASE 369AS
ISSUE B

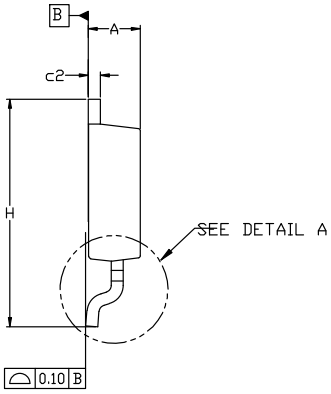
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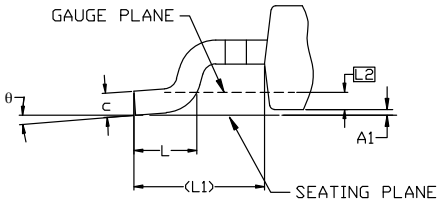
NON-DIODE PRODUCTS VERSION



NON-DIODE PRODUCTS VERSION

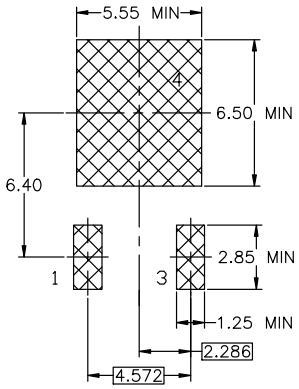


NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE F, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY STUB WITHOUT CENTER LEAD.
F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



DETAIL A
(ROTATED -90°)
SCALE: 12X

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	–	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	---	---
E	6.35	6.54	6.73
E1	4.32	---	---
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	---	---	1.02
θ	0°	---	10°



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

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DESCRIPTION:	**DPAK3 6.10x6.54x2.29, 4.57P**	**PAGE 1 OF 1**

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