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FSA831A — USB2.0 High-Speed (480Mbps) Charger Detection with Isolation Switch

Features

USB Detection	USB Battery Charging Rev. 1.2 Supports Data Contact Detect (DCD) Dead Battery Provision (DBP) with 30-Minute Timer
Switch Type	Isolation Switch Closes for Charging Downstream Port (CDP) Standard Downstream Port (SDP)
V_{BUS}	28 V Over-Voltage Tolerance -2 V Under-Voltage Tolerance
Package	10-Lead MicroPak™ 1.6 x 2.1 mm, 0.5 mm Pitch
Ordering Information	FSA831AL10X

Applications

- MP3, Mobile Internet Device (MID), Cell Phone, PDA, Digital Camera, Notebook and Netbook

Description

The FSA831A is a charger-detection IC with an integrated isolation switch for use with a micro/mini USB port. The FSA831A detects battery chargers and is compliant with USB Battery Charging Specification, Rev 1.2 (BC1.2). The algorithm incorporates Data Contact Detection (DCD), which ensures that the shorter, inner pins of the USB connector are making contact prior to continuing with battery charger detection. The device determines if a Dedicated Charging Port (DCP), Charging Downstream Port (CDP), or a typical PC host, called a Standard Downstream Port (SDP), is connected. If a charger is detected, the FSA831A determines whether the charger is a DCP or CDP. For SDP and CDP detection, an internal isolation switch is closed to connect the D+/D- lines of the USB cable to the resident USB transceiver within the portable device. The FSA831A conforms to all the constraints for the Dead Battery Provision (DBP) within the BC1.2 specification, including a 30-minute timer that cannot exceed 45 minutes, per BC1.2.

Typical Application

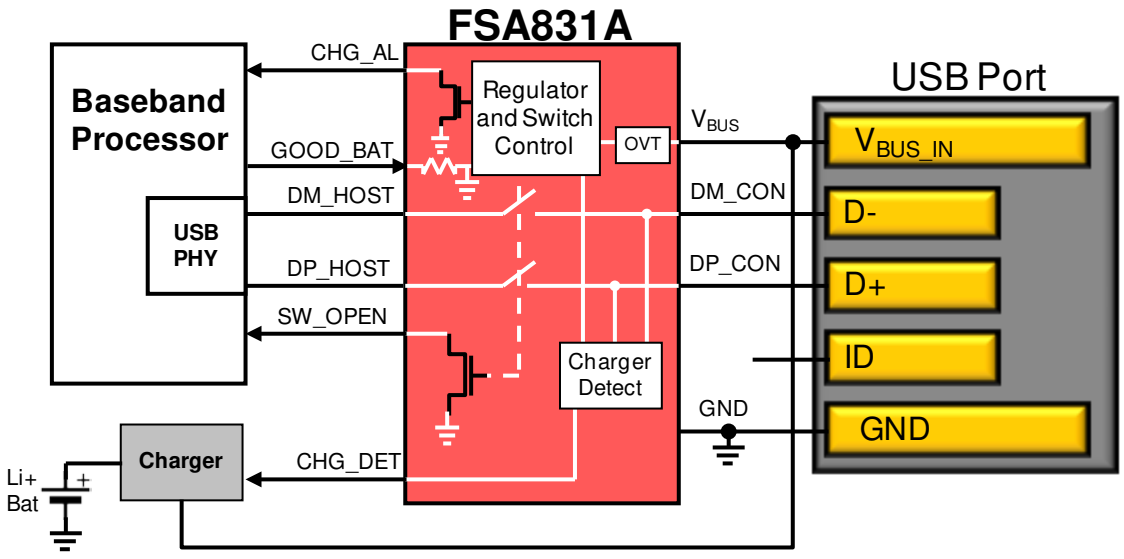


Figure 1. Mobile Phone Example

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December-2017, Rev 2.

Publication Order Number:
FSA831A/D

Pin Configurations

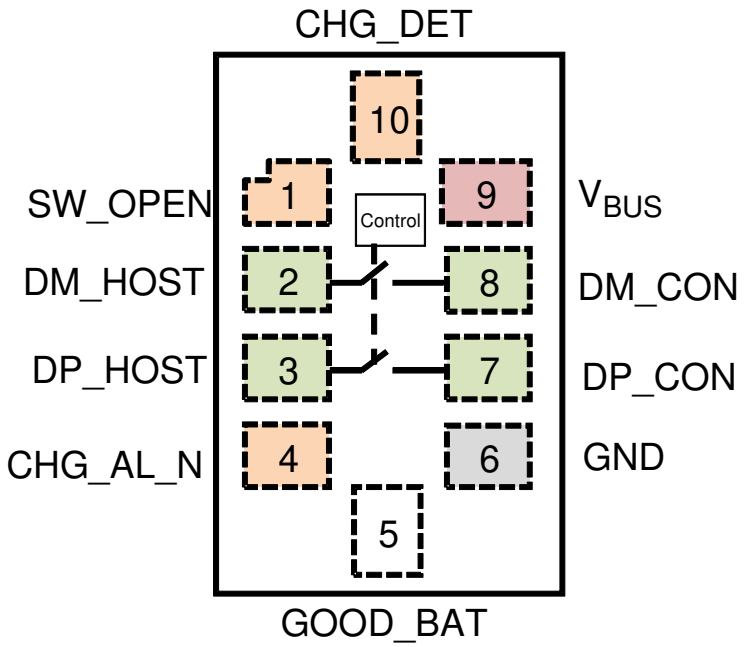


Figure 2. Pin Assignments (Top View)

Pin Descriptions

Name	Pin #	Description
USB Interface		
DP_HOST	3	D+ signal connected to the resident USB transceiver on the phone
DM_HOST	2	D- signal connected to the resident USB transceiver on the phone
Connector Interface		
V_{BUS}	9	Input voltage supply pin to be connected to the V_{BUS} pin of the USB connector
GND	6	Ground
DP_CON	7	Connected to the USB connector D+ pin
DM_CON	8	Connected to the USB connector D- pin
Status Outputs		
CHG_DET	10	CMOS push/pull output connected to charger IC for indicating if a charger has been detected (LOW=charger not detected, HIGH=DCP or CDP charger has been detected).
SW_OPEN	1	Open-drain output pin; requires pull-up resistor to I/O voltage supply (LOW=switch closed, Hi-Z=switch open).
CHG_AL_N	4	CMOS open-drain output pin (LOW=V_{BUS} is valid and charge is allowed to be drawn from V_{BUS}, Hi-Z=V_{BUS} is not at a valid voltage).
Input Pin		
GOOD_BAT	5	Input that indicates if the battery is a good battery or a dead battery (LOW=dead battery, HIGH=good battery).

Table 1. Functionality

Device Detected	GOOD_BAT	SW_OPEN	CHG_AL_N	CHG_DET	DP_HOST	DM_HOST	DP_CON	DM_CON
DCP	X	Hi-Z	LOW	HIGH	Hi-Z	Hi-Z	V_{DP_SRC}	Hi-Z(1)
CDP	HIGH	LOW	LOW	HIGH	DP_CON	DM_CON	DP_HOST	DM_HOST
CDP	LOW	Hi-Z	LOW	HIGH	Hi-Z	Hi-Z	V_{DP_SRC}	Hi-Z
SDP(2)	HIGH	LOW	LOW	LOW	DP_CON	DM_CON	DP_HOST	DM_HOST
SDP(2)	LOW	Hi-Z	LOW	LOW	Hi-Z	Hi-Z	V_{DP_SRC}	Hi-Z
SDP, CDP, or DCP plugged in and after 30-minute timer expires	LOW	Hi-Z	Hi-Z	LOW	Hi-Z	Hi-Z	Hi-Z	Hi-Z
V_{BUS} < V_{BUS} valid to V_{BUS} > V_{BUS} valid operation prior to completing detection of SDP, CDP, or DCP. Upon detection, all outputs switch as in rows above.	X	Hi-Z	Hi-Z	Hi-Z to LOW	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Notes:

1. Hi-Z is the internal state of DM_CON. Since a DCP has been detected, DM_CON is shorted to DP_CON externally and DM_CON is shorted to V_{DP_SRC}.
2. Proprietary chargers that leave DP_CON and DM_CON floating are detected as SDP. Proprietary chargers that force DP_CON=2V and DM_CON=2.7 V (or any other voltages) can be detected as CDP, DCP or SDP depending on the resistances of the resistor dividers on DP_CON and DM_CON used to create the voltages on those pins.

Functional Description

Data Contact Detect (DCD)

DCD relies on the D+ and D- lines being present. DCD waits until the internal timeout ($t_{DCD_TIMEOUT}$) has expired in the following cases:

- If a charger does not have a D+ pin on the USB connector
- If the D+ pin is not shorted to D- pin on the connector
- If D+ is pulled up to a supply
- If D+ does not have a sufficient path to ground to defeat a pull-up I_{DP_SRC} (10 µA typical) current source.

The FSA831A proceeds with charger detection even though it is unlikely a charger is present. If there is no charger, the algorithm reports an SDP and closes the switch. If a device is pulling D+ HIGH, this voltage presents itself to the USB transceiver or Physical Layer Interface (PHY) block within a System on Chip (SoC) after the switch is closed.

If the DCD timeout was insufficient and the PHY block is so equipped, DCD and the charging algorithm can be repeated in the PHY block. The stipulation is that the total time from V_{BUS} valid to USB transceiver connection with a 1.5 kΩ pull-up to 3.3 V must be one (1) second, per USB 2.0 standards (USB 2.0 connect timing), provided the portable device does not have a dead battery.

A typical PS/2 port (old PC mouse / keyboard port) has a resistive pull-up to V_{BUS}. This can cause the DCD to exceed the maximum wait time ($t_{DCD_TIMEOUT}$) and proceed to charger detection. The likely path through charger detection is classifying the PS/2 port as an SDP port. This results in closing the USB switches, which causes the voltage on the DP_CON and DM_CON pins to pass through the switch to DP_HOST and DM_HOST, respectively. Since voltages on the PS/2 port can go as high as the V_{BUS} voltage, the DP_HOST and DM_HOST pins can be pulled up to V_{BUS}. The USB PHY connected to DP_HOST and DM_HOST must be equipped to handle these higher voltages.

CHG_AL_N Output and Output Timing

CHG_AL_N output indicates that charge is allowed to be drawn from V_{BUS} when CHG_AL_N is LOW. When FSA831A first powers up and prior to detection, the CHG_AL_N pin can follow V_{BUS} up to 28 V, which is the absolute maximum V_{BUS} voltage allowed. Whenever V_{BUS} is at GND, the FSA831A is completely off and the switches and all I/Os are in the Hi-Z state. When V_{BUS} climbs above the valid V_{BUS} threshold, detection occurs automatically and CHG_DET, SW_OPEN, and CHG_AL_N all simultaneously switch to the states indicated in Table 1 if GOOD_BAT is HIGH *(see Dead Battery Provision description for GOOD_BAT = LOW).*

Dead Battery Provision (DBP)

BC1.2 and USB 2.0 allow a portable device (defined as a device with a battery) with a dead battery to take a maximum of 100 mA from the USB V_{BUS} line for a maximum of 45 minutes as long as the portable device forces the D+ line to V_{DP_SRC} (0.6 V typical). FSA831A starts detection when V_{BUS} crosses the V_{BUSVLD} threshold and, if it detects a CDP or SDP and GOOD_BAT is HIGH, automatically closes the switch and does not force the DP_CON pin to V_{DP_SRC}.

Once the charger detection is completed, the FSA831A starts a 30-minute timer and forces the DP_CON pin to V_{DP_SRC} until the timer elapses. During the 30 minute period, if GOOD_BAT is LOW, V_{DP_SRC} is applied to DP_CON and the D+/D- switches are opened, If GOOD_BAT is HIGH, V_{DP_SRC} is not applied to DP_CON and the D+/D- switches are closed, If GOOD_BAT is LOW when 30 minute timer expires; regardless of whether an SDP, CDP, or DCP was previously detected; the FSA831A removes V_{DP_SRC} from DP_CON and forces CHG_DET LOW and CHG_AL_N to Hi-Z (SW_OPEN remains Hi-Z) To exit this fault condition, remove V_{BUS}, wait for all the V_{BUS} Printed Circuit Board (PCB) capacitance to discharge, and re-apply V_{BUS}. Table 1 provides the functionality of the pins when the timer expires.

When GOOD_BAT is HIGH and the battery is removed from the portable device while V_{BUS} is valid, bringing GOOD_BAT LOW; the FSA831A opens the isolation switches on DP_CON and DM_CON and forces the DP_CON pin to V_{DP_SRC}. In this scenario, the timer generally expires because the SoC does not have a supply to bring GOOD_BAT HIGH unless the battery that was removed is re-inserted within 30 minutes from when the USB plug is inserted.

If an SDP or CDP is inserted with GOOD_BAT HIGH during the 30-minute timer, then GOOD_BAT changes to LOW; SW_OPEN changes to Hi-Z and the counter continues counting until the 30 minutes expires. If GOOD_BAT then returns to HIGH, SW_OPEN changes to LOW and finishes out the 30-minute time.

GOOD_BAT has an internal pull-down resistor to ensure it is LOW when the SoC is powered down. This input is designed to have very low thresholds to interface with low-voltage SoCs driven with 1.2 V supplies.

Proprietary Chargers

Only legitimate USB chargers that force V_{DM_SRC} (0.6V typical) on DM_CON when V_{DP_SRC} is applied to DP_CON are detected by the FSA831A and cause CHG_DET signal to be asserted. Any charger that forces a HIGH on both DP_CON and DM_CON can be detected as CDP, DCP, or SDP (depending on the resistances of the resistor dividers on DP_CON and DM_CON) and used to create the HIGH voltages on those pins. Any charger that lets both DP_CON and DM_CON signals float is detected as an SDP and CHG_DET stays de-asserted. In cases where the proprietary charger is detected as an SDP or CDP, since the switches are closed and access is made from the USB connector D+ and D- lines to the USB PHY block; the chargers can be detected within the PHY if so equipped

Ground Drops

When a DCP is detected, V_{DP_SRC} is forced on DP_CON provided GOOD_BAT is HIGH or if GOOD_BAT is LOW and the DBP timer has not expired. For current up to 1.5 A flowing into the V_{BUS} and GND lines of the USB cable, this can translate to substantial ground drops that lift the ground of the portable device. This drop adds to the voltage at the DP_CON pin as seen from the DCP D+ pin. For the maximum ground drop of 375 mV specified in the BC1.2 specification and for the maximum V_{DP_SRC} of 0.7 V, the

voltage as seen by the DCP would be 1.075 V. Smart DCPs that rely on this voltage detection to determine attach and detach detection need to take this into account.

V_{BUS} Tolerance

When V_{BUS} rises, an internal Power On Reset (POR) detects this voltage and prepares the FSA831A for charger detection.

V_{BUS} voltages up to 28 V can be tolerated by the V_{BUS} pin. V_{BUS} can tolerate voltages up to -2 V for cases where a charger is plugged in backwards.

Detection Flow

The flow diagram in Figure 3 shows how the FSA831A achieves battery charger detection consistent with BC1.2.

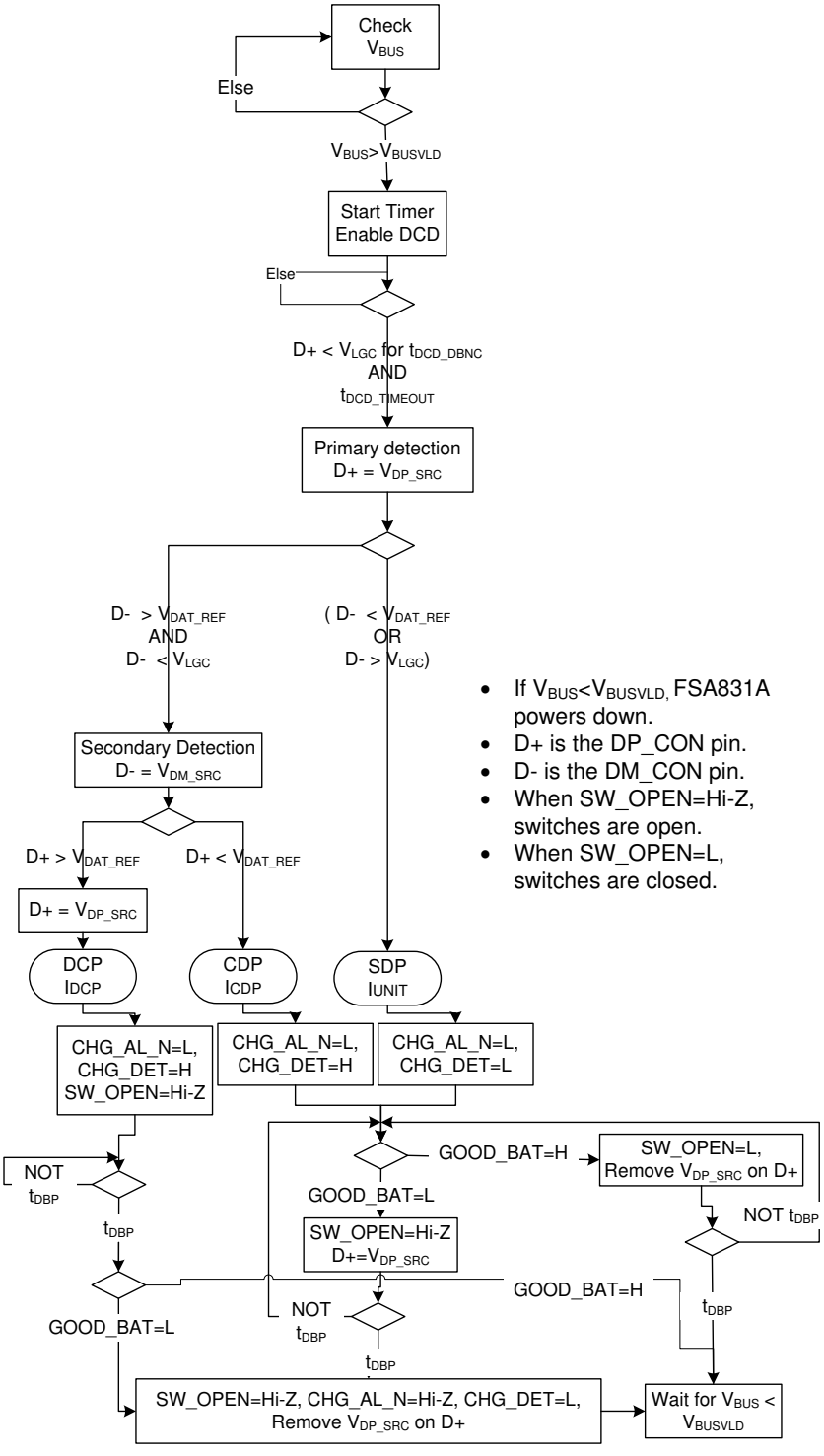


Figure 3. Battery Charger Detection

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter			Min.	Max.	Unit
V_{BUS}	Voltage from USB Connector			-2	28	V
V_{SW}	USB Switch I/O Voltage (DP_CON, DM_CON, DP_HOST, DM_HOST)			-0.5	6.0	V
I_{SW}	USB Switch Current (DP_CON to DP_HOST, DM_CON to DM_HOST)			-30	+30	mA
$V_{I/O}$	Voltage from GOOD_BAT, CHG_AL_N, CHG_DET and SW_OPEN I/Os			-0.5	6.0	V
V_{CA}	Voltage from CHG_AL_N Output			-0.5	28.0	V
$I_{I/O}$	CHG_AL_N, CHG_DET and SW_OPEN Outputs Sink/Source Current			-5	+5	mA
T_{STG}	Storage Temperature Range			-65	+150	°C
T_J	Maximum Junction Temperature				+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)				+260	°C
ESD	IEC 61000-4-2 System	USB Pins (DP_CON, DM_CON, V_{BUS})	Air Gap		15	kV
			Contact		8	
	Human Body Model, JEDEC JESD22-A114		All Pins		6	
	Charged Device Model, JEDEC JESD22-C101		All Pins		1	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. ON Semiconductor does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{BUS}	V_{BUS} Input HIGH Voltage	4	6	V
V_{SW}	Switch I/O Voltage for USB Path	0	3.6	V
T_A	Operating Temperature	-40	+85	ºC

DC Electrical Characteristics

Unless otherwise indicated, V_{BUS}=4 V to 6 V and T_A=-40 to +85°C. Typical values are at T_A=25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Status Outputs						
V_{OHCD}	Output HIGH Voltage (CHG_DET)	I_{OH}=-2 mA	2.0			V
V_{OL}	Output LOW Voltage (CHG_DET, CHG_AL_N, SW_OPEN)	I_{OL}=2 mA			0.4	V
t_{DIFF}	Skew Between Any Output (CHG_DET, CHG_AL_N, SW_OPEN) Switching Relative to the Other Outputs Switching	$I_{I/O}$=±2 mA, CHG_AL_N=20 kΩ to 5 V, SW_OPEN=10 kΩ to 1.8 V			100	ns
V_{BUS} Pin						
V_{BUSVLD}	V_{BUS} Valid Detection Threshold(1)		0.8		4.0	V
I_{BUSIN}	V_{BUS} Input Leakage	V_{BUS}=0 V to 0.8 V			3	µA
$I_{VBUSACT}$	V_{BUS} Active Mode Average Current	USB Path Active, USB Switch Closed After Charger Detection			250	µA
t_{OUT}	Time from V_{BUS} Valid Asserted to CHG_DET, CHG_AL_N and SW_OPEN Outputs Valid	DP_CON pulled down to GND, 15kΩ, all voltages forced on V_{BUS}, DP_CON, DM_CON and GND simultaneously			250	ms
Switch Characteristics						
I_{OFF}	Power Off Leakage Current	USB Path V_{BUS}=0V, V_{SW}=0 V or 3.6 V, Figure 5			10	µA
R_{ONUSB}	High-Speed USB Range Switch On Resistance(1)	V_{DP_CON} / V_{DM_CON}=0V, 0.4 V; I_{ON}=8 mA; Figure 4; V_{BUS}=4 V to 6 V		4.5	6.5	Ω
Control Input						
V_{IH}	Input HIGH Voltage (GOOD_BAT)		1.1			V
V_{IL}	Input LOW Voltage (GOOD_BAT)				0.5	V
R_{PD}	Pull Down Resistance (GOOD_BAT)		1			MΩ
I_{IN}	Input Leakage Current (GOOD_BAT)	V_{BUS}=5 V, GOOD_BAT=0 V to 4.4 V			10	µA
I_{IOFF}	OFF State Leakage Current (GOOD_BAT)	V_{BUS}=0 V, GOOD_BAT=0 V to 4.4 V			10	µA
t_{DBP}	Dead Battery Provision (DBP) Timer		15	30	45	min
t_{GB}	Time from GOOD_BAT Asserted to SW_OPEN De-Asserted, Switches Closed and Meet the R_{ONUSB} Specification				30	ms
t_{DB}	Time from GOOD_BAT De-asserted to SW_OPEN Asserted, Switches Opened				65	ms
Battery Charger Detection Parameters from BC1.2 Specification						
V_{DAT_REF}	Data Detect Voltage		0.25		0.40	V
V_{DM_SRC}	D- Source Voltage(2)		0.5		0.7	V
V_{DP_SRC}	D+ Source Voltage(2)		0.5		0.7	V
V_{LGC}	Logic Threshold		0.8		2.0	V
I_{DM_SINK}	D- Sink Current		25		175	µA
I_{DP_SINK}	D+ Sink Current		25		175	µA
I_{DP_SRC}	Data Contact Detect Current Source		7		13	µA
t_{DCD_DBNC}	Data Contact Detect Debounce		10			ms
t_{DCD_TOUT}	Time for DCD to Timeout		300	450	900	ms
t_{VDPSRC_ON}	D+ Voltage Source On Time		40			ms
t_{VDMSRC_ON}	D- Voltage Source On Time		40			ms

Notes:

1. Guaranteed by characterization; not production tested.
2. The voltage source, V_{DP_SRC} / V_{DM_SRC}, is able to source at least 250 µA when the output voltage is in the specified range. This voltage source should not pull DP_CON / DM_CON below 2.2V when DP_CON / DM_CON is pulled to a voltage of 3.0 V minimum or 3.6 V maximum with a resistance of 900 Ω minimum or 1575 Ω maximum.

AC Electrical Characteristics

Unless otherwise specified, values are at T_A=-40 to +85°C; all typical values are for V_{CC}=3.3 V at T_A=25°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit	Figure
Xtalk	Active Channel Crosstalk, DP_CON to DM_CON[3]	f=1 MHz, R_T=50 Ω, C_L=0 pF		-78		dB	Figure 7
		f=240 MHz, R_T=50 Ω, C_L=0 pF		-36			
O_{IRR}	Off Isolation Rejection Ratio, DM_HOST to DM_CON, DP_HOST to DP_CON[3]	f=1 MHz, R_T=50 Ω, C_L=0 pF		-84		dB	Figure 6
		f=240 MHz, R_T=50 Ω, C_L=0 pF		-34			
BW	Bandwidth of Switch	R_T=50 Ω		1.7		GHz	Figure 7

Note:

3. Guaranteed by characterization; not production tested.

Capacitance

Unless otherwise specified, values are at T_A=-40 to +85°C.

Symbol	Parameter	Condition	Typical	Unit	Figure
C_{OFF}	DP_CON, DM_CON Off Capacitance[4]	V_{BIAS}=0.2V, f=1MHz	3.2	pF	Figure 8
C_{ON}	DP_CON, DM_CON On Capacitance[4]	V_{BIAS}=0.2V, f=1MHz	5.8	pF	Figure 9

Note:

4. Guaranteed by characterization; not production tested.

Test Diagrams

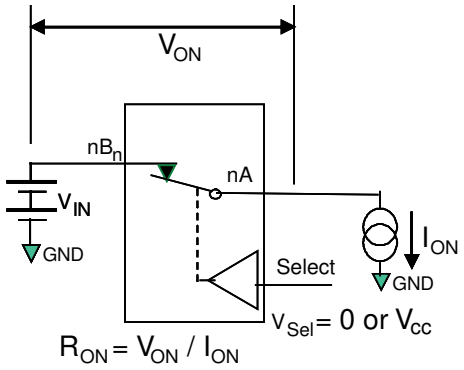
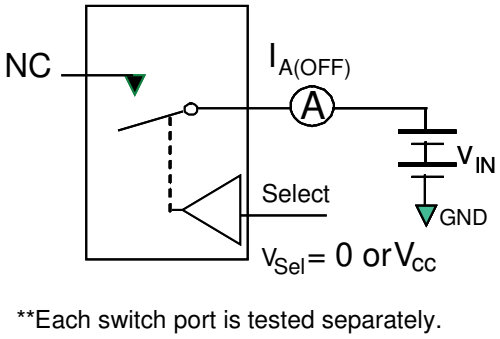


Figure 4. On Resistance



**Each switch port is tested separately.

Figure 5. Off Leakage

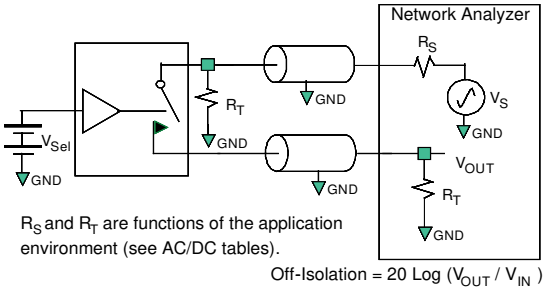


Figure 6. Channel Off Isolation

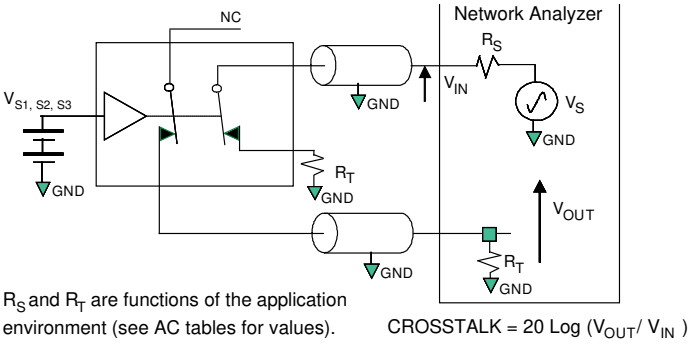


Figure 7. Active Channel Crosstalk

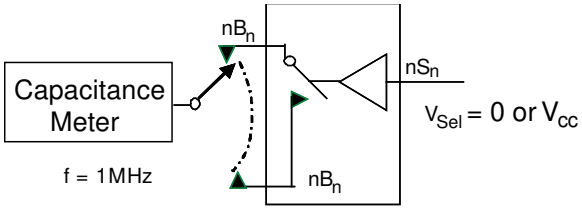


Figure 8. Channel Off Capacitance

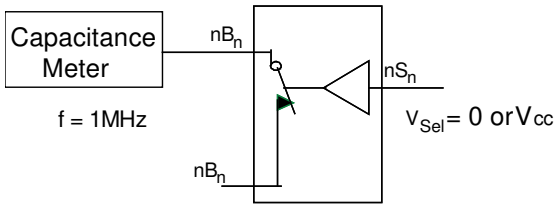
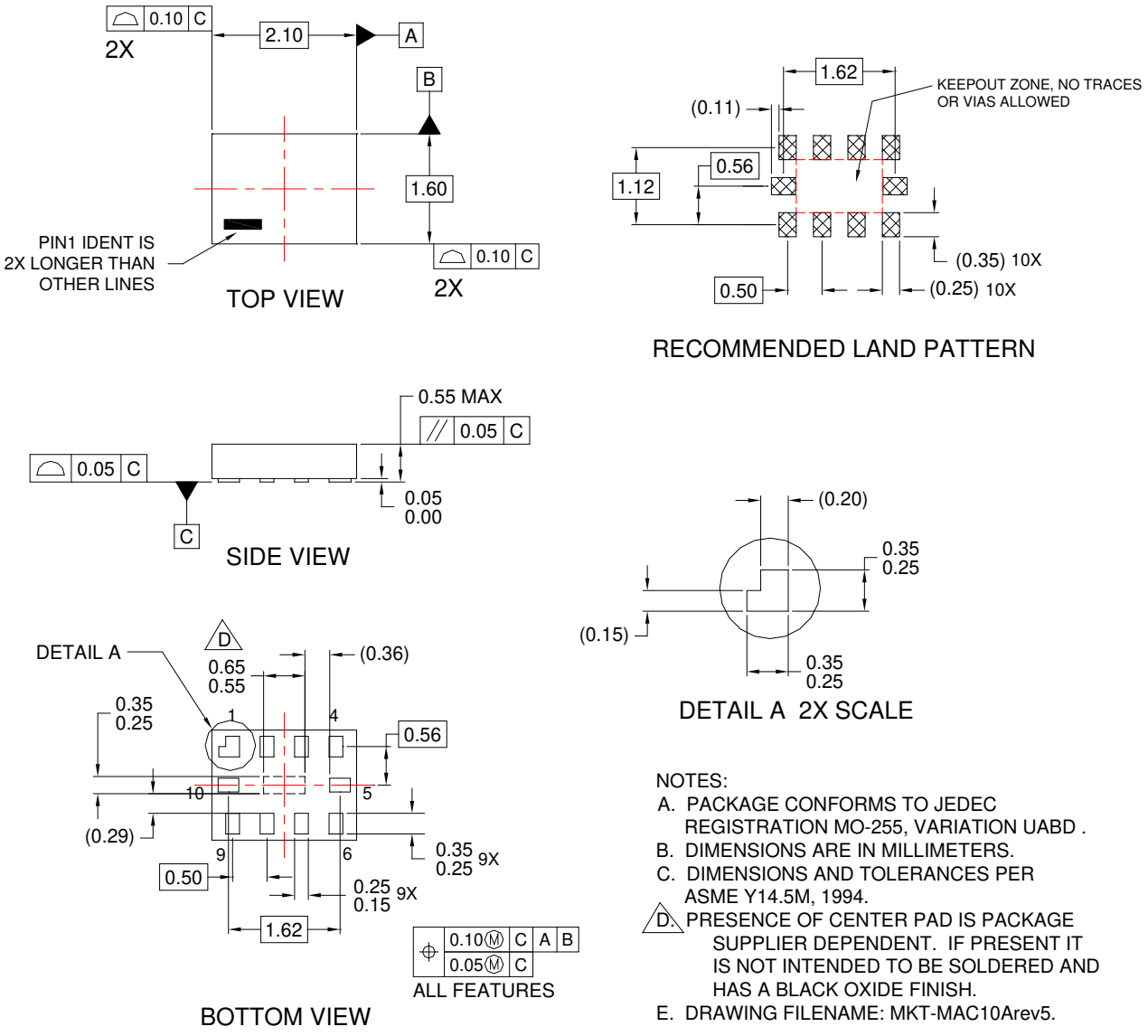


Figure 9. Channel On Capacitance

Physical Dimensions



NOTES:

A. PACKAGE CONFORMS TO JEDEC REGISTRATION MO-255, VARIATION UABD .

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. PRESENCE OF CENTER PAD IS PACKAGE SUPPLIER DEPENDENT. IF PRESENT IT IS NOT INTENDED TO BE SOLDERED AND HAS A BLACK OXIDE FINISH.

E. DRAWING FILENAME: MKT-MAC10Arev5.

Figure 10. 10-Lead, MicroPak™

Part Number	Top Mark	Operating Temperature Range	Package Description	Packing Method
FSA831AL10X	NY	-40 to 85°C	10-Lead, MicroPak™ 1.6 x 2.1 mm, 0.5 mm Pitch	Tape & Reel

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