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September 2013

FUSB2805
USB2.0 High-Speed OTG Transceiver with ULPI Interface

Features

- Complies with USB 2.0, OTG Rev 1.3 Supplement, and ULPI Rev 1.1 Specifications
- Supports 480 Mbps, 12 Mbps, and 1.5 Mbps USB2.0 Speeds
  - Integrated Termination Resistors Meet USB2.0 Resistor ECN
  - Integrated Serializer and Deserializer
  - Insertion and Removal of Stuffed Bits as Appropriate
  - USB Clock and Data Recovery to ±150ppm
- Supports USB OTG Rev 1.3 Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
- 15 kV ESD, IEC 61000 Board Level, Air Gap

Applications

- Set-Top Box Video Camera, MP3 Player
- Cell Phone, Digital Still Camera, PDA
- DVD Recorder, Scanner, Printer

Description

The FUSB2805 is a UTMI+ Low-Pin Interface (ULPI) USB2.0 OTG transceiver. It is compliant with the Universal Serial Bus Specification Rev 2.0 (USB2.0), the ULPI Specification Rev. 1.1, and the On-The-Go (OTG) supplement to USB2.0, Rev. 1.3.

The FUSB2805 is optimized to connect the USB2.0 host, peripheral, or OTG-controller to the USB connector via the ULPI link. Data can be transmitted and received at high speed (480 Mbps), full speed (12 Mbps), and low speed (1.5 Mbps) through a 12-bit (SDR) interface.

Related Resources

UTMI+ Low Pin Interface Specification (ULPI), Revision 1.1, October 20, 2004. http://www.ulpi.org

UTMI+ Specification, Revision 1.0, February 22, 2004. http://www.ulpi.org

For additional performance information, please contact analogswitch@fairchildsemi.com.

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FUSB2805MLX	FUSB2805	-40 to +85°C	32-Terminal, Molded Leadless Package (MLP), Quad, JEDEC MO-220

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Block Diagram

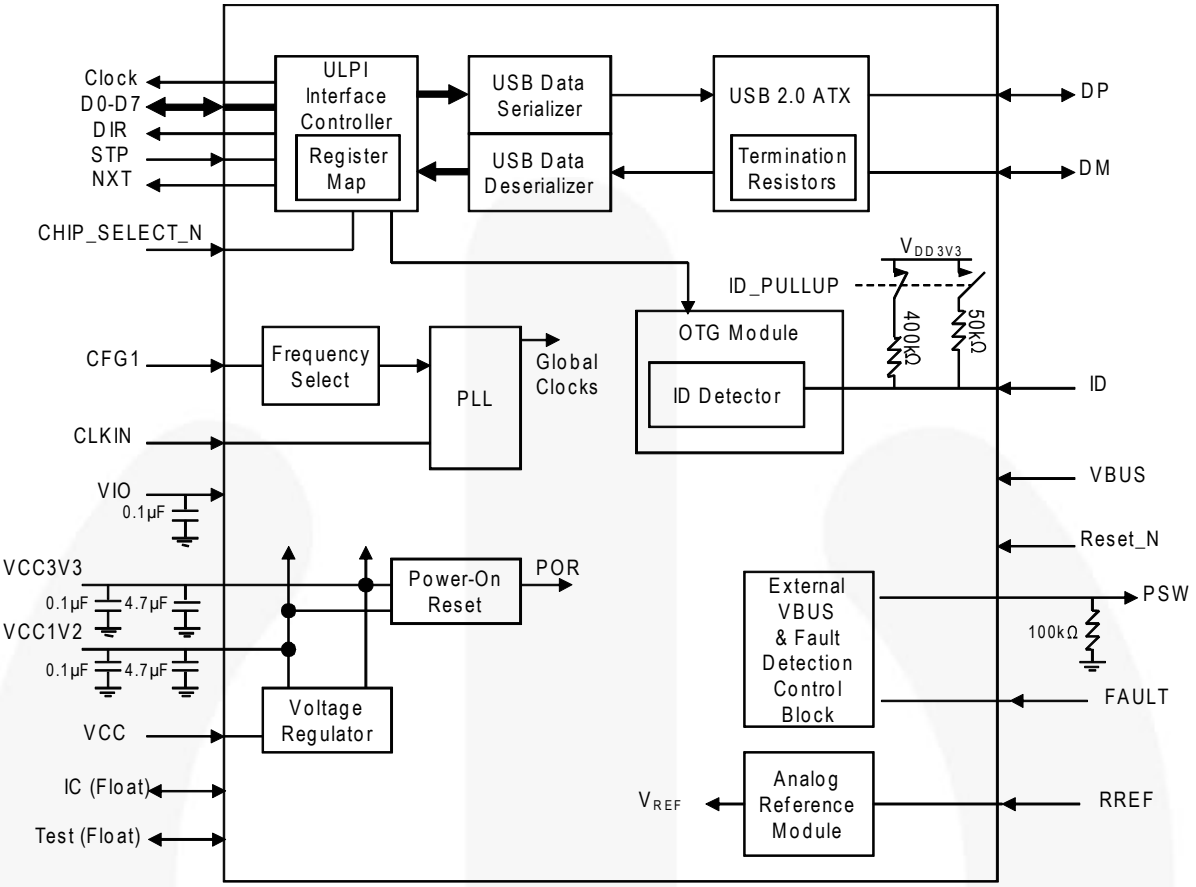


Figure 1. Functional Block Diagram

Pin Configuration

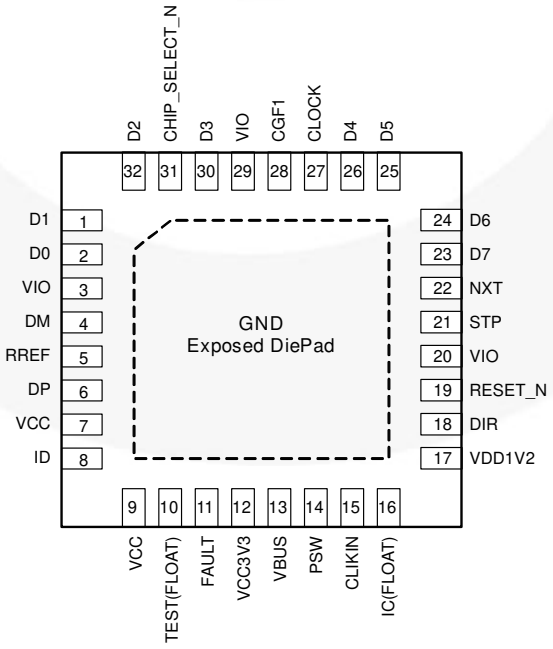


Figure 2. Pin Assignments (Through View)

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Pin Definitions

Symbol	Type[1]	Description
Chip Select_N	I	Active LOW. HIGH – ULPI pin three-stated; LOW – ULPI operates normally. TTL compatible; CMOS input with hysteresis.
R_{REF}	AI/O	Resistor reference. Connect through 12 kΩ ±1% to GND.
DM	AI/O	USB D- pin. USB mode: data minus (D-) pin of the USB cable.
DP	AI/O	USB D+ pin. USB mode: data plus (D+) pin of the USB cable.
FAULT	I	FAULT is used to signal a V_{BUS} over-current/over-voltage condition from an external SMPS or power management IC. The link must enable this function via the ExternalVbusFault register bit and the polarity must be set via the ExternalVbusActiveLow register bit.
ID	I	Identification (ID) pin of the micro-USB cable. TTL; if not used, connect to 3V3.
VCC	P	Input supply voltage or battery source.
PSW	O	Controls an external, active HIGH, V_{BUS} power switch/charge pump and/or an SMPS charger IC. An external 100 kΩ pull-down resistor is required. Open source, slew-rate-controlled output; this pin is referenced to V_{CC3V3}.
V_{BUS}	AI/O	Should be connected to the VBUS pin of the USB cable. Leave open circuit if not used. An internal 90 kΩ ±11% pull-down resistor is present on this pin.
V_{CC3V3}	P	3.3 V regulator output requiring capacitors. Internally powers OTG, analog core, and ATX.
CLKIN	I	Clock input; frequency depends on the CFG1 pin. This is a digital input buffer, not analog for a crystal.
I.C.	I/O	Internally connected; float pin.
TEST	I/O	Internally connected; float pin.
CFG1	I	Configures the clock frequency; 0: input is 19.2 MHz. 1: input is 26 MHz.
V_{DD1V2}	P	1.2 V regulator output requiring capacitors. Internally powers the digital core and analog core.
V_{IO}	P	Input I/O supply rail; 0.1 µF capacitor connected to power input.
Reset_N	I	Connect to V_{IO} when not used. Resets the transceiver; active LOW.
GND	P	Connect to ground.
DIR	O	ULPI direction output signal.
STP	I	ULPI stop input signal; CMOS input.
NXT	O	ULPI next output signal.
D7	I/O	ULPI data pin 7; three-state output.
D6	I/O	ULPI data pin 6; three-state output.
D5	I/O	ULPI data pin 5; three-state output.
D4	I/O	ULPI data pin 4; three-state output.
D3	I/O	ULPI data pin 3; three-state output.
D2	I/O	ULPI data pin 2; three-state output.
D1	I/O	ULPI data pin 1; three-state output.
D0	I/O	ULPI data pin 0; three-state output.
CLOCK	O	60 MHz clock output when digital 19.2 MHz (or 26 MHz) clock is applied; Push-pull output.

Notes:
1. I=input; O=output; I/O=digital input/output; OD=open-drain output; AI/O=analog input/output; P=power or ground.
2. Per USB2.0, below a supply of 2.97 V, USB full-speed and low-speed transactions are not guaranteed; although some devices may continue to function with the FUSB2805 at the lower supply rail.

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Functional Description

ULPI Interface Controller

The FUSB2805 provides a 12-pin interface (SDR) compliant with the UTMI+ Low-Pin Interface (ULPI) specification, revision 1.1. This interface must be connected to the USB link controller.

The ULPI controller provides the following functions:

- ULPI-compliant interface and register set
- Full control of USB peripheral, host, and On-The-Go functionality
- Prioritizes USB receive data, USB transmit data, interrupts, and register operations
- Parses USB transmit and receive data
- Controls the V_{BUS} external source
- V_{BUS} monitoring, charging, and discharging
- Low-power mode
- 6- and 3-pin serial modes
- Generates RX CMDs (status updates)
- Maskable interrupts
- Control over the ULPI bus state

USB Serializer and Deserializer

The USB data serializer prepares data for transmitting onto the USB bus. To transmit data, the USB link controller sends a transmit command and data on the ULPI bus. The serializer performs parallel-to-serial conversion, bit stuffing, and Non Return to Zero, Invert (NRZI) encoding. For packets with a PID, the serializer adds a SYNC pattern to the start of the packet and an EOP pattern to the end of the packet. When the serializer is busy and cannot accept more data, the ULPI interface controller de-asserts NXT.

The USB data deserializer decodes data received from the USB bus. When data is received, the deserializer strips the SYNC and EOP patterns, if applicable, then performs serial-to-parallel conversion, NRZI decoding, and bit unstuffing on the data payload. The ULPI interface controller sends the data to the USB link controller by asserting DIR, then asserting NXT whenever a byte is ready. The deserializer also detects various receive errors, including bit-stuff errors, elasticity buffer under-run or over-run, and byte-alignment errors.

USB 2.0 ATX

The USB 2.0 ATX block is an analog front-end containing the circuitry needed for transmitting, receiving, and terminating the USB bus in high speed (HS), full speed (FS), and low speed (LS); for USB peripheral, host, and OTG implementations; per the USB2.0 specification and its relevant supplements. The following circuitry is included:

- Differential drivers for transmitting data at HS, FS, and LS
- Differential receiver and single-ended receivers for receiving data at HS, FS, and LS
- Squelch circuit to detect HS bus activity
- HS disconnect detector
- 45 Ω HS bus terminations on DP and DM for peripheral and host mode
- 1.5 kΩ pull-up resistor on DP for FS for peripheral mode only (DM resistor pull up for LS peripheral is not supported since FUSB2805 is HS capable.)
- 15 kΩ bus terminations on DP and DM for host mode only

PLL and Clock Generation

The FUSB2805 has a built-in Phase Locked Loop (PLL) for clock generation.

The PLL takes the square wave clock (19.2 MHz or 26 MHz) from the CLKIN and multiplies or divides it into various frequencies for internal use.

From the clock source, the PLL produces the following frequencies:

- 60 MHz clock for the ULPI interface controller
- 1.5 MHz for low-speed USB data
- 12 MHz for full-speed USB data
- 480 MHz for high-speed USB data

Interface Protection

To prevent incorrect activity when the ULPI interface is not correctly driven by the link, such as when the link controller powers up slower than the FUSB2805, there is a weak pull-up resistor on the STP pin.

If the STP is unexpectedly HIGH at any time, the FUSB2805 protects the ULPI interface by enabling weak pull-down resistors on D[7:0].

This interface protection scheme can be disabled by setting the INTF_PROT_DIS bit to 1b (INTF_CNTRL[7]).

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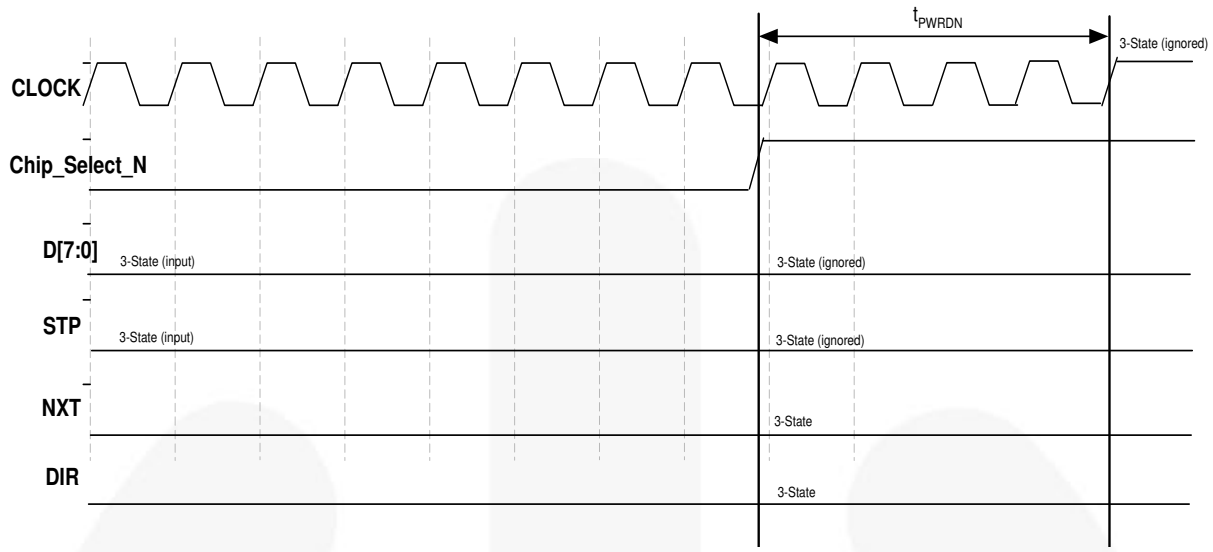


Figure 3. ULPI Behavior with Chip_Select_N as a Power-Down Control Signal

Power Down Using Chip_Select

When CHIP SELECT_N is de-asserted (HIGH), the FUSB2805 three-states the ULPI interface pins and powers down the internal circuitry. If CHIP SELECT_N is not used as a power-down control signal, it is tied to a LOW. Figure 3 shows the ULPI interface behavior when CHIP SELECT_N is asserted and subsequently de-asserted.

After the t_{PWRDN} duration, the CLOCK output enters three-state and is ignored by the link.

Power-On Reset (POR)

The power supply for the internal regulators is V_{CC}. This supply is fed into the 3.3 V and 1.2 V regulators. The output of the 3.3 V regulator is V_{CC3V3}. The 1.2 V regulator generates V_{DD1V2}.

During the power-up stage, the POR is held in a stable state to ensure that the digital logic does not operate the I/O or any analog circuit in such a way that may be damaging to the rest of the system.

The output of the POR block, PORB (internal signal), should be 1'b0 during the power supply ramping period. Once the power supplies have completely ramped, PORB should be de-asserted. This signal is driven into the 19.2 / 26 MHz to 12 MHz PLL. The POR signal (active HIGH reset) in the USB OTG PHY block must remain asserted for no less than 40 µs.

PORB de-assertion is determined via a comparator on V_{CC3V3} with a POR trigger threshold, V_{POR}, of 2.0 V.

Figure 4 illustrates how PORB should be pulsed based on the voltage level of V_{CC3V3}. This diagram also shows what the POR should do to PORB when V_{CC3V3} drops below V_{POR} for any length of time.

When CLOCK starts toggling after power up, the USB link controller must issue a reset command over the ULPI bus to ensure correct operation.

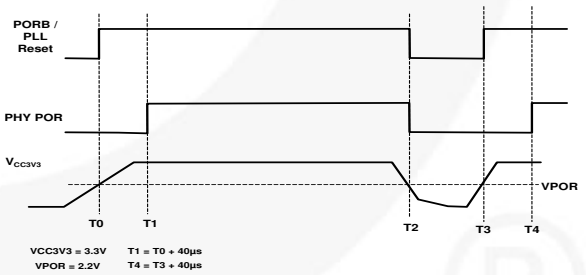


Figure 4. Power-On Reset Sequence

OTG Module

The OTG module contains several sub-blocks that provide the functionality required by the USB On-The-Go Rev. 1.3 supplement. Specifically, it provides the following circuits:

- ID detector to sense the ID pin of the micro-USB cable. The ID pin dictates which device is initially configured as the host and which is configured as the peripheral.
- V_{BUS} comparators to determine the V_{BUS} voltage level. This is required for Host Negotiation Protocol (HNP) and Session Request Protocol (SRP).
- Resistors to temporarily charge and discharge V_{BUS}. This is required for SRP.

ID Detector

Detects which end of the mini-USB (or micro-USB) cable is plugged in. The ID detector must first be enabled by setting the ID_PULLUP register bit to 1b. If the FUSB2805 senses a value on ID different from the previously reported value, an RX CMD status update is sent to the USB link controller or an interrupt is asserted.

If the micro-B end of the cable is plugged in, the FUSB2805 reports that ID_GND is logic 1 and the USB link controller changes to peripheral mode.

If the micro-A end of the cable is plugged in, the FUSB2805 reports that ID_GND is logic 0 and the USB link controller changes to host mode.

The ID pin has a weak pull-up resistor (400kΩ) to avoid floating conditions. This resistor is connected when ID_PULLUP register bit is 0. If the application does not use the ID pin, tie this pin to V_{CC3V3}.

V_{BUS} Comparators

The FUSB2805 provides three comparators for detecting the V_{BUS} voltage level, as listed in Table 9 and Table 12. The comparators are as follows:

V_{BUS}-Valid Comparator

This comparator is used by an A-device (or host) to determine whether or not the voltage on V_{BUS} is at a valid level for operation. The minimum threshold for the V_{BUS} valid comparator is 4.4 V. Any voltage on V_{BUS} below this threshold is considered a fault. During power-up, the comparator output is ignored.

Session-Valid Comparator

The session-valid comparator is a TTL-level input that determines when V_{BUS} is high enough for a session to start. Both the A-device and the B-device use this comparator to detect when a session is being started. The A-device also uses this comparator to determine when a session is completed. The session valid threshold is between 0.8 V to 2.0 V.

Session-End Comparator

The session-end comparator determines when V_{BUS} is below the B-device session-end threshold of 0.2 V to 0.8 V. The B-device uses this threshold to determine when a session has ended.

SRP Charge and Discharge Resistors

The FUSB2805 provides on-chip resistors for short-term charging and discharging of V_{BUS}. These are used by the B-device to request a session, prompting the A-device to restore V_{BUS} power. First, the B-device verifies that V_{BUS} is fully discharged from the previous session by setting the DISCHARGE_VBUS register bit to 1b and waiting for SESS_END to be 1b. Then the B-device charges V_{BUS} by setting the CHARGE_VBUS register bit to 1b. The A-device detects that V_{BUS} is charged above the session-valid threshold and starts a session by turning on V_{BUS} power.

Analog Reference Module

The analog reference module provides stable internal voltage and current references for biasing internal analog circuitry. This module requires an accurate external reference resistor. A value of 12 kΩ ±1% resistor is required between the R_{REF} pin and GND.

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Detailed Description of Pins

D0 to D7

D0 to D7 are bi-directional ULPI data bus pins. The USB link controller must drive D0-D7 LOW when the ULPI bus is idle (DIR is LOW). When the link has data to transmit to the FUSB2805, it drives a non-zero value.

The data bus can be re-configured to carry different data types. There are four modes of the data bus:

- Synchronous mode: default is SDR mode[3], with the 8-bit data bytes being synchronous to the rising edge of CLOCK.
- Low-power mode: carries asynchronous line state and V_{BUS} information.
- 3-pin serial mode: carries asynchronous 3-pin FS/LS serial signaling.
- 6-pin serial mode: carries asynchronous 6-pin FS/LS serial signaling.

Data pins can also be three-stated by driving chip_select_N HIGH.

Note:
3. DDR is not supported by the FUSB2805.

V_{IO}

V_{IO} is the input power pin that sets the I/O voltage level. V_{IO} powers the on-chip pads of the following pins:

- CLOCK
- DIR
- STP
- NXT
- D0-D7
- RESET_N
- CFG1

R_{REF}

Resistor reference analog I/O pin. A 12 kΩ ±1% resistor is required.

DP and DM

When in USB mode, the DP pin functions as USB data plus line; the DM pin functions as USB data minus line.

The DP and DM pins should be connected to the D+ and D- pins of the USB receptacle.

FAULT

This input pin is used by an external SMPS or power management IC to signal an over-current or over-voltage fault condition. This is applicable in OTG host where PSW is used to control driving V_{BUS} or signaling for higher charging currents to an OTG SMPS management IC, as shown in Figure 5.

ID

For OTG implementation, the ID (identification) pin is connected to the ID pin of the mini-USB (or micro-USB) receptacle. As defined in the OTG specification, the ID pin dictates the initial role of the link controller. If ID is detected as HIGH, the link controller must assume the role of peripheral. If ID is detected as LOW, the link controller must assume the host role. Roles can be swapped later using Host Negotiation Protocol (HNP).

The FUSB2805 provides an internal pull-up resistor to sense the value of the ID pin. The pull-up resistor, with a value of 50 kΩ, must first be enabled by setting the ID_PULLUP register bit to 1b. If the value on ID has changed, the FUSB2805 sends an RX CMD or interrupt to the link controller by time t_{ID}. If the link controller does not receive any RX CMD or interrupt by t_{ID}, then the ID value has not changed.

To avoid a floating ID pin, a 400 kΩ resistor pull-up is switched in when ID_PULLUP register bit is set to 0b.

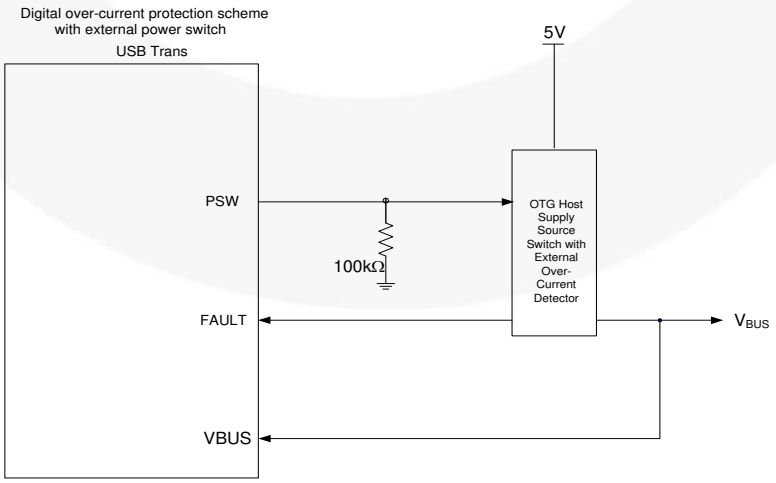


Figure 5. Digital Over-Current Detection Scheme

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V_{CC}

V_{CC} is the main input supply voltage for FUSB2805. The FUSB2805 operates correctly when V_{CC} is between 2.7 V and 4.5 V. The maximum transients that should be seen on V_{CC} are 5.5V for a maximum of 5ms. A 100nF decoupling capacitor is preferred.

PSW

This is an active-HIGH, open-source, power-switch analog output. This pin can be connected to an external V_{BUS} switch or an external charge pump enable circuit to control the external V_{BUS} power source. If the link controller is in host mode, this can be set via the DRV_VBUS and DRV_VBUS_EXT bits in the OTG control register to logic 1. The FUSB2805 drives PSW to HIGH to enable the external V_{BUS} supply. If the link controller detects an over-current condition (V_{BUS_valid}=0), it should disable the external V_{BUS} supply by setting DRV_VBUS_EXT to 0b. An external 100 kΩ pull-down resistor is used.

In addition, the polarity of the signal that controls PSW can be changed via the INTF_CTRL register.

V_{BUS}

This power I/O pin acts as input to the V_{BUS} comparators and over-current detector.

When the DRIVE_VBUS bit of the OTG control register is set to 1b, an external V_{BUS} source tries to drive V_{BUS} to a voltage of 4.4 V to 5.25 V with an output current capability of at least 8 mA.

V_{CC3V3} and V_{DD1V2}

Regulator output voltages. These supplies are used to internally power digital and analog circuits.

CLKIN

Clock input pin; CLKIN is the digital clock input. The allowed frequencies on CLKIN are 19.2 MHz and 26 MHz. The frequency tolerance required by the clock is 50 ppm. The link controller requires a 60 MHz clock from the FUSB2805. This is generated from the PLL, which uses the CLKIN as the input clock.

- 19.2 MHz – CFG1 set to LOW
- 26 MHz – CFG1 set to HIGH

CHIP SELECT_N

Active LOW chip-select pin. When asserted HIGH; D[0-7], CLOCK, DIR, and NXT pins are three-stated and ignored and all internal circuits are powered down, including the regulator. When LOW, the FUSB2805 wakes up and the ULPI pins operate normally.

IR

Direction output pin. This pin is synchronous to the rising edge of CLOCK and controls the direction of the data bus. By default, the FUSB2805 holds DIR LOW, causing the data bus to be an input. When DIR is LOW, the FUSB2805 listens for data from the link controller. The FUSB2805 pulls DIR HIGH only when it has data to send to the link, which is for one of two reasons:

1. To send USB receive data, RX CMD status updates, and register-read data to the link controller.
2. To block the link controller from driving the data bus during power up, reset, and low-power mode (suspend).

The DIR pin can also be three-stated when Chip_Select_N is de-asserted HIGH .

STP

Stop input pin. This signal is synchronous to the rising edge of CLOCK. The link must assert STP to signal the end of a transmit packet or a register-write operation. When DIR is asserted, the link controller can optionally assert STP to abort the FUSB2805, causing it to de-assert DIR in the next clock cycle.

NXT

Next data output pin. This signal is synchronous to the rising edge of CLOCK. The FUSB2805 holds NXT LOW by default. When DIR is LOW and the link is sending data, NXT is asserted to tell the link to provide the next data byte. When DIR is HIGH and the FUSB2805 is sending data to the link, NXT is asserted to tell the link another valid byte is on the bus. NXT is not used for register read data or the RX CMD status update.

The NXT pin can also be three-stated when Chip_Select_N is de-asserted HIGH.

CLOCK

This is the 60MHz interface clock for synchronizing the ULPI bus. It is configured as an output. Being a 12-pin interface implementation, all the ULPI signals are synchronous to the rising edge of CLOCK. The FUSB2805 accepts a digital clock input and outputs the 60MHz to the link.

GND

The global ground signal acts as a ground to all circuits in the FUSB2805.

Reset_N

Reset_N is an active LOW reset signal with V_{IO} voltage. Tie to V_{IO} 1.8 V if not used. Typically tied to the power-on reset signal of the product.

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Modes of Operation

ULPI Modes

The ULPI bus can be programmed to operate in four different modes and a power-down mode. Each mode re-configures the signals on the data bus. Setting more than one mode leads to undefined behavior.

Synchronous Mode

This is the default mode. On power-up and when CLOCK is stable, the FUSB2805 enters synchronous mode.

In synchronous mode, the link controller must synchronize all ULPI signals to CLOCK, meeting the setup and hold times defined in the Dynamic Characteristics tables.

This mode is used by the link controller to perform the following tasks:

- Detect high-speed handshake (chirp)
- Transmit and receive USB packets
- Read and write to registers
- Receive USB status updates (RX CMDs) from FUSB2805

Please refer to section 3.8 of the ULP Rev. 1.1 specification for further details.

Low-Power Mode

When the USB is idle, the link controller can place the FUSB2805 into low-power mode (also known as “suspend” mode). To enter low-power mode, the link controller clears the SUSPENDM bit in the function control (FUNC_CTRL) register to 0b.

During low-power mode, the FUSB2805 provides line state and interrupt information on the data bus for the link controller to monitor basic USB states and draws less than 200 µA from the V_{CC} supply.

In addition, during low-power mode, the clock on CLKIN may be stopped; but it must be restarted before asserting STP to exit low-power mode.

Once in low-power mode, the FUSB2805 must remain in low-power mode for a minimum of 120 clock cycles (or 2 µs). After the 2 µs delay, low-power mode may be exited by asserting the STP signal. The FUSB2805 then issues an RXCMD to the link if a change was detected in any interrupt source and the change still exists. An RXCMD may not be sent if the interrupt condition is removed before exiting.

In low-power mode, the data bus assignments are changed to those described in Table 1.

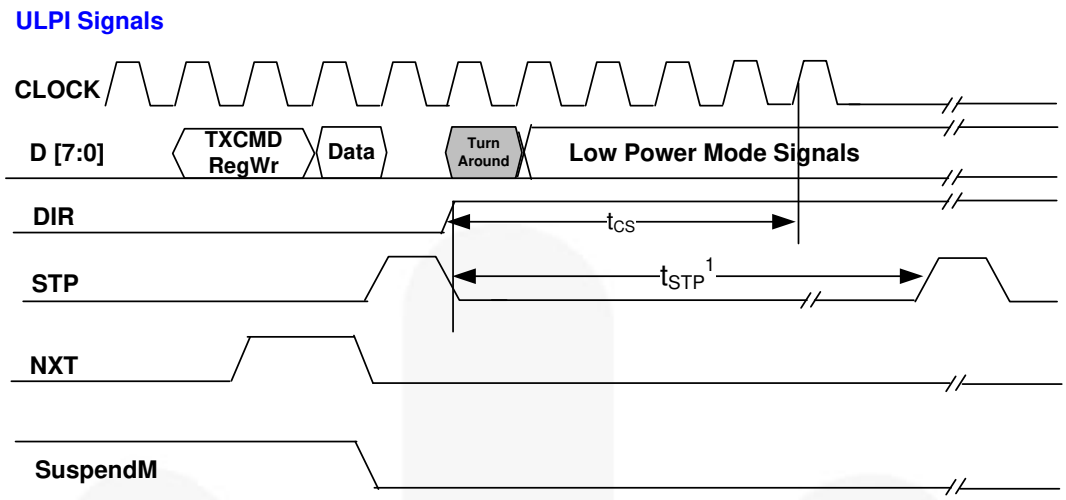
Table 1. Signal Mapping on ULPI Bus During Low-Power Mode

Signal	Maps To	Direction	Description
LINESTATE0	D0	Out	Combinatorial LINESTATE0 directly driven by the analog receiver
LINESTATE1	D1	Out	Combinatorial LINESTATE1 directly driven by the analog receiver
RESERVED	D2	Out	Reserved; the FUSB2805 drives this pin LOW
INT	D3	Out	Active-HIGH interrupt signal; asserted and latched whenever any unmasked interrupt occurs
RESERVED	D[7:4]	Out	Reserved; the FUSB2805 drives these pins LOW

Entering Low-Power Mode

The link sets SuspendM=0b (in Function Control Register) to place the FUSB2805 into low-power mode. The CLOCK may be stopped a minimum of five (5) cycles after the FUSB2805 accepts the register write data as described in Figure 6. When entering low-power mode, the FUSB2805 asserts DIR and holds NXT LOW. There is one cycle of data bus turnaround provided after the assertion of DIR, during which the value of D[7:0] is not valid. Upon completion of the turnaround cycle the FUSB2805 begins driving the signals as described in Table 1.

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Note: The second STP pulse indicates the exit of low-power (suspend) mode

Figure 6. Entering Low-Power Mode

Exiting Low-Power Mode

If the FUSB2805 has been in suspend at least 2 µs, the link may signal the FUSB2805 to exit low-power mode by asynchronously asserting STP. The FUSB2805 immediately starts to wake up its internal circuitry. Upon meeting the ULPI timing requirements the FUSB2805 then de-asserts DIR, ensuring a minimum of 5 cycles of CLOCK have been driven before de-asserting DIR and setting SuspendM=1b (in Function Control Register). The link de-asserts STP in the cycle following the de-assertion of DIR. There is one cycle of data bus turnaround provided after the assertion of DIR, during which the value of D[7:0] is not valid. Upon completion of the turnaround cycle the FUSB2805 begins driving the signals as described in Table 1.

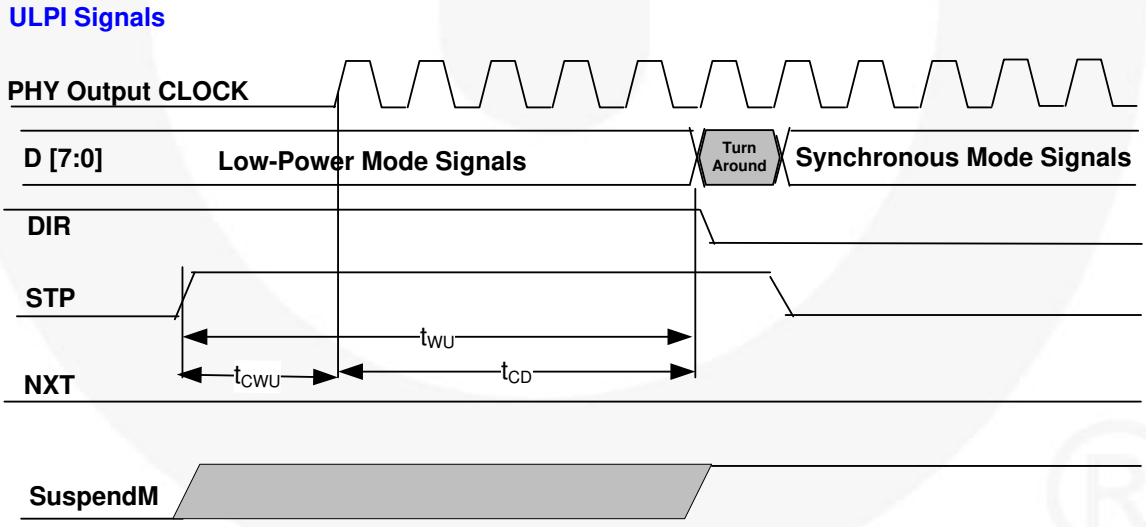


Figure 7. Exiting Low-Power Mode when FUSB2805 Provides Output CLOCK

6-Pin Full-Speed / Low-Speed Serial Mode

This mode of operation is provided for links that contain legacy FS/LS functionality and enables a cost-effective upgrade path to HS functionality.

To enter 6-pin serial mode, the link controller sets the 6PIN_FSLS_SERIAL bit in the interface control register to logic 1. To exit 6-pin serial mode, the link controller asserts STP.

An INT signal is also provided to inform the link of USB events. If the link requires CLOCK to be running during 6-pin serial mode, the CLK_SUSPENDM register bit must be set to logic 1b before entering 6-pin serial mode.

The FUSB2805 requires CLKIN to be kept running when in 6-pin mode. In 6-pin serial mode, the data bus assignments are changed to those described in Table 2. Examples of the signaling of data packets are shown in Figure 22.

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Table 2. Signal Mapping on ULPI Bus During 6-Pin Serial Mode

Signal	Maps To	Direction	Description
TX_ENABLE	D0	In	Active-HIGH transmit enable
TX_DATA	D1	In	Transmit the differential data on DP and DM
TX_SE0	D2	In	Transmit single-ended zero (SE0) on DP and DM
INT	D3	Out	Active-HIGH interrupt signal; asserted and latched whenever any unmasked interrupt occurs
RX_DP	D4	Out	Single-ended receive data from DP
RX_DM	D5	Out	Single-ended receive data from DM
RX_RCV	D6	Out	Differential receive data from DP and DM
RESERVED	D7	Out	Reserved; the FUSB2805 drives this pin LOW

3-Pin FS/LS Serial Mode

This mode is provided for links that contain legacy FS/LS functionality and enables a cost-effective upgrade path to HS functionality.

To enter 3-pin serial mode, the link controller sets the 3PIN_FSLS_SERIAL bit in the interface control register to logic 1. To exit this mode, the link controller asserts STP.

An INT signal is also provided to inform the link of USB events. If the link requires CLOCK to be running during 3-pin serial mode, the CLK_SUSPENDM register bit must be set to logic 1b before entering 3-pin serial mode.

The FUSB2805 requires CLKIN to be kept running when in 3-pin mode. In 3-pin serial mode, the data bus assignments are changed to those described in Table 3. Examples of the signaling of data packets are shown in Figure 21.

Table 3. Signal Mapping on ULPI Bus During 3-Pin Serial Mode

Signal	Maps To	Direction	Description
TX_ENABLE	D0	In	Active-HIGH transmit enable
DAT	D1	I/O	Transmit differential data on DP and DM when TX_ENABLE is HIGH Receive differential data from DP and DM when TX_ENABLE is LOW
SE0	D2	I/O	Transmit single-ended zero on DP and DM when TX_ENABLE is HIGH Receive single-ended zero on DP and DM when TX_ENABLE is LOW
INT	D3	Out	Active-HIGH interrupt signal; asserted and latched whenever any unmasked interrupt occurs
RESERVED	D[7:4]	Out	Reserved; the FUSB2805 drives this pin LOW

Power Supply Modes

The FUSB2805 supports two basic modes of supply operation and include the following:

- Normal Mode
- Power-Down Mode

Normal Mode

This mode is entered when V_{CC} and V_{IO} are powered and Chip_Select_N is asserted.

Power-Down Mode

When chip select is inactive, FUSB2805 enters power-down mode, during which the following apply:

- Chip_Select_N is HIGH or V_{IO} is not present.
- All internal circuits are powered down; total V_{CC} current <36 μA.
- D[0-7], CLOCK, NXT, and DIR are three-stated and ignored; STP is ignored.
- Voltage regulators powering the OTG PHY are turned off.
- Pull-down resistors on the ULPI interface are enabled to prevent a floating bus (V_{IO} present).
- The FUSB2805 is forced into a low-power state and ignores any ULPI commands, including wake-up events.
- If V_{IO} is not present, those signals referenced to V_{IO} are also not powered.

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USB State Transitions

A high-speed USB host or On-The-Go (OTG) device handles more than one electrical state, as defined in the USB and OTG specifications. The FUSB2805 accommodates the various states through the register bit settings of XcvrSelect, TermSelect, OpMode[1:0], DpPulldown, and DmPulldown. Table 4 summarizes the operating states.

Table 4. Operating States and Corresponding Resistor Settings

Signaling Mode	Register Settings					Internal Resistor Settings				
	XcvrSelect[1:0]	TermSelect	OpMode[1:0]	DpPulldown	DmPulldown	rpu_dp_en	rpu_dm_en	rpd_dp_en	rpd_dm_en	hsterm_en
General Settings										
Three-State Drivers	XXb	Xb	01b	Xb	Xb	0b	0b	0b	0b	0b
Power-up or $V_{BUS} < V_{th}$ (SESS_END)	01b	0b	00b	1b	1b	0b	0b	1b	1b	0b
Host Settings										
Host Chirp	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Host High Speed	00b	0b	00b	1b	1b	0b	0b	1b	1b	1b
Host Full Speed	X1b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Suspend	01b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host HS/FS Resume	01b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host Low Speed	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host Low Speed Suspend	10b	1b	00b	1b	1b	0b	0b	1b	1b	0b
Host Low Speed Resume	10b	1b	10b	1b	1b	0b	0b	1b	1b	0b
Host Test_J/Test_K	00b	0b	10b	1b	1b	0b	0b	1b	1b	1b
Peripheral Settings										
Peripheral Chirp	00b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral High Speed	00b	0b	00b	0b	0b	0b	0b	0b	0b	1b
Peripheral Full Speed	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Suspend	01b	1b	00b	0b	0b	1b	0b	0b	0b	0b
Peripheral HS/FS Resume	01b	1b	10b	0b	0b	1b	0b	0b	0b	0b
Peripheral Test_J/Test_K	00b	0b	10b	0b	0b	0b	0b	0b	0b	1b
OTG Device, Peripheral Chirp	00b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG Device, Peripheral High Speed	00b	0b	00b	0b	1b	0b	0b	0b	1b	1b
OTG Device, Peripheral Full Speed	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG Device, Peripheral HS/FS Suspend	01b	1b	00b	0b	1b	1b	0b	0b	1b	0b
OTG Device Peripheral, HS/FS Resume	01b	1b	10b	0b	1b	1b	0b	0b	1b	0b
OTG Device Peripheral, Test_J/Test_K	00b	0b	10b	0b	1b	0b	0b	0b	1b	1b

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Protocol Description

ULPI References

The FUSB2805 provides a 12-pin (SDR) ULPI interface for communication with the link controller. It is strongly recommended that users of the FUSB2805 read the ULPI and UTMI+ specifications as listed below:

UTMI+ Low Pin Interface Specification (ULPI), Revision 1.1, October 20, 2004. http://www.ulpi.org

UTMI+ Specification, Revision 1.0, February 22, 2004. http://www.ulpi.org

ULPI Bus

A description of the ULPI pin signals are given in Table 5. During synchronous mode, all signals are synchronous to CLOCK. Using the ULPI bus, the link controller can perform register reads and writes and transmit data on the USB bus. The FUSB2805 uses the ULPI bus to send status information, decoded USB data, and register contents to the link controller. During low-power and serial modes, all signals are asynchronous to CLOCK, even if the clock is running. An example of ULPI bus usage is shown in Figure 8.

Table 5. ULPI Signal Description

Signal Name	Direction on FUSB2805	Signal Description
CLOCK	OUT	60 MHz interface clock. If a clock is attached on CLKIN, the FUSB2805 drives a 60 MHz output clock. During low-power and serial modes, the clock can be turned off to save power.
D0-D7	I/O	8-bit data bus. In synchronous (SDR) mode, the link drives D0-D7 LOW by default. The link initiates transfers by sending a non-zero data pattern called a TXCMD (transmit command). In synchronous mode, the direction of D0-D7 is controlled by DIR. Contents of the D0-D7 lines must be ignored for exactly one clock cycle whenever DIR changes value; called a “turnaround” cycle. The data lines have fixed directions and different meanings in low-power, 6-pin, and 3-pin serial modes.
DIR	OUT	Controls the direction of the D0-D7 data bus. In synchronous (SDR) mode, the FUSB2805 drives DIR LOW by default, making the data bus an input so the FUSB2805 can listen for TXCMDs from the link controller. The FUSB2805 drives DIR HIGH only when it has data for the link. When DIR and NXT are both HIGH, the byte on the data bus contains decoded USB data. When DIR is HIGH and NXT is LOW, the byte contains status information called an RXCMD (receive command). The only exception is when the FUSB2805 returns register-read data, where NXT is also LOW, replacing the usual RXCMD byte. Every change in DIR causes a turnaround cycle on the data bus, during which D0-D7 are not valid and must be ignored by the link. DIR is always asserted during low-power, 6-pin, 3-pin, and serial modes.
STP	IN	Stop. In synchronous (SDR) mode, the link drives STP HIGH for one cycle after the last byte of data sent to the FUSB2805. The link can optionally assert STP to force DIR to be de-asserted. In low-power and serial modes, the link holds STP HIGH to wake up the FUSB2805, causing the ULPI bus to return to synchronous mode.
NXT	OUT	Next. In synchronous (SDR) mode, the FUSB2805 drives NXT HIGH to throttle data. If DIR is LOW, the FUSB2805 asserts NXT to tell the link controller to place the next data byte on D0-D7 in the following clock cycle. If DIR is HIGH, the FUSB2805 asserts NXT to tell the link controller a valid USB data byte is on D0-D7 in the current cycle. The FUSB2805 always drives an RXCMD when DIR is HIGH and NXT is LOW, unless register-read data is to be returned to the link controller in the current cycle. NXT is not used in low-power or serial modes.

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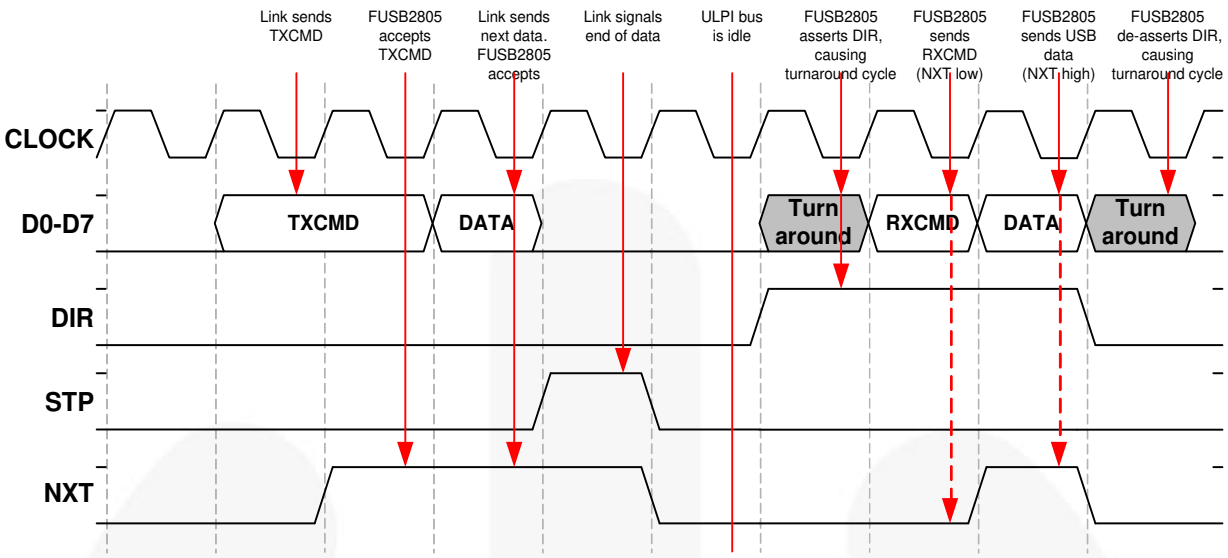


Figure 8. ULPI Generic Data Transmit Followed by Data Receive

On power-up, the FUSB2805 performs an internal power-on reset and asserts DIR to indicate to the link that the ULPI bus cannot be used. When the internal PLL is stable, the FUSB2805 de-asserts DIR. The power-up time depends on the V_{CC} supply rise time and the PLL startup time ($t_{startPLL}$).

Whenever DIR is asserted, the FUSB2805 drives the NXT pin LOW and must drive the data bus (D0-D7) with RXCMD values. When DIR is de-asserted, the link must drive the data bus (D0-D7) to the default LOW. Before beginning USB packets, the FUSB2805 is reset by the link setting the RESET bit in the function control register. After the RESET bit is set, the FUSB2805 asserts DIR until the internal reset completes. The FUSB2805 automatically de-asserts DIR and clears the RESET bit when the reset has completed. After every reset, an RX CMD is sent to the link to update USB status information. After this sequence, the ULPI bus is ready for use and the link can start USB operations.

If Chip_Select_N is de-asserted, the FUSB2805 is retained in power-down mode, where all ULPI interface pins are three-state, internal regulators are shut down, and power consumption is reduced even further than in low-power mode.

If low-power mode is entered due to no V_{IO}, the recommended power-up sequence for the link is:

1. Connect V_{CC} and V_{IO} supplies.
2. Chip_Select_N goes HIGH to LOW to enable the FUSB2805.
3. Link waits for at least t_{PWRUP}, ignoring all ULPI pins' status.
4. The link may start to detect DIR status level; if the DIR is detected LOW, the link may send a reset command.
5. The ULPI interface is ready for use.

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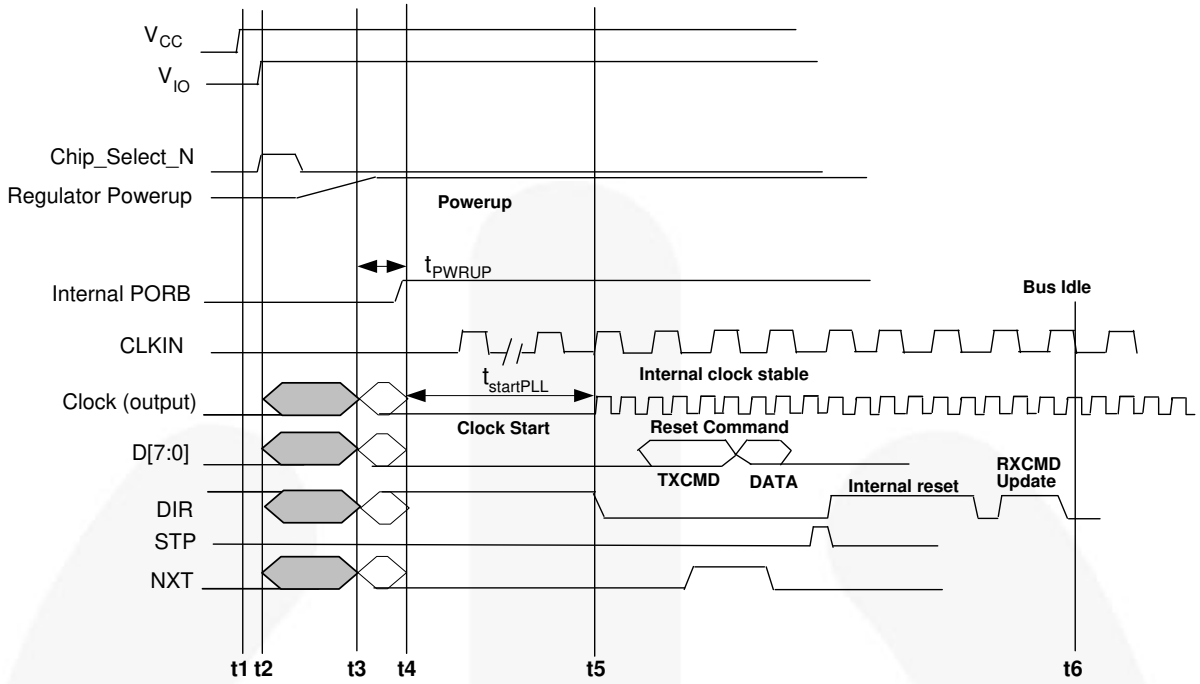


Figure 9. Power-up, Reset, and Bus Idle Sequence for ULPI Ready

Notes:

4. With the CLKIN stable, the FUSB2805 drives a 60 MHz clock out from the CLOCK pin when DIR de-asserts. This is shown as “CLOCK (output)” above.
5. t1: V_{CC} is applied to the FUSB2805.
6. t3: Chip_Select_N transitions to active state (LOW). FUSB2805 internal regulator turns on and the ULPI pins become active (may be driven HIGH or LOW), but should be ignored during the power-up time t_{PWRUP}.
7. t4: After the POR pulse (Power-On Reset), the ULPI pins are driven to a defined level. DIR is driven HIGH, then the other ULPI pins are driven LOW.
8. t5: The PLL stabilizes after the PLL startup time, $t_{startPLL}$. The CLOCK pin begins to output 60 MHz, the DIR pin transitions LOW, and the link must drive STP and D[7:0] to LOW (idle). The link then initiates a reset command to initialize the FUSB2805.
9. t6: The power-up sequence is completed and the ULPI bus interface is ready for use.

V_{BUS} Power and Over-Current Detection

Driving 5 V on V_{BUS} – External Only

No internal charge pump is supported by the FUSB2805. The PSW pin supports an external V_{BUS} supply and is an active HIGH (open source) signal used to control external power management integrated circuits, such as OTG support SMPS devices.

Over-Current Detection

Only external over-current detection is supported by the FUSB2805. An over-current detection circuit is required for host applications that supply more than 100 mA on V_{BUS} between voltages of 4.75 V to 5.25 V.

A digital signal from this external circuit must be connected to the FAULT pin, which directly controls the PSW pin (as shown in Figure 5). The polarity of the signal input to this pin, which controls PSW, is selectable.

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USB Packet Transmit and Receive

When transmitting and receiving USB packets, there are limits set on the link and PHY processing time to ensure that USB inter-packet delays are also met. These times are determined by the USB event and the packet format (i.e. transmit with PID or NOPID, transmit error, receive error, etc.).

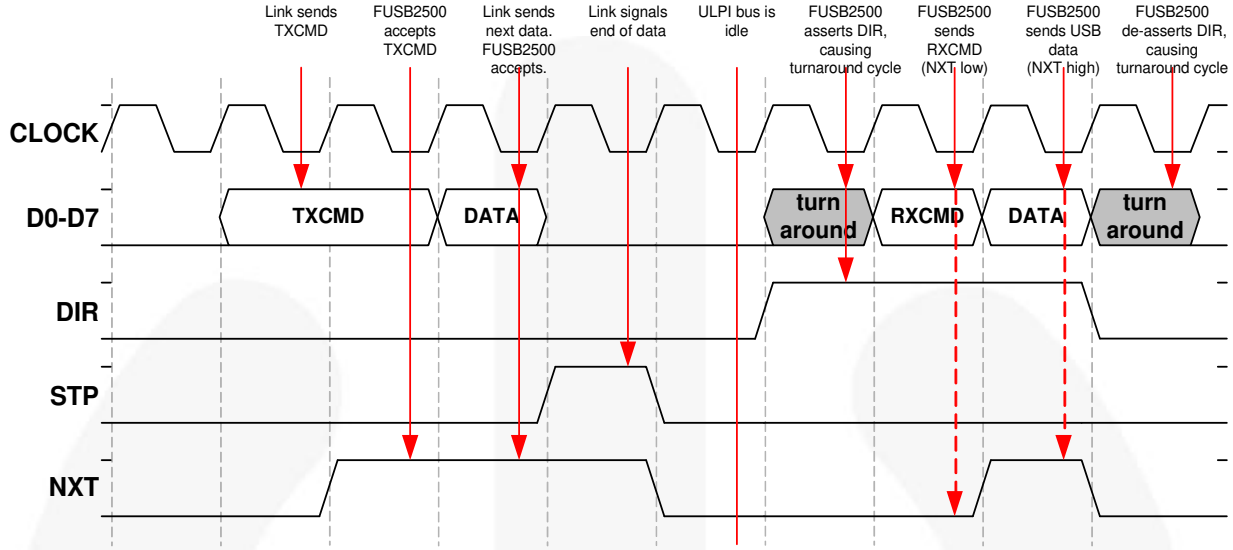


Figure 10. Example ULPI Packet Transmit and Receive

Note:

10. Please refer to ULPI specifications section 3.8.2 for further detail on USB packet operations and functionality.

USB Packet Timing

The USB2.0 specification defines the inter-packet timing and the UTMI/UTMI+ specifications define synchronization and processing delays. The ULPI Rev. 1.1 specification defines the inter-packet delays to ensure compatibility with USB2.0 and supplemental specifications.

Pipeline Delays

Table 6 describes the delays (in clock cycles) with which to comply using ULPI. The USB bus events are measured relative to D+ and D-. The ULPI timings are relative to the clock edge on which the transition is detected (i.e. the clock edge on which STP is detected).

Table 6. Pipeline Delays

Parameter Name	HS PHY Delay	FS PHY Delay	LS PHY Delay	Definition
RXCMD Delay(J/K)	4	4	4	Number of clocks after a change in the internal USB bus state is detected to an RXCMD byte being sent over the ULPI bus. Applies to all changes except SE0.
RXCMD Delay(SE0)	4	4 to 6	16 to 18	Number of clocks between the USB bus state indicating SE0 to an RXCMD byte being sent over the ULPI bus. Delay is increased due to filtering.
TX Start Delay	1 to 2	6 to 10	74 to 75	Number of clocks between the FUSB2805 detecting a TXCMD on the ULPI bus to transmitting the first K of the SYNC pattern on the USB bus.
TX End Delay (packets)	2 to 5	NA	NA	Number of clocks between the FUSB2805 detecting STP on the ULPI bus to completing EOP transmission on the USB bus. HS EOP is completed when all eight consecutive ones have finished transmitting on the USB bus. FS/LS packets finish many clock cycles after STP is asserted. The link must look for RXCMD bytes indicating SE0-to-J transition to determine when the transmission is completed on the USB bus.
TX End Delay (SOF)	6 to 9	NA	NA	HS SOF packets have a long EOP. The link must wait at least nine clocks or for an RXCMD, indicating squelch (LINESTATE=00b), before transmitting the next packet.
RX Start Delay	3 to 8	NA	NA	Number of clocks after first K of SYNC pattern is seen on the USB bus to the simultaneous assertion of DIR and NXT or an RXCMD indicating RxActive. Used for HS packets only. For FS/LS packets, the link must look for RXCMD bytes indicating J-to-K transition.
RX End Delay	3 to 8	17 to 18	122 to 123	Number of clocks after EOP occurs on the USB bus to the FUSB2805 de-asserting DIR or indicating RxActive LOW in an RXCMD byte. HS EOP is completed when all eight consecutive ones have finished transmitting on the USB bus. FS/LS EOP occurs when SE0 starts on the USB bus. For FS/LS, the link uses LINESTATE and not RxEnd delay to time USB packets.

Note:

11. Please refer to ULPI Rev 1.1 specifications, section 3.8.2.6.2 for details on PHY pipeline delays.

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Link Decision Times
The amount of clock cycles allocated to the link to respond to a received packet and correctly receive back-to-back packets is given in Table 7.

Table 7. Link Decision Times

Parameter Name	HS PHY Delay	FS PHY Delay	LS PHY Delay	Definition
Transmit-Transmit (Host Only)	15 to 24	7 to 18	77 to 247	Number of clocks a host link must wait before driving the TXCMD for the second packet. In HS, the link starts counting from the assertion of STP for the first packet. In FS, the link starts counting from the RXCMD indicating LINESTATE has transitioned from SE0-to-J for the first packet. The timings given ensure inter-packet delays of 2.0 to 6.5 bit times.
Receive-Transmit (Host or Peripheral)	1 to 14	7 to 18	16 to 18	Number of clocks the link must wait before driving the TXCMD for the transmit packet. In HS, the link starts counting from the end of the receive packet (de-assertion of DIR or an RXCMD indicating RxActive is LOW). In FS/LS, the link starts counting from the RXCMD indicating LINESTATE has transitioned from SE0-to-J for the receive packet. The timings given ensure inter-packet delays of 2.0 to 6.5 bit times.
Receive-Receive (Peripheral Only)	1	1	1	Minimum number of clocks between consecutive receive packets. The link must be capable of receiving both packets.
Transmit-Receive (Host or Peripheral)	92	80	718	Host or peripheral transmits a packet, then times out after this number of clock cycles if a response is not received. Any subsequent transmission can occur after this time.

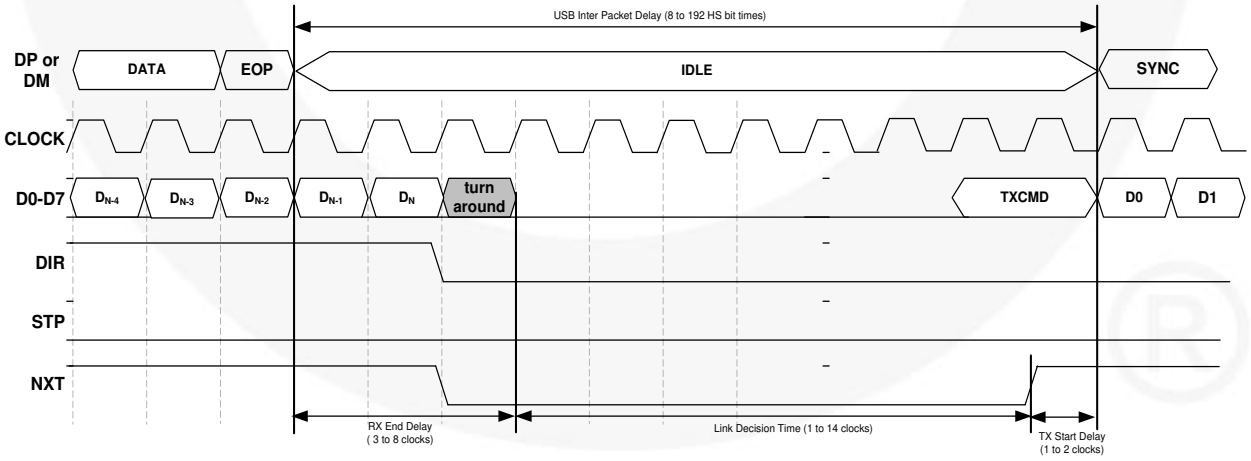


Figure 11. HS Receive to Transmit Packet Timing, Example 1

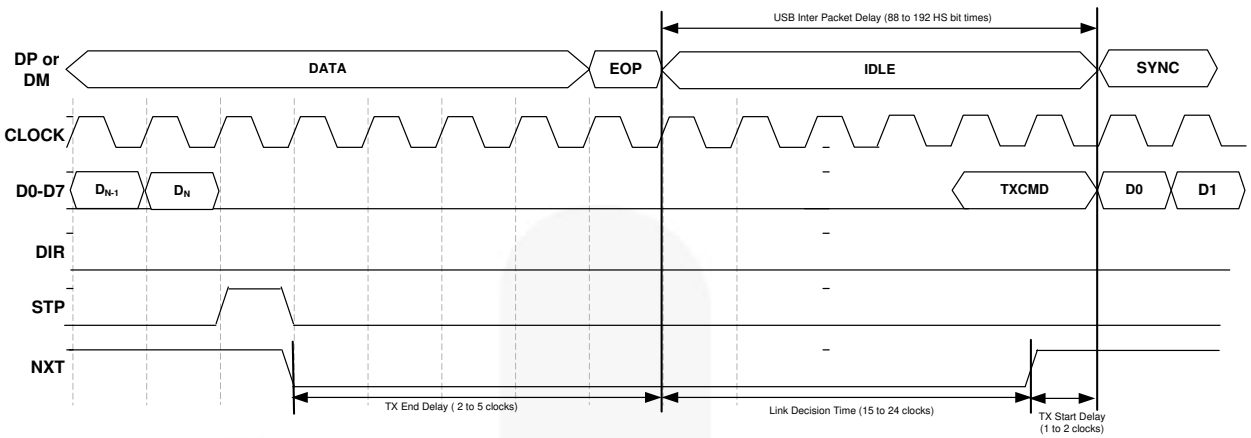


Figure 12. HS Transmit to Transmit Packet Timing, Example 2

Preamble

Preamble packets are headers to low-speed packets that must travel over a FS bus between a host and a hub. To enter preamble mode, the link sets XCVRSELECT[1:0]=11b in the FUNC_CTRL register and, when in this mode (Preamble), the FUSB2805 operates just as in FS mode and sends all the data with the FS rise and fall time characteristics. Whenever the link transmits a USB packet in preamble mode, the FUSB2805 automatically sends a preamble header at the FS bit rate before sending the packet at low-speed bit rate. The FUSB2805 ensures a minimum gap of four FS bit times between the last bit of the FS PRE_PID and the first bit of the LS SYNC. The FUSB2805 drives a J-state for at least one FS bit time after sending the PRE-PID, after which the resistor can hold the J-state on the bus. In preamble mode, the FUSB2805 can also receive LS packets from the FS bus. Figure 13 shows an example preamble packet.

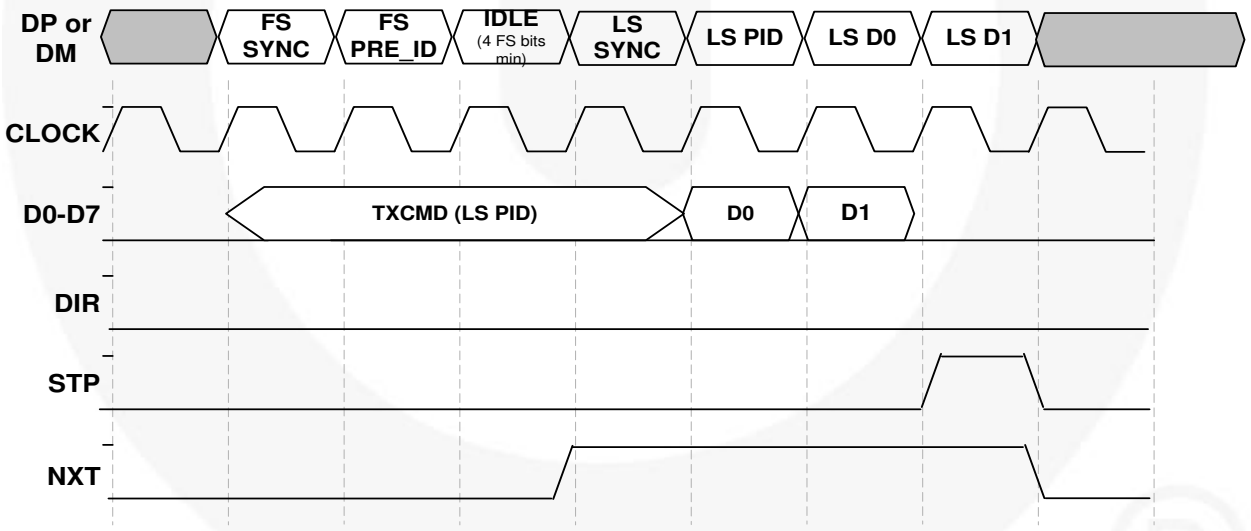


Figure 13. Preamble Sequence

RXCMD and TXCMD

ULPI modifies the original UTMI data stream such that it can fit more data types. Redundancy in the PID byte during transmit is overloaded with ULPI transmit commands (TXCMD). Unused data bytes in the receive stream are overloaded with receive commands (RXCMD). ULPI defines a transmit command byte that is sent by the link and a receive command byte that is sent by the FUSB2805.

Transmit Command (TXCMD)

The link initiates transfers to the FUSB2805 by sending the transmit command (TXCMD) byte, as described in Table 8. TXCMD is comprised of a 2-bit command code and a 6-bit payload.

Table 8. Transmit Commands (TXCMD) from Link to FUSB2805

Command Type Descriptor	Command Code [7:6]	Command Payload [5:0]	Description
IDLE	00b	00 0000b (NOOP)	No operation. 00h is the idle state of the ULPI bus. The link drives NOOP by default.
		XX XXXXb	Reserved command space. Values other than those above create undefined behavior.
TRANSMIT	01b	00 0000b (NOPID)	Transmit USB data that does not have a PID (packet ID), such as chirp, and resume signaling. The FUSB2805 starts transmitting on the USB beginning with the next data byte.
		00 XXXXb (PID)	Transmit USB packet. D[3:0] indicates USB packet identifier PID[3:0].
		XX XXXXb (RSVD)	Reserved command space. Values other than those above create undefined behavior.
REGISTER WRITE	10b	10 1111b (EXTW)	Extended register write command (optional). The 8-bit address must be in the next clock cycle after the command is accepted.
		XX XXXXb (REGW)	Register write command with 6-bit immediate address.
REGISTER READ	11b	10 1111b (EXTR)	Extended register read command (optional). The 8-bit address must be provided in the next clock cycle after the command is accepted.
		XX XXXXb (REGR)	Register read command with 6-bit immediate address.

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Receive Command (RXCMD)

The FUSB2805, after asserting DIR, uses the receive command (RXCMD) byte to update the link on line state, USB receive, disconnect, and OTG information via the ULPI data bus.

The FUSB2805 automatically sends an RXCMD whenever there is a change in any of the RXCMD data fields. The link must be able to accept an RXCMD at any time; including single or multiple (back-to-back) RXCMDs and, at any time during USB receive packets, when NXT is LOW.

Table 9. RXCMD Data Byte Format

<table>
<tr><th>DATA[7:0]</th><th>Status Name</th><th>Description</th></tr>
<tr><td>[1:0]</td><td>LINESTATE</td><td>Line State Signals:
D[0]: LINESTATE0
D[1]: LINESTATE1
LINESTATE[1:0] reflects the current status of DP and DM and is a function of various register settings and whether the device is a host or peripheral. The detailed encoding, and descriptions thereof, is shown in Table 10 and Table 11.</td></tr>
<tr><td>[3:2]</td><td>V_{BUS} State</td><td>Encoded V_{BUS} Voltage State: This encoding is used for over-current detection, session start, and session request (SRP). The Sess_End and Sess_VLD indicators are signals from the internal FUSB2805 V_{BUS} comparators. These encoded V_{BUS} states are:
<table>
<tr><th>Value</th><th>V_{BUS} Voltage</th><th>Sess_End</th><th>Sess_VLD</th><th>A_V_{BUS}_VLD</th></tr>
<tr><td>00b</td><td>$V_{BUS} < V_{B_Sess_End}$</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>01b</td><td>$V_{B_Sess_End} \le V_{BUS} < V_{A_Sess_Vld}$</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>10b</td><td>$V_{A_Sess_Vld} \le V_{BUS} < V_{A_VBUS_Vld}$</td><td>X</td><td>1</td><td>0</td></tr>
<tr><td>11b</td><td>$V_{BUS} \ge V_{A_VBUS_VLD}$</td><td>X</td><td>X</td><td>1</td></tr>
</table></td></tr>
<tr><td>[5:4]</td><td>RxEvent</td><td>RxEvent Encoding: This encoding field of RXCMD is used to inform the link of information packets received on the USB bus. These events are:
<table>
<tr><th>Value</th><th>RxError</th><th>RxActive</th><th>HostDisconnect</th></tr>
<tr><td>00b</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>01b</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>10b</td><td>X</td><td>X</td><td>1</td></tr>
<tr><td>11b</td><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>[6]</td><td>ID</td><td>This bit reflects the state of the ID pin. It is valid 50ms after ID_PULLUP is set to 1b.</td></tr>
<tr><td>[7]</td><td>ALT_INT</td><td>Default is not to use this alternate interrupt bit. The link, optionally, can enable the BVALID_RISE and/or BVALID_FALL bits in the PWR_CNTRL register.
Corresponding changes in BVALID cause an RXCMD to be sent to the link with this ALT_INT bit asserted.</td></tr>
</table>

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Line State Encoding

As mentioned in Table 9, the LINESTATE[1:0] sent to the link is a function of whether the port is upstream (peripheral) or downstream (host) facing. Dual-role OTG devices must select the correct LINESTATE encoding, depending upon its mode. Note that the configuration as a LS peripheral (upstream facing port), with DM pull-up, is not supported by the FUSB2805.

Table 10. LINESTATE[1:0] Encoding for Upstream (Peripheral) Facing Ports; DP_PULLDOWN=0b

Mode	Value	Full Speed	High Speed	Chirp
XCVRSELECT[0:1]		01, 11	00	00
TERMSELECT		1	0	1
LINESTATE[1:0]	00b	SE0	Squelch	Squelch
	01b	FS-J	! Squelch	(! Squelch) AND (HS_Differential_Receiver_Output)
	10b	FS-K	Invalid	(! Squelch) AND (! HS_Differential_Receiver_Output)
	11	SE1	Invalid	Invalid

Notes:
12. (! Squelch) indicates inactive squelch.
13. (! HS_Differential_Receiver_Output) indicates inactive HS_Differential_Receiver_Output.

Table 11. LINESTATE[1:0] Encoding for Downstream (Host) Facing Ports; DP_PULLDOWN and DM_PULLDOWN=1b

Mode	Value	Low Speed	Full Speed	High Speed	Chirp
XCVRSELECT[0:1]		10	01, 11	00	00
TERMSELECT		1	1	0	0
OPMODE[1:0]		X	X	00, 01 or 11	10
LINESTATE[1:0]	00b	SE0	SE0	Squelch	Squelch
	01b	LS-K	FS-J	! Squelch	(! Squelch) AND (HS_Differential_Receiver_Output)
	10b	LS-J	FS-K	Invalid	(! Squelch) AND (! HS_Differential_Receiver_Output)
	11	SE1	SE1	Invalid	invalid

Notes:
14. (! Squelch) indicates inactive squelch.
15. (! HS_Differential_Receiver_Output) indicates inactive HS_Differential_Receiver_Output.

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V_{BUS} Voltage State Encoding

As mentioned in Table 9, changes in the V_{BUS} state encoding initiate an RXCMD to the link. For the link to receive V_{BUS} state updates, the link must first enable the corresponding interrupts in the USB_INTR_EN_R and USB_INTR_EN_F registers. Link uses the indicator signals to take action based on typical configurations (host, peripheral, OTG device). Table 12 shows the V_{BUS} indicators in RXCMD based on the configuration.

Table 12. V_{BUS} Indicator Signals in RXCMD

Configuration	A_VBUS_VLD	SESS_VLD	SESS_END
Standard Host	Yes	No	No
Standard Peripheral	No	Yes	No
OTG A-Device	Yes	Yes	No
OTG B-Device	No	Yes	Yes

For the standard USB host controller application, the following applies:

- The system must be able to provide 500 mA for 4.75 V ≤ V_{BUS} ≤ 5.25 V.
- An external circuit is to be used to detect over-current conditions. If the external over-current detector provides a digital fault signal, the signal must be connected to the FAULT input pin and the link must do the following:

1. Set the IND_COMPL bit in the INTF_CTRL register to 0b or 1b, depending on the polarity of the external fault signal.
2. Set the USE_EXT_VBUS_IND bit in the OTG_CTRL register to 1b.
3. If it is not necessary to qualify the fault indicator with the internal A_VBUS_VLD comparator, set the IND_PASSTHRU bit in the INTF_CTRL register to 1b.

For the standard USB peripheral controller applications, the standard peripherals detect when V_{BUS} is at a sufficient level for operation. SESS_VLD must be enabled to detect the start and end of a USB peripheral operation. Detection of the A_VBUS_VLD and SESS_END thresholds is not needed for standard peripherals.

For a device configured as an OTG B-device, SESS_VLD must be used to detect when V_{BUS} is at a sufficient level for operation. SESS_END must be used to detect when V_{BUS} has dropped to a LOW level, allowing the B-device to safely initiate V_{BUS} pulsing SRP.

A device configured as an OTG A-device must provide a minimum of 8 mA onto V_{BUS}. This 8 mA (minimum) is provided external to the FUSB2805. If the external charge pump source provides more than 100 mA, the over-current circuit must be used and the host controller application criteria apply. The OTG A-device also uses SESS_VLD to detect when an OTG B-device is initiating V_{BUS} pulsing SRP. The control of this external charge pump is accomplished via the PSW pin.

RxEvent Encoding

As mentioned in Table 9, this encoding provides information to the link related to the packets received on the USB bus. The primary encodings are RxActive, RxError, and HostDisconnect.

RxActive

When the FUSB2805 detects a SYNC pattern on the USB bus, it signals an RxActive event to the link. This RxActive event can be communicated in two methods:

- FUSB2805 simultaneously asserts DIR and NXT; or
- FUSB2805 sends an RXCMD to the link with the RxActive field in the RxEvent bits set to 1b.

The link must be capable of detecting both methods and the RxActive frames the receive packet from the first byte to the last byte. It also must assume that RxActive is set to 0b when indicated in an RXCMD or when DIR is de-asserted, whichever occurs first.

The RxActive is also used by the link to time the high-speed packets and ensure that the bus turn-around times are met.

RxError

When the FUSB2805 detects an error while receiving a USB packet, it de-asserts NXT and sends an RXCMD with the RxError field set to 1b. The received packet is no longer valid and must be dropped by the link.

HostDisconnect

This encoding is only valid when the FUSB2805 is configured as a host (DP_PULLDOWN= DM_PULLDOWN=1b) and indicates to the host controller when a peripheral is connected (0b) or disconnected (1b). The host controller must enable HostDisconnect by setting the HOST_DISCON_R and HOST_DISC_F bits in the USB_INTR_EN_R and USB_INTR_EN_F registers, respectively. Changes in HostDisconnect cause the FUSB2805 to send an RXCMD to the link with the updated value.

In peripheral mode, HostDisconnect must be ignored and must not mask events on RxActive or RxError.

Refer to ULPI specifications, section 3.8.1 for details on RXCMD and TXCMD operations and functionality.

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Register Read and Write Operations

The link can read or write register bytes, and set or clear register bits as needed, using the TXCMD byte. The FUSB2805 supports immediate and extended addressing register operations, with the extended register addressing being optional for the link. If the FUSB2805 asserts DIR during an operation, the register operation is aborted. When a register operation is aborted, the link must retry until successful.

Immediate Register Read and Write

Immediate address registers are accessed by first sending the TXCMD byte as either a RegRead or RegWrite command with the required register address.

For RegRead, the link sends its read command request and waits for NXT to assert. In the cycle after NXT asserts, the FUSB2805 asserts DIR to gain control of the bus. In the cycle after DIR asserts, the FUSB2805 must return the register read data. The FUSB2805 does not assert NXT when DIR is asserted during the register read operation, including during the period that the register read data is being returned, to ensure that a USB receive event always overrides the register read during any cycle *(see section 3.8.3.2 of ULPI Rev. 1.1 specification)*. If the FUSB2805 aborts the RegRead by asserting DIR early, the link must retry the RegRead when the bus is idle.

For RegWrite, the link sends its write command request and waits for NXT to assert. In the cycle after NXT asserts, the link sends the register write data and waits for NXT to assert again. When NXT asserts the second time, the link asserts STP in the following cycle to complete the operation. The FUSB2805 must detect STP assertion before it accepts another transmit command. If the FUSB2805 aborts the RegWrite by asserting, DIR the link must retry the RegWrite when the link is idle.

For back-to-back read/write and USB receive signaling, refer to ULPI specifications, section 3.8.3.3 for details and timing waveforms.

Extended Register Read and Write

Extended addressing read (EXTR) and write (EXTW) means that the address is available in the next clock cycle. Accessing immediate address 2Fh indicates an access to the extended register set.

For an EXTR (extended register read), the link sends a register-read command with the address set to 2Fh and waits for NXT to assert. In the cycle after NXT asserts, the link sends the extended register address and waits for NXT to assert again. When NXT asserts the second time, the FUSB2805 asserts DIR to gain control of the bus. In the cycle after DIR asserts, the FUSB2805 must return the register read data. The FUSB2805 does not assert NXT when DIR is asserted during the register read operation, including during the period that the register read data is being returned, to ensure that a USB receive event always overrides the register read during any cycle *(see section 3.8.3.5 of ULPI Rev. 1.1 specification)*. If the FUSB2805 aborts the RegRead by asserting DIR early, the link must retry the RegRead when the bus is idle.

For an EXTW (extended register write), the link sends a register write command with the address set to 2Fh and waits for NXT to assert. In the cycle after NXT asserts, the link sends the extended register address and waits for NXT to assert again. When NXT asserts the second time, the link sends the register write data and waits for NXT to assert again. When NXT asserts the third time, the link asserts STP in the following cycle to complete the operation. If the FUSB2805 aborts the RegWrite by asserting DIR, the link must retry the RegWrite when the bus is idle.

For back-to-back extended read and USB receive signaling, refer to ULPI specifications section 3.8.3.5 for details and timing waveforms.

Please refer to ULPI specification, section 3.8.3 for details on register read and write operations and functionality.

Aborting ULPI Transfers

There are two ways to abort ULPI transfers:

- Link aborted by the FUSB2805
- FUSB2805 aborted by the link.

Link Aborted by the FUSB2805

When the link is transferring data, the FUSB2805 can abort the link by asserting DIR.

FUSB2805 Aborted by the Link

When FUSB2805 has DIR asserted (in synchronous mode), the link can abort by asserting STP. There are very specific criteria to meet in the timing diagram to guarantee the link transaction, which is related to the cycle in which STP is asserted by the link to request aborting the FUSB2805 *(see section 3.3.4.2 of the ULPI Rev. 1.1 specification for timing details)*. While this feature can be used at any time, it is provided to terminate a “babbling” port by disabling the FUSB2805. The FUSB2805 cannot guarantee the validity of USB data during the current packet and the next packet if the link asserts STP during a USB receive packet.

Please refer to ULPI specification, section 3.8.4 for details on aborting ULPI transfers.

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USB High-Speed Detection Handshake (Chirp)

The sequence for detection includes the USB reset and the HS detection handshake (“chirp”) and includes the following sequence of events:

1. USB Reset - The host detects the peripheral attachment (LS if DM is HIGH; FS if DP is HIGH). If LS is detected, the host does not continue with the following sequence of events. If a FS peripheral is detected, it resets the peripheral by writing to FUNC_CTRL and setting XCVRSELECT[1:0]=00b (high speed) and TERMSELECT=0b that drives a SE0 on the bus (DP and DM connected to GND through 45 Ω). The host also sets OPMODE[1:0]=10b for correct chirp transmit and receive. The start of SE0 is defined as T0 time. The peripheral FUSB2805 asserts DIR and informs the link of the LINESTATE change using an RXCMD.

   Note:
   16. The host must also take into account, when receiving chirp signaling, the high-speed differential receiver output so as not to see false bus activity.

2. Peripheral Chirp Response - After detecting the SE0 for no less than 2.5 µs; if HS capable, the peripheral sets XCVRSELECT[1:0]=10b and OPMODE[1:0]=10b, then sends immediately after a TXCMD (NOPID) command. This means a transmission of a chirp-K for no less than 1ms and ending no more than 7 ms after the reset time, T0. If the peripheral is in low-power mode, it must wake up the clock within 5.6 ms, leaving 200 µs for the link to start transmitting the chirp-K and 1.2 ms for the chirp-K to complete (based on worst-case 10% slow clock).

3. Host Chirp Response – If the host does not detect the peripheral chirp, it must continue asserting SE0 until the end of reset. If the peripheral chirp response is detected by the host for a period no less than 2.5 µs, then no more than 100 µs after the bus leaves chirp-K, the host sends a TXCMD(NOPID) with an alternating sequence of chirp-Ks and chirp-Js. Each chirp-K or chirp-J must last no less than 40 µs and no longer than 60 µs.

4. High-Speed Idle Response – The peripheral must detect a minimum of chirp K-J-K-J-K-J, with each chirp detection being for at least 2.5 µs. The peripheral sets TERMSELECT=0b and OPMODE[1:0]=00b after seeing the minimum chirp sequence. The peripheral is in high-speed mode and detects the !squelch (LINESTATE=01b). When the peripheral detects squelch (LINESTATE=10b), it recognizes that the host has completed chirp and waits for HS USB traffic to begin. After transmitting the chirp sequence, the host changes OPMODE[1:0]=00b and begins sending packets.

Figure 14 shows the USB reset and HS chirp sequence.

Refer to ULPI Rev. 1.1 specification, section 3.8.5.1 for details on HS detection timing.

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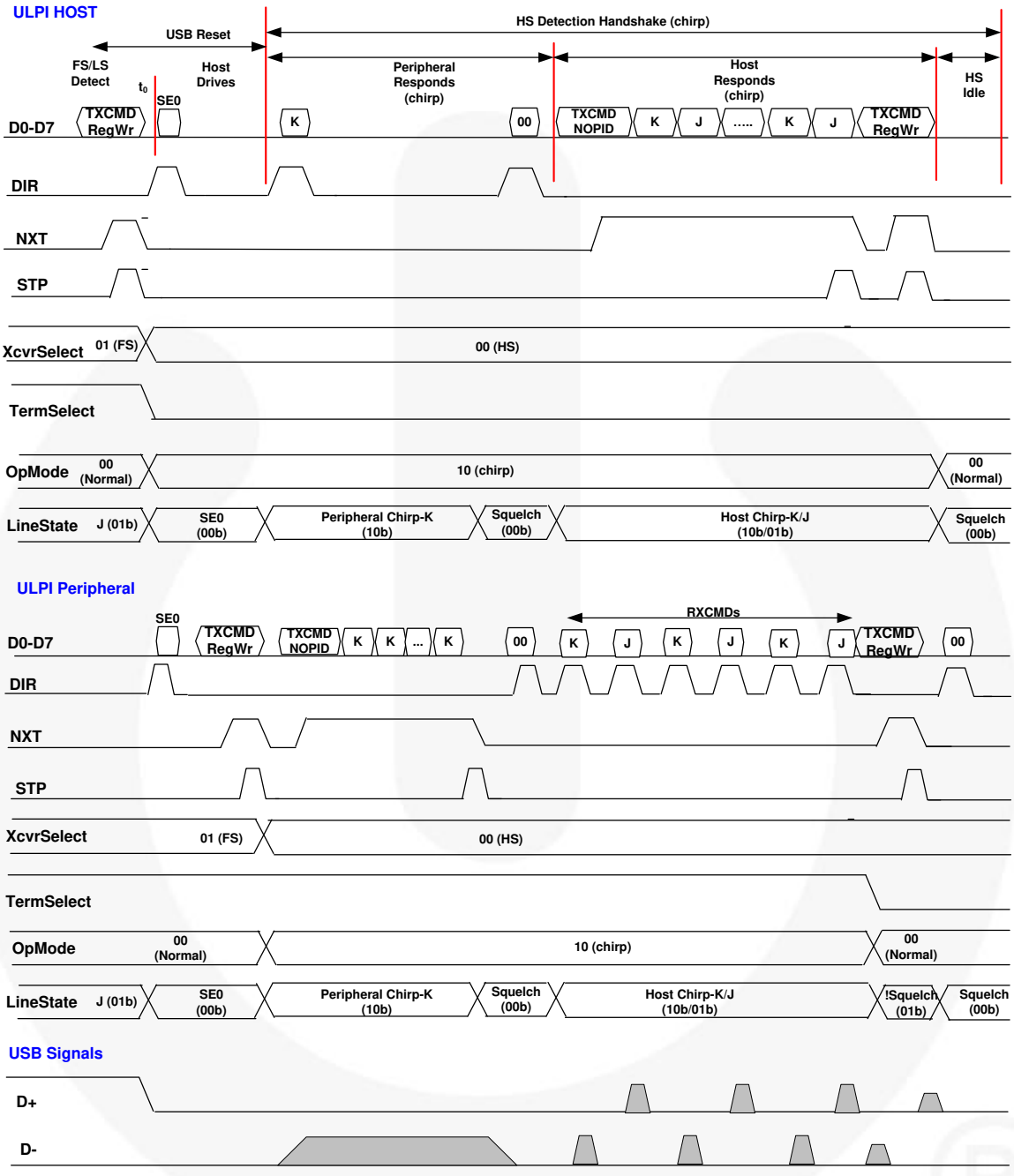


Figure 14. USB Reset and HS Chirp Handshake Timing

Note:

17. Timing is not to scale and not all the RXCMD updates or bus turn-around cycles are necessarily shown. The bus turn-around cycles would be included for one cycle after every assertion and de-assertion of DIR.

USB Suspend and Resume

This section describes the suspend and resume functionality, when initiated by a host or hub, and how to subsequently wake the downstream peripheral.

Full-Speed Suspend and Resume

The sequence of events for a host and peripheral using FUSB2805 is described below and shown in Figure 15.

Sequence of events:

1. FS Traffic – Initially both the host and peripheral are sending FS traffic over the USB bus (XCVRSELECT = 01b). The host has its 15 kΩ pull-down resistors enabled (DP_PULLDOWN = DM_PULLDOWN = 1b) and the 45 Ω terminations disabled (TERMSELECT=1b). The peripheral has the 1.5 kΩ pull-up connected to DP for full-speed. or DM for low-speed (TERMSELECT is set to 1b).
2. Suspend – If the peripheral detects no bus activity for 3 ms, it enters “suspend” state. The peripheral places the FUSB2805 into low-power mode by clearing the SUSPENDM bit in the FUNC_CTRL register, causing the FUSB2805 to draw only suspend current. The host may or may not be powered down.
3. Resume K – When the host wishes to wake the peripheral, it sets OPMODE[1:0]=10b and transmits a K-state for at least 20 ms. The peripheral link detects the resume-K on LINESTATE and asserts STP to wake the FUSB2805.
4. EOP – When STP is asserted, the FUSB2805 on the host side automatically appends an EOP (End of Packet) of two bits of SE0 at LS bit rate, followed by one bit of J-state. The FUSB2805 on the host side knows to add the EOP because DP_PULLDOWN and DM_PULLDOWN are set to 1b for a host. After the EOP is completed, the host link sets OPMODE[1:0]=00b for normal FS operation. The peripheral link detects the EOP and resumes normal FS operation.

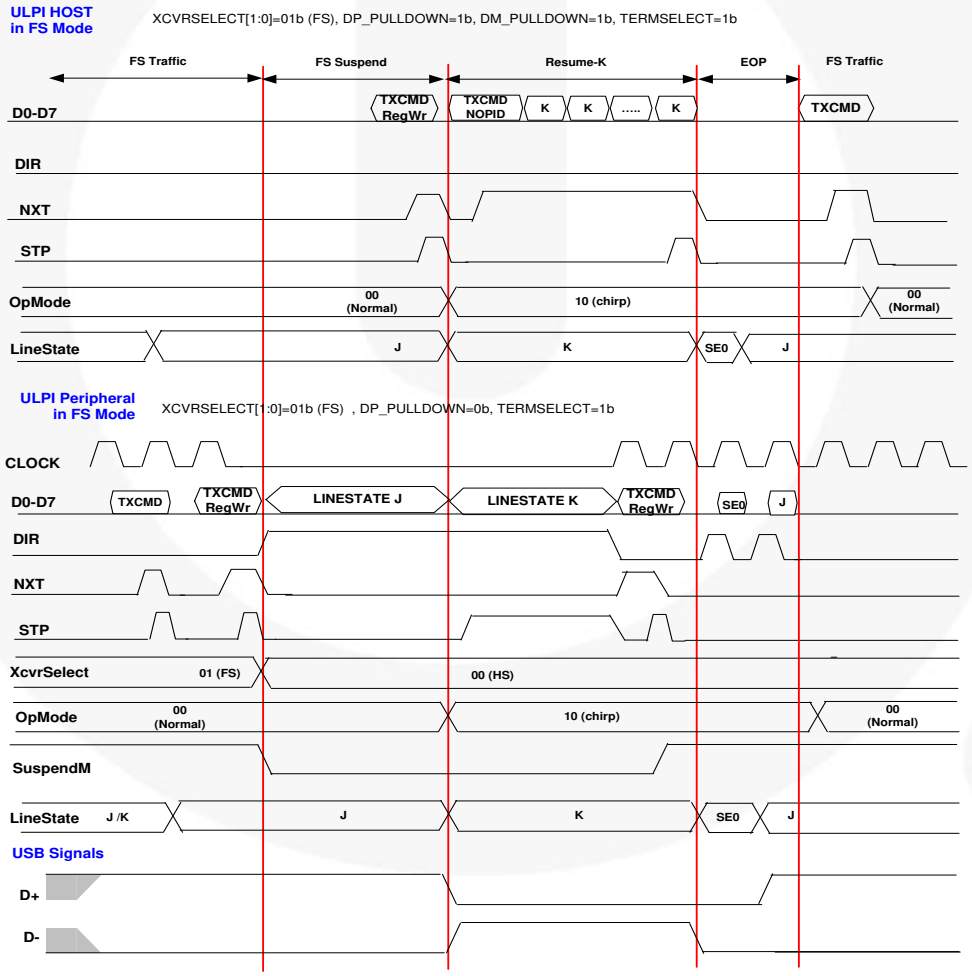


Figure 15. FS Suspend and Resume Timing (Timing Not to Scale)

Note:

18. Timing is not to scale and not all the RXCMD updates or bus turn-around cycles are necessarily shown. The bus turn-around cycles would be included for one cycle after every assertion and de-assertion of DIR.

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High-Speed Suspend and Resume

The sequence of events for a host and HS peripheral using FUSB2805 is described below and shown in Figure 16.

Sequence of events:

1. HS Traffic – Initially both the host and peripheral are idle. The host has its 15 kΩ pull-down resistors enabled (DP_PULLDOWN=DM_PULLDOWN=1b) and the 45 Ω terminations enabled (TERMSELECT=0b). The peripheral has its 45 Ω terminations enabled (TERMSELECT=0b).
2. FS Suspend - If the peripheral detects no bus activity for 3 ms, it enters the suspend state. The peripheral link places the FUSB2805 into FS mode (XCVRSELECT[1:0]=01b), removes the 45 Ω terminations, and enables the 1.5 kΩ pull-up resistor on DP (TERMSELECT=1b). The peripheral link then places the FUSB2805 into low-power mode by clearing the SUSPENDM bit in the FUNC_CTRL register, causing the FUSB2805 to draw only suspend current. The host also changes the FUSB2805 to FS mode (XCVRSELECT[1:0]=01b), removes the 45 Ω terminations (TERMSELECT=1b), and may or may not be powered down.
3. Resume K – When the host wishes to wake the peripheral, it sets OPMODE[1:0]=10b and transmits a full-speed K-state for at least 20 ms. The peripheral link detects the resume-K (10b) on LINESTATE and asserts STP to wake FUSB2805.
4. HS Traffic – the host link sets HS (XCVRSELECT[1:0]=00b) and enables its 45 Ω terminations (TERMSELECT=0b). The peripheral link detects SE0 on LINESTATE, sets HS mode (XCVRSELECT[1:0]=00b), and enables its 45 Ω terminations (TERMSELECT=0b). The host link sets OPMODE[1:0]=00b for normal HS operation.

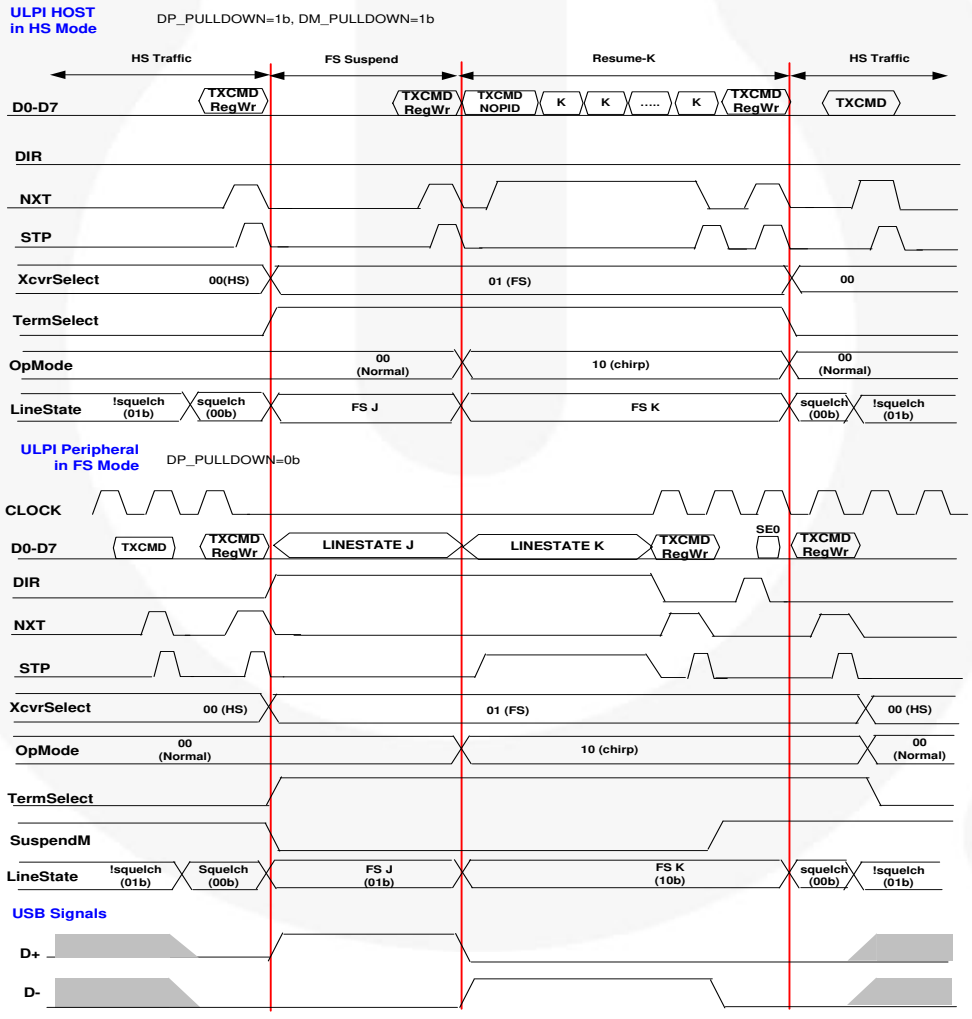


Figure 16. HS Suspend and Resume Timing

Note:

19. Timing is not to scale and not all the RXCMD updates or bus turn-around cycles are necessarily shown. The bus turn-around cycles would be included for one cycle after every assertion and de-assertion of DIR.

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Remote Wake Up

The FUSB2805 supports peripherals that can initiate remote wake-up. When placed into USB suspend, the peripheral remembers the speed at which it was originally operating. Depending on that original operating speed, the link follows one of the protocols described below.

The sequence of events is:

1. Both the host and peripheral are assumed to be in low-power mode.
2. The peripheral begins remote wake-up by re-enabling the clock and setting its SUSPENDM bit=1b.
3. The peripheral begins driving a K-state on the bus to signal resume. The peripheral link must assume that LINESTATE is K (01b) while transmitting (since it does not receive any RXCMDs).
4. The host recognizes the resume, re-enables its clock, and sets its SUSPENDM bit.
5. The host takes over resume driving within 1ms of detecting the remote wake-up.
6. The peripheral stops driving resume.
7. The peripheral recognizes the host continuing to drive the resume.
8. The host stops driving resume and the FUSB2805 automatically adds the EOP to the end of resume. The peripheral recognizes the EOP as the end of resume.
9. Both the host and peripheral revert to normal operation by writing OPMODE[1:0]=00b. If the host or the peripheral was previously in HS mode, it must revert to HS mode before the SE0 of the EOP is completed. This can be achieved by writing XCVRSELECT[1:0]=00b and TERMSELECT=0b after LINESTATE indicates SE0.

Figure 17 shows the remote wake-up timing.

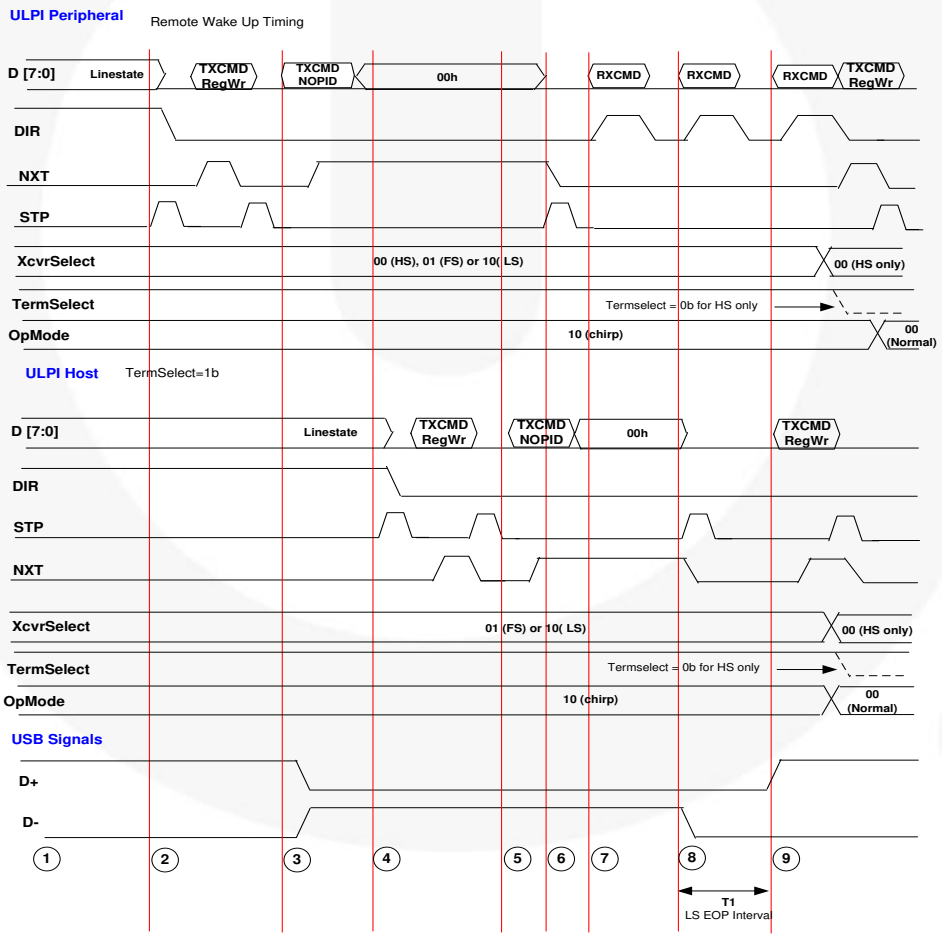


Figure 17. Remote Wake-Up from Low-Power Mode

Note:

20. Timing is not to scale and not all the RXCMD LINESTATE updates or bus turn-around cycles are necessarily shown. The bus turn-around cycles are included for one cycle after every assertion and de-assertion of DIR.

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In some mobile applications; the system clock, CLKIN, may be turned off to conserve battery power. In effect placing the device into a “deep sleep” mode. When this occurs, a remote wakeup event may not be able to start CLKIN or the subsequent internal PHY clock to restore resume signaling in the required 1ms period to the remote wake-up capable device.

To allow for this capability, the FUSB2805 has an autoresume feature.

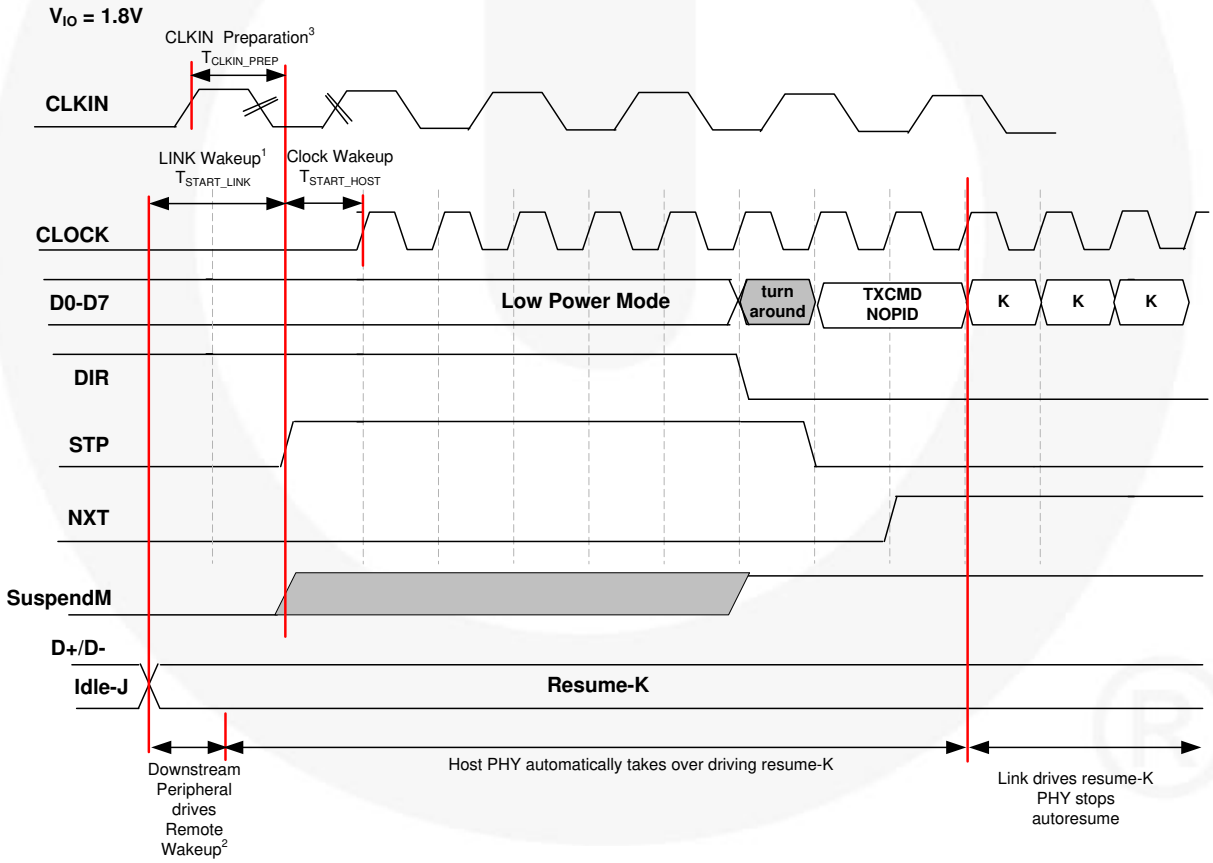
Autoresume

When a USB host detects remote wake-up signaling (resume-K) from a downstream peripheral (or hub), the host must take over the resume-K signaling within 1ms *(see USB2.0 Specification Sections 7.1.7.7 and 7.12).*

Depending on the system architecture, the FUSB2805 may utilize the autoresume feature. When the FUSB2805 is configured as a host and is suspended; CLKIN is running; the STP assertion to exit low-power mode results in the PHY clock restarting in under 1ms. The link can immediately take control of the resume signaling in response to the remote wake-up event. This can be viewed as a ‘light sleep’ mode whereby the PHY is suspended, internal PLL and clock trees are powered down, but power is being dissipated in the system to run CLKIN.

If, however, the implementation is such that the CLKIN is also powered down, it is most likely to take >1 ms to wake from suspended (low-power) mode. In this scenario, the FUSB2805 is required to internally drive resume-K until the PHY clocks are restored and it receives a TXCMD (NOPID type) from the link. With the clock restoration, the link takes over the resume-K signaling to keep the remote wake-up capable peripheral awake. The FUSB2805 is responsible for setting the suspendM register back to 1b before exiting low-power mode. The time taken for this clock wake up is specified as the t_{START_HOST} timing parameter.

The autoresume feature is enabled or disabled according to Table 18 and is described in Figure 18 (timing is not to scale).



[1] Link Wakeup time is a function of the application implementation response to LINESTATE[1:0], the time for CLKIN to become active and for the Link to assert STP within the system. This time needs to meet the UTMI+ and ULPI Specification.
[2] The time from the remote wakeup being signaled and the FUSB2500 driving resume-K is of the order of tens of nanoseconds
[3] The T_{CLKIN_PREP} is the time for CLKIN to have become active prior to STP going high. This always has to be greater than zero

Figure 18. Autoresume Signaling

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No Automatic Generation of SYNC or EOP Packets

This functionality is considered optional in the ULPI specification, but is supported by the FUSB2805 and allows for the link to turn off the automatic generation of SYNC and EOP packets. This is only pertinent to HS packet data. It is provided for backward compatibility for the controllers that include SYNC and EOP bytes in the data payload when transmitting packets. The FUSB2805 does not automatically generate SYNC and EOP when OPMODE[1:0]=11b. The FUSB2805 NRZI encodes the data and performs bit stuffing. The link must always send packets using the TXCMD(NOPID) packet type. The FUSB2805 does not provide bit stuffing on an individual byte basis, but automatically turns off bit stuffing for EOP when STP is asserted with data set to FEh. If data is set to 00h when STP is asserted, the FUSB2805 does not transmit an EOP. The FUSB2805 also detects if the PID byte is A5h (indicating SOF) and automatically sends a long EOP when STP is asserted. To transmit chirp and resume signaling, the link sets OPMODE[1:0]=10b.

Figure 19 shows USB packets without automatic SYNC and EOP generation.

Please refer to ULPI specification, section 3.8.5.6 for details on no SYNC and EOP generation functionality.

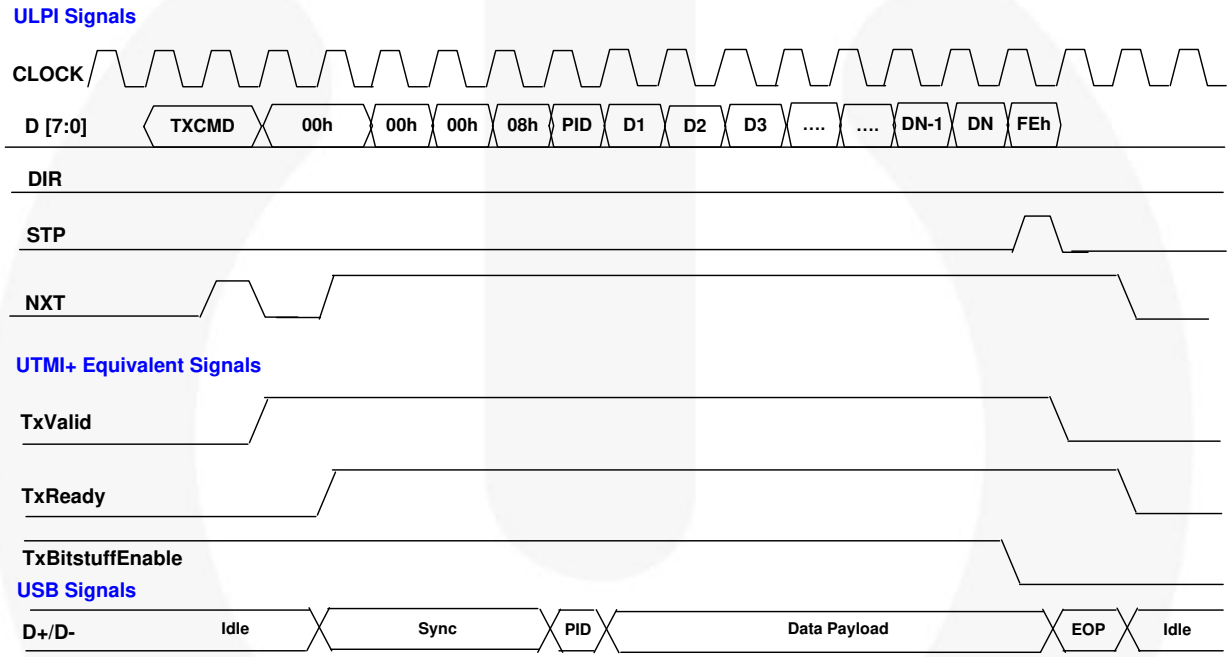


Figure 19. USB Packets without Automatic SYNC and EOP Generation (OpMode=11b)

OTG Operations

The FUSB2805 provides full support for OTG Rev. 1.3 compliance. The supporting functional blocks for dual-role devices include:

- Voltage comparators (for V_{BUS}-valid, session-end, and session-valid signaling)
- DP and DM pull-up and pull-down resistors compliant to the USB2.0 resistor ECN
- ID detection for micro-A or micro-B plug insertion
- V_{BUS} charge and discharge resistors

V_{BUS} Comparators

The FUSB2805 combines the A-device and B-device session valid signals into V_{SESS_VLD} due to overlapping thresholds that allow for such combination.

The $V_{A_VBUS_VLD}$ threshold allows for the A-device to determine if it is capable of outputting a valid voltage on V_{BUS}. For the FUSB2805, the V_{BUS} source voltage is external to the device when an A-device, so the ExtV_{BUS}Indicator signal must be utilized.

These comparators are controlled, and determine when RXCMDs are sent, by interaction with the INTF_CTRL, OTG_CTRL, USB_INTR_R, USB_INTR_F, USB_INTR_STAT, and USB_INTR_L registers.

Table 13 defines use of the UseExternalVbusIndicator, IndicatorPassThru, and IndicatorComplement register bits to control the use of the ExternalVbusIndicator input pin and the internal V_{BUS}-valid comparator output to generate the VA_VBUS_VLD indicator for encoding in the RXCMD data byte.

Figure 20 shows a graphical representation of the RXCMD V_{BUS}-valid.

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Pull-Up and Pull-Down Resistors

The FUSB2805 integrates the DP and DM termination resistors required to initiate data line pulsing. The pull-up and pull-down resistors are connected according to Table 4.

Please refer to ULPI specifications, section 3.8.7, for details on OTG functionality with respect to ULPI or OTG supplement Rev. 1.3 for USB2.0. Please refer to ULPI specifications section 3.8.7.3 for further detail on OTG V_{BUS} comparator thresholds.

Table 13. RXCMD V_{BUS_VALID} Over-Current Conditions

Typical Application	UseExternal V_{BUS}Indicator	IndicatorPass Thru	Indicator Complement	RXCMD V_{BUS} Valid Source
OTG Device	0	Don't Care	Don't Care	Internal $V_{A_VBUS_VLD}$ comparator
	1	1	0	External active HIGH $V_{A_VBUS_VLD}$ signal
	1	1	1	External active LOW $V_{A_VBUS_VLD_N}$ signal
	1	0	1	External active HIGH power fault signal qualified with internal $V_{A_VBUS_VLD}$ comparator
	1	0	0	External active LOW power fault signal qualified with internal $V_{A_VBUS_VLD}$ comparator
Standard Host	1	1	0	External active HIGH power fault signal
	1	1	1	External active LOW power fault signal
Standard Peripheral	0	Don't Care	Don't Care	Internal $V_{A_VBUS_VLD}$ comparator

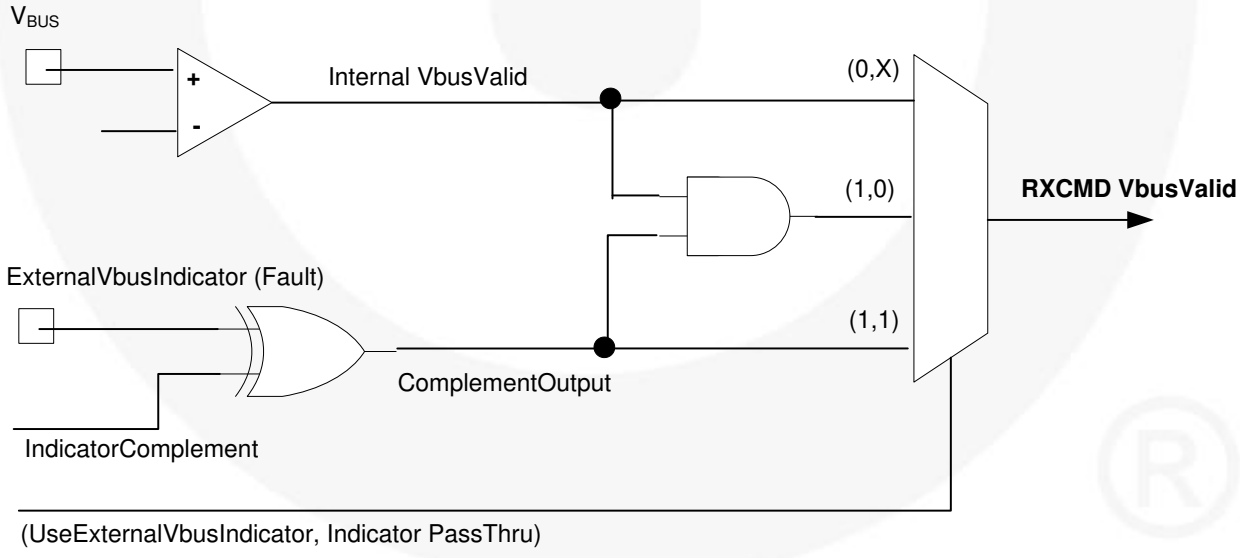


Figure 20. Graphical Representation of the RXCMD V_{BUS}-Valid

Serial Modes

Figure 21 and Figure 22 provide examples of 6-pin and 3-pin serial modes as controlled in the INTF_CTRL register via the 6-pin and 3-pin register bits.

Please refer to ULPI specification, section 3.10 for details on the 3-pin and 6-pin serial mode functionality.

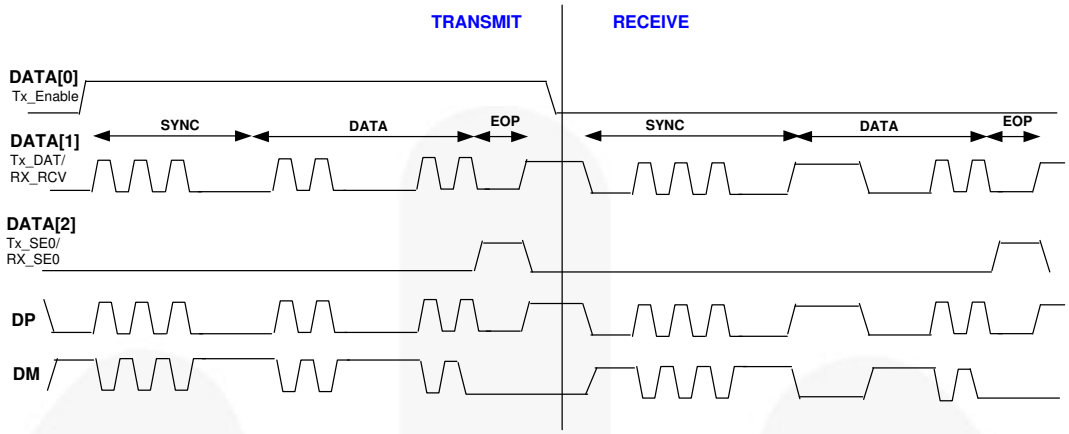


Figure 21. 3-Pin Serial Mode – Transmit and Receive Example

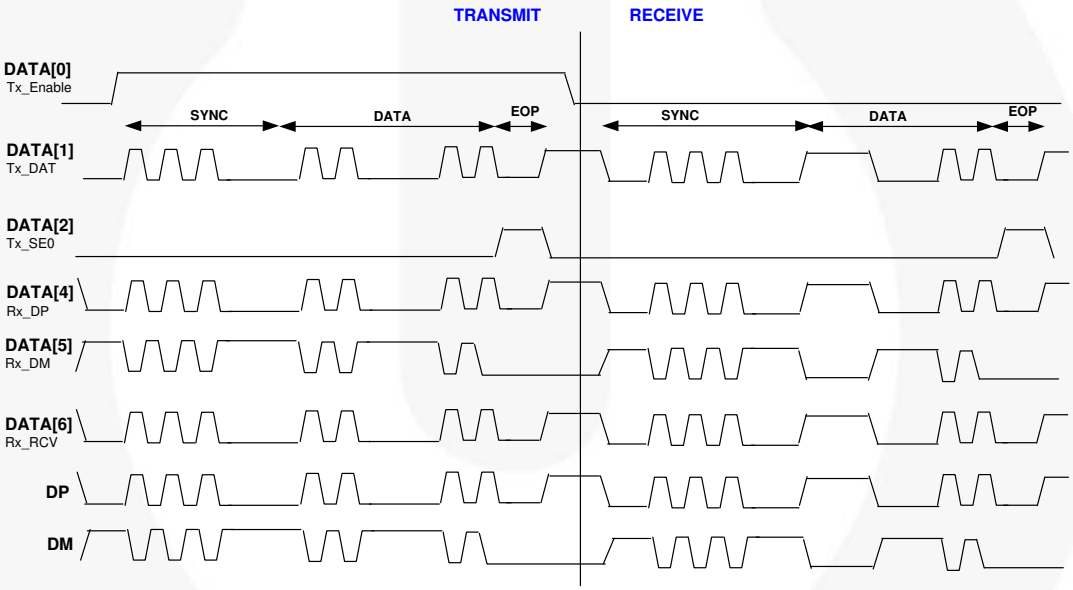


Figure 22. 6-Pin Serial Mode – Transmit and Receive Example

Avoiding Contention on the ULPI Data Bus

Because the ULPI data bus is bi-directional, it is necessary to avoid situations in which both the link and FUSB2805 drive the data bus simultaneously.

The following points should be considered while implementing the data bus drive control on the link.

After the power-up and clock stabilization, the default states are:

- FUSB2805 drives DIR=0.
- Data bus is an INPUT to FUSB2805.
- HOST/LINK ULPI data bus is OUTPUT (with all data bus bits driven to 0).

When FUSB2805 wants to take control of data bus to initiate a data transfer, it changes DIR value from 0 to 1.

At this point, HOST/LINK should disable its output pad buffers. This needs to be as fast as possible, so LINK should use a combinational path from DIR.

FUSB2805 does not enable its output buffers immediately, but delays the enabling buffers until the next clock edge, avoiding bus contention.

When data transfer is no longer required by the FUSB2805, it changes DIR from 1 to 0 and starts to turn off its output drivers immediately. The HOST/LINK senses the change of DIR from 1 to 0, but delays enabling its output buffers for one CLOCK cycle, thereby avoiding data bus contention.

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ULPI Registers

ULPI provides an immediate register set, with a 6-bit address, that is part of the transmit command byte. An extended register set is also provided (8-bit address) that requires an extra clock cycle to complete. The immediate register set is mirrored into the lower end of the extended address space. For example, an operation to the extended address of *00XXXXXX* operates on the immediate register set. The FUSB2805 must support both immediate and extended register operations.

The registers specific to FUSB2805 – vendor ID, product ID, and power control registers, are described in the following sections.

Table 14. Register Map

Field Name	Size (bits)	Address (6 bits)			
		Rd	Wr	Set	Clr
Immediate Register Set					
Vendor ID Low *(see Table 16)*	8	00h			
Vendor ID High *(see Table 16)*	8	01h			
Product ID Low *(see Table 16)*	8	02h			
Product ID High *(see Table 16)*	8	03h			
Function Control *(see Table 17)*	8	04-06h	04h	05h	06h
Interface Control *(see Table 18)*	8	07-09h	07h	08h	09h
OTG Control *(see Table 19)*	8	0A-0Ch	0Ah	0Bh	0Ch
USB Interrupt Enable Rising *(see Table 20)*	8	0D-0Fh	0Dh	0Eh	0Fh
USB Interrupt Enable Falling *(see Table 21)*	8	10-12h	10h	11h	12h
USB Interrupt Status Register *(see Table 22)*	8	13h			
USB Interrupt Latch Register *(see Table 23)*	8	14h			
Debug *(see Table 25)*	8	15h			
Scratch *(see Table 26)*	8	16-18h	16h	17h	18h
Reserved[21]	8	19-2Eh			
Access Extended Register Set *(see below)*	8		2Fh		
Reserved (defined in ULPI specification as vendor specific)	8	30-3Ch			
Extended Register Set		**Address (8 bits)**			
Maps to Immediate Register Set *(see below modes)*	8	00-3Fh			
Reserved (80-FFh defined in ULPI specification as vendor specific)	8	40-FFh			

Note:
21. 19-27h carkit; not supported by FUSB2805.

Table 15. Register Access Legend

Access Code	Expanded Name	Meaning
rd	Read	Register can be read. Read-only if this is the only mode given.
wr	Write	Pattern on the data bus is written over all bits of the register.
s	Set	Pattern on the data bus is OR'd with and written into the register.
c	Clear	Pattern on the data bus is a mask. If a bit in the mask is set, the corresponding register bit is set to zero (cleared).

Notes:
22. The register set above is compliant with the register set defined in the ULPI specifications. *For details, please refer to section 4.0 of the ULPI specifications, version 1.1.*

ULPI Registers Specific to FUSB2805

Table 16. Vendor ID and Product ID Registers

Register	Bits	Access	Address	Value	Description
VENDOR_ID_LOW	7:0	rd	00h	79h	Lower byte of vendor ID supplied by USB-IF. Fixed value of 79h.
VENDOR_ID_HIGH	7:0	rd	01h	07h	Upper byte of vendor ID supplied by USB-IF. Fixed value of 07h.
PRODUCT_ID_LOW	7:0	rd	02h	00h	Lower byte of product ID number. Fixed value of 00h.
PRODUCT_ID_HIGH	7:0	rd	03h	25h	Upper byte of product ID number. Fixed value of 25h.

Function Control Register– FUNC_CTRL (04h-06h Read, 04h Write, 05h Set, 06h Clear)

These registers control the UTMI function settings of the FUSB2805.

Table 17. Function Control Register

Field Name	Bits	Access	Reset	Description
XcvrSelect	1:0	rd/wr/s/c	01b	Selects the transceiver speed: 00b: Enable HS transceiver 01b: Enable FS transceiver 10b: Enable LS transceiver 11b: Enable FS transceiver for LS packets (FS preamble pre-pended by default)
TermSelect	2	rd/wr/s/c	0b	Controls the internal 1.5 kΩ pull-up resistor and 45 Ω HS terminations. Control over the bus resistor changes, as described in Table 4, by the XcvrSelect, OpMode, DpPulldown, and DmPulldown register settings. Since LS peripherals never support FS or HS for HS-capable transceivers, the FUSB2805 does not support providing 1.5 kΩ on D-.
OpMode	4:3	rd/wr/s/c	00b	Selects the required bit encoding style during transmit. 00b: Normal operation 01b: Non-driving 10b: Disable bit stuffing and NRZI encoding 11b: Do not automatically add SYNC and EOP when transmitting. Must *only* be used for HS packets.
Reset	5	rd/wr/s/c	0b	Active HIGH transceiver reset. After the link sets this bit, the FUSB2805 must assert DIR and reset the UTMI+ core. When the reset is completed, the FUSB2805 de-asserts DIR and automatically clears this bit. After de-asserting DIR, the FUSB2805 must re-assert DIR and send an RXCMD update to the link. The link must wait for DIR to de-assert before using the ULPI bus. Does not reset the ULPI interface or ULPI register set. 0b: No Reset 1b: Reset
SuspendM	6	rd/wr/s/c	1b	Active LOW PHY suspend. Puts the FUSB2805 into low-power mode. The FUSB2805 can power down all blocks except the FS receiver, OTG comparators, and the ULPI interface pins. The FUSB2805 must automatically set this bit to 1b when low-power mode is exited (prior to exit STP is asserted by the link). 0b: Low-power mode 1b: Powered
RESERVED	7	rd/wr/s/c	0b	Reserved

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Interface Control Register – INTF_CTRL (07h-09h Read, 07h Write, 08h Set, 09h Clear)

These registers control various interface and PHY features of the FUSB2805. All bits in this register are viewed as optional features in the ULPI Specification Rev 1.1; however, many are supported by the FUSB2805 and are provided for legacy link cores.

Table 18. Interface Control Register

Field Name	Bits	Access	Reset	Description
6-pin FsLsSerialMode 6PIN_FSLS_SER	0	rd/wr/s/c	0b	Changes the ULPI interface to 6-pin serial mode. The FUSB2805 must automatically clear this bit when serial mode is exited. It is an optional mode for support by the ULPI PHY. A PHY with only four data pins, D[3:0] cannot support this mode. 0b: FS/LS packets are sent using the parallel interface. 1b: FS/LS packets are sent using the 6-pin serial interface assignments. CLKIN must remain running.
3-pin FsLsSerialMode 3PIN_FSLS_SER	1	rd/wr/s/c	0b	Changes the ULPI interface to 3-pin serial mode. The FUSB2805 must automatically clear this bit when serial mode is exited. It is an optional mode for support by the ULPI PHY. 0b: FS/LS packets are sent using the parallel interface. 1b: FS/LS packets are sent using the 3-pin serial interface assignments. CLKIN must remain running.
CarkitMode *(not supported in FUSB2805)*	2	rd/wr/s/c	0b	Reserved
ClockSuspendM	3	rd/wr/s/c	0b	Active LOW clock suspend. Used to output CLOCK in serial modes. Internal clock circuitry is not powered down and CLKIN must remain running for serial modes. 0b: Clock is not output in serial modes. 1b: Clock is output in serial modes.
Autoresume	4	rd/wr/s/c	0b	Enables the PHY to automatically transmit resume signaling. 0b: The system is able to wake up its PHY clock in < 1 ms and Autoresume feature is disabled. 1b: The system is unable to wake up its PHY clock in 1 ms and Autoresume feature is enabled. Refer to USB2.0 specification, section 7.1.7.7 and section 7.12 for more information.
Indicator Complement IND_COMPL	5	rd/wr/s/c	0b	Tells the FUSB2805 to invert the ExternalVBUSIndicator input signal, generating the complement output (ie.FAULT). 0b: FUSB2805 does not invert ExternalVBUSIndicator signal (default). 1b: FUSB2805 inverts ExternalVBUSIndicator signal. Refer to 3.8.7.3 and Figure 45 of the ULPI Rev. 1.1, October 2004 specification for details.
Indicator Pass Thru IND_PASS_THRU	6	rd/wr/s/c	0b	Controls whether the complement output is qualified with the internal VBUSValid comparator before being used in the V_{BUS} state in the RXCMD. 0b: Complement output signal is qualified with the internal VBUSValid comparator. 1b: Complement output signal is not qualified with the internal VBUSValid comparator. Refer to 3.8.7.3 and Figure 45 of the ULPI Rev. 1.1, October 2004 specification for details.

Continued on the following page…

Field Name	Bits	Access	Reset	Description
Interface Protect Disable INTF_PROT_DIS	7	rd/wr/s/c	0b	Controls circuitry built into the FUSB2805 for protecting the ULPI interface when the link three-states STP and D[7:0]. Any pull-ups or pull-downs employed by this feature can be disabled. This bit is not intended to affect the operation of the holding state. When this bit is enabled, the FUSB2805 automatically detects when the link stops driving STP. 0b: Enables the interface-protect circuit (default). A weak pull-up resistor is attached to STP and, if STP is unexpectedly HIGH, the FUSB2805 attaches weak pull-down resistors on D[7:0] to protect the data inputs. 1b: Disables the interface-protect circuit. Detaches the weak pull-down resistors on D[7:0] and weak pull-up on STP. *Refer to 3.12 of the ULPI Rev. 1.1, October 2004 specification for details.*

OTG Control Register – OTG_CTRL (0Ah-0Ch Read, 0Ah Write, 0Bh Set, 0Ch Clear)

These registers control the UTMI+ OTG function settings of the FUSB2805.

Table 19. OTG Control Register

Field Name	Bits	Access	Reset	Description
IDPullup	0	rd/wr/s/c	0b	Connects a pull-up to ID line and enables sampling the signal level; 0b: Disables sampling of ID pin 1b: Enables sampling of ID pin
DpPulldown	1	rd/wr/s/c	1b	Enables the 15 kΩ pull-down resistor on D+[23] 0b: Pull-down resistor not connected to D+ 1b: Pull-down resistor connected to D+
DmPulldown	2	rd/wr/s/c	1b	Enables the 15 kΩ pull-down resistor on D-[23] 0b: Pull-down resistor not connected to D- 1b: Pull-down resistor connected to D-
DischrgV_{BUS}	3	rd/wr/s/c	0b	Discharges V_{BUS} through a resistor. A minimum of 656 Ω is defined in the OTG specification. If the link sets this bit to 1b, it waits for an RXCMD indicating SessEnd has transitioned from 0b to 1b, then resets this bit to 0b to stop the discharge event. 0b: Do not discharge V_{BUS} 1b: Discharge V_{BUS}
ChrgV_{BUS}	4	rd/wr/s/c	0b	Charges V_{BUS} through a resistor. Used for V_{BUS} pulsing SRP. A minimum output impedance of 281 Ω with a voltage source of 3.0 V as defined in the OTG specification can be used. The link must first check that V_{BUS} has been discharged *(see DischrgV_{BUS}bit)* and that both D+ and D- have signaled an SE0 for a minimum of 2ms. 0b: Do not charge V_{BUS} 1b: Charge V_{BUS}
Reserved	5	rd/wr/s/c	0b	Reserved
DrvV_{BUS} External	6	rd/wr/s/c	0b	Selects the external 5 V V_{BUS} supply via PSW pin. 0b: Drive PSW LOW 1b: Drive PSW HIGH
UseExternalV_{BUS} Indicator	7	rd/wr/s/c	0b	Tells the FUSB2805 to use an external V_{BUS} over-current indicator. This bit is optional. 0b: Use the internal OTG comparator ($V_{A_VBUS_VLD}$) or internal V_{BUS} valid indicator (default). 1b: Use external V_{BUS} valid indicator signal on FAULT *Refer to 3.8.7.3 of the ULPI Rev. 1.1, October 2004 specification for details.*

Note:

23. Resistor termination implementations conform to USB2.0 resistor ECN.

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USB Interrupt Enable (Rising) Register – INTR_EN_R_CTRL (0Dh-0Fh Read, 0Dh Write, 0Eh Set, 0Fh Clear)

These register bits control the interrupt event notification settings of the FUSB2805 for LOW-to-HIGH signal changes. By default, all transitions are enabled. Interrupt circuitry can be powered down in any mode when both rising and falling edge enables are disabled. To ensure interrupts are detectable when CLOCK is powered down, the link should enable both rising and falling edges.

Table 20. USB Interrupt Enable (Rising) Register

Field Name	Bits	Access	Reset	Description
HostDisconnect Rise	0	rd/wr/s/c	1b	Generates an interrupt event notification when HostDisconnect changes from LOW to HIGH. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b).
V_{BUS}Valid Rise	1	rd/wr/s/c	1b	Generates an interrupt event notification when V_{BUS}Valid changes from LOW to HIGH.
SessValid Rise	2	rd/wr/s/c	1b	Generates an interrupt event notification when SessValid changes from LOW to HIGH. SessValid is the same as UTMI+ AValid.
SessEnd Rise	3	rd/wr/s/c	1b	Generates an interrupt event notification when SessEnd changes from LOW to HIGH.
IDGnd Rise	4	rd/wr/s/c	1b	Generates an interrupt event notification when IDGnd changes from LOW to HIGH. IDGnd is valid 50 ms after IDPullup is set to 1b; otherwise, IDGnd is undefined and should be ignored.
RESERVED	7:5	rd/wr/s/c	0b	Reserved

USB Interrupt Enable (Falling) Register – INTR_EN_F_CTRL (10h-12h Read, 10h Write, 11h Set, 12h Clear)

These register bits control the interrupt event notification settings of the FUSB2805 for HIGH-to-LOW signal changes. By default, all transitions are enabled. Interrupt circuitry can be powered down in any mode when both rising and falling edge enables are disabled. To ensure interrupts are detectable when CLOCK is powered down, the link should enable both rising and falling edges.

Note:

24. RxActive and RxError must always be communicated immediately, these events are not included in this register.

Table 21. USB Interrupt Enable (Falling) Register

Field Name	Bits	Access	Reset	Description
HostDisconnect Fall	0	rd/wr/s/c	1b	Generates an interrupt event notification when HostDisconnect changes from HIGH to LOW. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b).
V_{BUS}Valid Fall	1	rd/wr/s/c	1b	Generates an interrupt event notification when V_{BUS}Valid changes from HIGH to LOW.
SessValid Fall	2	rd/wr/s/c	1b	Generates an interrupt event notification when SessValid changes from HIGH to LOW. SessValid is the same as UTMI+ AValid.
SessEnd Fall	3	rd/wr/s/c	1b	Generates an interrupt event notification when SessEnd changes from HIGH to LOW.
IDGnd Fall	4	rd/wr/s/c	1b	Generates an interrupt event notification when IDGnd changes from HIGH to LOW. IDGnd is valid 50ms after IDPullup is set to 1b; otherwise, IDGnd is undefined and should be ignored.
RESERVED	7:5	rd/wr/s/c	0b	Reserved

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USB Interrupt Status Register – USB_INTR_STAT (13h Read Only)

These register bits indicate the current value of the interrupt event source signal. Interrupt circuitry can be powered down in any mode when both rising and falling edge enables are disabled. To ensure interrupts are detectable when CLOCK is powered down, the link should enable both rising and falling edges.

Table 22. USB Interrupt Status Register

Field Name	Bits	Access	Reset	Description
HostDisconnect	0	rd	0b	Current value of UTMI+ HostDisconnect output. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b). Automatically reset to 0b when low-power mode is entered.
V_{BUS}Valid	1	rd	0b	Current value of UTMI+ V_{BUS}Valid output.
SessValid	2	rd	0b	Current value of UTMI+ SessValid output. SessValid is the same as UTMI+ AValid.
SessEnd	3	rd	0b	Current value of UTMI+ SessEnd output.
IDGnd	4	rd	0b	Current value of UTMI+ IDGnd output. IDGnd is valid 50ms after IDPullup is set to 1b; otherwise, IDGnd is undefined and should be ignored.
RESERVED	7:5	rd	Xb	Reserved

USB Interrupt Latch – USB_INTR_L (14h Read Only with Auto-Clear)

These register bits are set by the FUSB2805 when an unmasked change occurs on the corresponding internal signal. The FUSB2805 automatically clears all bits when the link reads this register or when low-power mode is entered. The FUSB2805 also clears this register when either 6-pin or 3-pin serial mode is entered, regardless of the value of ClockSuspendM. Interrupt circuitry can be powered down in any mode when both rising and falling edge enables are disabled. To ensure interrupts are detectable when CLOCK is powered down, the link should enable both rising and falling edges.

It is optional for the link to read the USB Interrupt Latch register in synchronous mode because the RXCMD byte already indicates the interrupt source directly.

Table 23. USB Interrupt Latch Register

Field Name	Bits	Access	Reset	Description
HostDisconnect Latch	0	rd	0b	Set to 1b by the FUSB2805 when an unmasked event occurs on HostDisconnect. Cleared when this register is read. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b).
V_{BUS}Valid Latch	1	rd	0b	Set to 1b by the FUSB2805 when an unmasked event occurs on V_{BUS}Valid. Cleared when this register is read.
SessValid Latch	2	rd	0b	Set to 1b by the FUSB2805 when an unmasked event occurs on SessValid. Cleared when this register is read. SessValid is the same as UTMI+ AValid.
SessEnd Latch	3	rd	0b	Set to 1b by the FUSB2805 when an unmasked event occurs on SessEnd. Cleared when this register is read.
IDGnd Latch	4	rd	0b	Set to 1b by the FUSB2805 when an unmasked event occurs on IDGnd. Cleared when this register is read. IDGnd is valid 50 ms after IDPullup is set to 1b; otherwise, IDGnd is undefined and should be ignored.
RESERVED	7:5	rd	0b	Reserved

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The FUSB2805 must follow the rules defined in Table 24 for setting any of the Latch register bits. If register read data is returned to the link in the same cycle, a USB interrupt latch bit is set, the interrupt condition is given immediately in the register read data and the latch bit is not set to 1b.

Table 24. Interrupt Latch Register Setting Rules

Input Conditions		
Register Read Data Returned in Current Clock Cycle	**Interrupt Latch Bit Set (1b) in Current Clock Cycle**	**Resultant Value of Latch Register Bit**
NO	NO	0b
NO	YES	1b
YES	NO	0b
YES	YES	0b

Debug Register (15h Read Only)

These register bits indicate the current values of various signals useful for debugging.

Table 25. Debug Register

Field Name	Bits	Access	Reset	Description
LineState0	0	rd	0b	Contains the current value of Linestate0
LineState1	1	rd	0b	Contains the current value of Linestate1
RESERVED	7:2	rd	0b	Reserved

Scratch Register (16h-18h Read, 16h Write, 17h Set, 18h Clear)

These register bits indicate the current values of various signals useful for debugging.

Table 26. Scratch Register

Field Name	Bits	Access	Reset	Description
Scratch	7:0	rd/wr/s/c	00h	Empty register byte for testing purposes. Software can read, write, set, and clear this register and the FUSB2805 functionality is not affected.

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage[25]	Continuous	-0.5	+5.5	V
		Pulse	-0.5	+5.5	
V_{IO}	I/O Supply Voltage		-0.5	+5.5	V
V_{IN}	DC Input Voltage[26]	Pins: STP, DIR, NXT, D[7:0], CFG1, RESET_N, CLKIN	-0.5	V_{IO} + 0.5	V
		Pins: FAULT, Chip_Select_N	-0.5	+5.5	
		Pins: DP, DM, V_{BUS}	-0.5	5.5[27]	
I_{IK}	DC Input Diode Current		-50		mA
I_{LU}	DC Latch-Up Current		-100		mA
T_{STG}	Storage Temperature		-65	+150	°C
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins		6	kV
		I/O to GND		12	
		Power to GND		12	
	Charged Device Model, JEDEC: JESD22-C101			2	
	IEC 61000 Board Level, Air Gap			19	
	Machine Model, JEDEC: JESD22-A115			350	V

Notes:

25. V_{CC} is able to withstand short (up to 5 ms) pulses of up to 5.5 V peak voltage.
26. The input and output negative ratings may be exceeded only if the input and output diode current ratings are observed.
27. V_{BUS} is able to withstand higher voltages using an external series resistance. Target is to withstand >10 V for greater than five (5) seconds with a series resistance of 1 kΩ ±5%.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	2.7	3.6	4.5	V
V_{CC3V3}	Internal Regulated Supply Voltages	V_{CC}-0.1	3.30	3.60	V
V_{DD1V2}		1.08	1.20	1.32	
V_{IO}	I/O Supply Voltage	1.65		3.60	V
V_{IN}	Input Voltage – Digital I/O[28] (STP, D[7:0], CFG1, NXT, DIR, FAULT, CLKIN, RESET_N)	0		V_{IO}	V
	V_{BUS}, Chip_Select_N	0		5.25	
V_{AIO}	Input Voltage – Analog I/O (DP, DM, ID)	-0.5		3.6	V
T_A	Operating Temperature	-40	+25	+85	°C

Note:

28. The digital inputs must be held HIGH or LOW; they must not float.

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Static Characteristics

V_{CC3V3}=V_{CC}-0.1 to 3.6 V; V_{DD1V2}=1.1 V to 1.25 V; V_{IO}=1.65 V to 3.60 V; T_J=-40°C to +85°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply Pins						
V_{POR}	Power-On Reset Trip Voltage	Referenced to V_{DDIO} Supply			1.4	V
I_{VCC}	Operating Supply Current	Full-Speed Data at 12 MHz, 50 pF Load		25		mA
		Full-Speed Data at 12 MHz, Idle		23		
		HS Receiving at 480 MHz		31		
		HS Transmitting at 480 MHz		36		
$I_{VCC(lowpwr)}$	Low-Power Mode Supply Current(32)	Bit SuspendM=0b, CLKIN=LOW, PSW De-asserted		95	200	µA
I_{PWRDN}	Current Drawn from V_{CC} in Power-Down Mode	V_{IO} Off or Chip_Select_N De-asserted, No V_{BUS} Present		22	36	µA
I_{IO}	Operating V_{IO} Supply Current	12pF on CLOCK, ULPI Idle		2.1		mA
$I_{IOPWRDN}$	Static V_{IO} Supply Current in Power-Down Mode	Chip_Select_N De-asserted			2	µA
I_{IOSPND}	Static V_{IO} Supply Current in Suspend Mode (Low-Power)	I/O Pins Idle			2	µA
I_{VBUS_SUSPND}	Static V_{BUS} Supply Current in Suspend Mode (Low-Power)	I/O Pins Idle		60	90	µA
Digital Pins (CLOCK, DIR, STP, NXT, D0-D7, RESET_N)						
V_{IL}	LOW Level Input Voltage				0.3•V_{IO}	V
V_{IH}	HIGH Level Input Voltage		0.7•V_{IO}			V
V_{OL}	LOW Level Output Voltage	I_{OL}=4 mA			0.4	V
V_{OH}	HIGH Level Output Voltage	I_{OH}=4 mA	V_{IO}-0.4			V
I_{PD}	Input Pull-Down Current (Interface Protect – D[7:0])	V_{IN}=V_{IO}	25	50	90	µA
I_{PU}	Input Pull-Up Current (Interface Protect –STP)	V_{IN}=0 V	-30	-50	-80	µA
Digital Pins (FAULT)						
V_{IL}	LOW Level Input Voltage				0.8	V
V_{IH}	HIGH Level Input Voltage		2.0			V
I_{IN}	Input Leakage Current		-1		1	µA
Digital Pins (PSW)						
V_{OHPSW}	HIGH Level Output Voltage-PSW	External 100 kΩ Pull-Down to GND	2.6		3.6	V
I_{OHPSW}	HIGH Level Current-PSW	External 100 kΩ Pull-Down to GND			4	mA

Continued on the following page…

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Static Characteristics (Continued)

V_{CC3V3}=V_{CC}-0.1 to 3.6 V; V_{DD1V2}=1.1 V to 1.25 V; V_{IO}=1.65 V to 3.60 V; T_J=-40°C to +85°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Analog I/O Pins (DP, DM)						
FS/LS Path						
V_{DI}	Differential Input Sensitivity	$\|V_{DP} - V_{DM}\|$			0.2	V
V_{CM}	Differential Common Mode Voltage	Includes V_{DI} Range	0.8		2.5	V
V_{IL}	LOW-Level Input Voltage				0.8	V
V_{IH}	HIGH-Level Input Voltage		2.0			V
V_{OL}	LOW-Level Output Voltage	Pull-Up on DP; R_L=1.5 kΩ to 3.6 V	0		0.3	V
V_{OH}	HIGH-Level Output Voltage	Pull-Down on DP/DM; R_L=15 kΩ to GND	2.8		3.6	V
V_{TERM}	Termination Voltage for 1.5 kΩ Pull-Up Resistor		3.0		3.6	V
R_{PU}	Pull-Up Resistance on DP	Per USB2.0 Resistor ECN	900		1575	Ω
R_{WKPU}	Weak Pull-Up Resistance on DP	Bit DP_WKPU_EN=1, V_{BUS}>$V_{A\text{-}SESS_VLD}$	105.8	132.0	158.0	kΩ
HS Path						
V_{HSSQ}	High-Speed Squelch Detection Threshold	Squelch Detected			100	mV
		No Squelch Detected	150			
V_{DSCHS}	HS Disconnect Detection Threshold (Differential)		525		625	mV
V_{DIHS}	HS Differential Input Sensitivity	$\|V_{DP} - V_{DM}\|$	300			mV
V_{CMHS}	HS Differential Common-Mode Voltage	Includes V_{DIHS} Range	-50		+500	mV
V_{ILHS}	HS Idle-Level Input Voltage (Differential)		-10		+10	mV
V_{IHHS}	HS LOW-Level Input Voltage (Differential)		-10		+10	mV
V_{OLHS}	HS HIGH-Level Output Voltage		360		440	mV
V_{CHIRPJ}	Chirp-J Output Voltage (Differential)		700		1100	mV
V_{CHIRPK}	Chirp-K Output Voltage (Differential)		-900		-500	mV
I_{OZ}	Leakage Current		-4		+4	µA
Z_{DRV}	Driver Output Impedance (Both HS and FS)	Steady-State Conditions per USB2.0	40.5		49.5	Ω
Z_{IN}	Input Impedance		0.8			MΩ
R_{PD}	Pull-Down Resistance on DP, DM	Per USB2.0 Resistor ECN	14.25		24.80	kΩ
$C_{I/O}$	Capacitance	Pin to GND			10	pF
V_{BUS} Comparators						
$V_{th(VBUSVLD)}$	V_{BUS} Valid Threshold		4.40		4.75	V
$V_{th(SESSEND)}$	V_{BUS} Session-End Comparator Threshold		0.2		0.8	V
$V_{hys(SESSEND)}$	V_{BUS} Session-End Comparator Hysteresis			150		mV
$V_{th(SESSVLD)}$	V_{BUS} Session-Valid Comparator Threshold	A-Device and B-Device	0.8		2.0	V
$V_{hys(SESSVLD)}$	V_{BUS} Session-Valid Comparator Hysteresis			200		mV

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Static Characteristics (Continued)

V_{CC3V3}= V_{CC}-0.1 to 3.6 V; V_{DD1V2}=1.1 V to 1.25 V; V_{IO}=1.65 V to 3.60 V; T_J=-40°C to +85°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{BUS} Resistors						
$R_{VBUS(PU)}$	V_{BUS} Charge Resistance	Connect to V_{CC3V3} when CHRG_V_{BUS}=1	281			Ω
$R_{VBUS(PD)}$	V_{BUS} Discharge Resistance	Connect to GND when DISCHRG_V_{BUS}=1	656			Ω
$R_{VBUS(IDLE)}$	V_{BUS} Idle Impedance	Not in Power-Down Mode	80	90	100	kΩ
		Chip Select De-assserted or V_{IO} Lost	40		100	
ID Detection Circuit (ID)						
t_{ID}	ID Detection Time		50			ms
R_{ID_PU}	ID Pull-Up Resistance	Bit ID_PULL_UP=1	40	50	60	kΩ
$R_{ID_PU_WK}$	Weak ID Pull-Up Resistance	Bit ID_PULL_UP=0	320	400	480	kΩ
V_{PU_ID}	ID Pull-Up Reference		3.0	3.3	3.6	V
V_{TH_ID}	ID Threshold		1.0		2.0	V
External Resistor Reference						
V_{RREF}	Voltage Across External R_{REF} (12 kΩ ±1%)	SUSPENDM Bit=HIGH		0.8		V
Reset						
t_{START_HOST}	PHY Clock Startup when Remote Wake-up Event Occurs	CLKIN Running, Autoresume=0			850	µs
		CLKIN Must be Started First[30], Autoresume=1			110.9	µs
Clock Input						
f_{CLKIN}	Input Clock Frequency[31]	USB Config 0		19.2		MHz
		USB Config 1		26.0		
J_{CLKIN}	RMS Jitter				200	ps
δ_{CLKIN}	Duty Cycle			50		%
V_{CLKIN}	Amplitude			1.8		V
t_{R_CLKIN}, t_{F_CLKIN}	Rise and Fall Time				5	ns
Output CLOCK Characteristics						
f_{CLK60_OUT}	Output Clock Frequency	Active Only When a Clock is Input on CLKIN		60		MHz
J_{CLK60_OUT}	RMS Output Jitter				500	ps
δ_{CLK60_OUT}	Duty Cycle			50		%
t_{R_CLK60}	Rise Time	CLOCK Pin Transitioning from 10% to 90% of V_{IO} (C_L 4 – 12 pF)	1.0		4.0	ns
t_{F_CLK60}	Fall Time	CLOCK Pin Transitioning from 90% to 10% of V_{IO} (C_L 4 – 12 pF)	1.0		4.4	ns
$t_{startPLL}$	Startup (PLL Stabilization) Time	Measured from Power Good or Assertion of STP			640	µs

Notes:

29. Excludes suspend current through 15 kΩ host pull-down when configured as a peripheral controller. Typically an additional 200 µA is allowed.
30. Time for CLKIN to be woken up is a function of external system timing, so Autoresume is needed for remote wake-up capability *(please see Figure 18)*.
31. An external clock is to be applied to the CLKIN pin. Recommended frequency accuracy is 200 ppm.

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Dynamic Characteristics

V_{CC3V3}= V_{CC}-0.1 to 3.6 V; V_{DD1V2}=1.1 V to 1.25 V; V_{IO}=1.65 V to 3.60 V; T_J=-40°C to +85°C; unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Output CLOCK Characteristics							
f_{CLK60_OUT}	Output Clock Frequency	Active Only When a Clock is Input on CLKIN			60		MHz
J_{CLK60_OUT}	RMS Output Jitter					500	ps
δ_{CLK60_OUT}	Duty Cycle				50		%
t_{R_CLK60}	Rise Time	CLOCK Pin Transitioning from 10% to 90% of V_{IO} (C_L – 4-12 pF)		1.0		4.0	ns
t_{F_CLK60}	Fall Time	CLOCK Pin Transitioning from 90% to 10% of V_{IO} (C_L - 4-12 pF)		1.0		4.4	ns
$t_{startPLL}$	Startup (PLL Stabilization) Time	Measured from Power Good or Assertion of STP				640	µs
Regulator Characteristics							
$t_{regPWRUP}$	Regulator Power-Up Time	4.7 µF ±20% Decoupling on V_{CC3V3} and V_{DD1V2}				1.2	ms
$t_{regPWRDN}$	Regulator Power-Down Time	4.7 µF ±20% Decoupling on V_{CC3V3} and V_{DD1V2}				100	ms
Digital I/O Pins							
C_{IN}	Pin Input Capacitance	Input-only Pins, (STP, RESET_N)		2.7	3.0	3.5	pF
C_{IN_BIDI}	Pin Input Capacitance	Bi-directional Pins as Input (CLK, D0-D7)		2.7	3.0	3.5	pF
C_{OUT}	Pin Output Capacitance	Output (Digital) Pins (NXT, DIR, CLKOUT)		2.7	3.0	3.5	pF
ULPI Interface Single Data Rate (SDR) Timing							
t_{SU}	Setup Time with Respect to Positive Edge of Clock	Input-only Pins (STP) & Bi-directional Pins (D0-D7) as Inputs	Output 60 MHz Clock	6			ns
t_{HD}	Hold Time with Respect to Positive Edge of Clock	Input-only Pins (STP) & Bi-directional Pins (D0-D7) as Inputs	Output 60 MHz Clock	0			ns
t_{DC}	Output Delay with Respect to Positive Edge of Clock	Output-only Pins (DIR, NXT)	Output 60 MHz Clock, 12 pF on all ULPI pins			9	ns
t_{DD}	Output Delay with Respect to Positive Edge of Clock	Bi-directional Pins as Output (D0-D7)	Output 60 MHz Clock, 12 pF on all ULPI pins			9	ns
t_{rise}	Rise Time	Transitioning from 10% to 90% of V_{IO} (C_L – 4-12 pF)		1.0		5.0	ns
t_{fall}	Fall Time	Transitioning from 90% to 10% of V_{IO} (C_L – 4-12 pF)		1.0		5.0	ns

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Dynamic Characteristics (Continued)

V_{CC3V3}= V_{CC}-0.1 to 3.6 V; V_{DD1V2}=1.1 V to 1.25 V; V_{IO}=1.65 V to 3.60 V; T_J=-40°C to +85°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ULPI Interface Exiting and Entering Low-Power Mode						
t_{CS}	Entering Low-Power Mode Time	From DIR LH Transition-to-CLOCK Stop (6 Cycles Minimum)		0.145		µs
t_{STP}	Low-Power Mode Delay(32)	From DIR LH Transition STP to LH Transition		2		µs
t_{WU}	Exiting Low-Power Mode (Total Wake-Up Time)	From STOP LH Transition to DIR HL Transition		111		µs
t_{CWU}	Exiting Low-Power Mode (Clock Wake-Up Time)	From STOP LH Transition-to-Clock Start		110.9		µs
t_{CD}	Exiting Low-Power Mode (Clock-to-DIR)	From Clock Start-to-DIR HL Transition (6 Clock Cycles)		97		ns
Analog I/O Pins						
High-Speed Driver Characteristics						
t_{HSR}	Differential Rise Time		500			ps
t_{HSF}	Differential Fall Time		500			ps
Full-Speed Driver Characteristics						
t_{FR}	Rise Time	C_L=50 pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
t_{FF}	Fall Time	C_L=50 pF; 10 to 90% of $\|V_{OH} - V_{OL}\|$	4		20	ns
FRFM	Differential Rise Time / Fall Time Matching	Excluding First Transition from Idle State	90.0		111.1	%
V_{CRS}	Output Signal Crossover Voltage	Excluding First Transition from Idle State	1.3		2.0	V
t_{LR}	Rise Time	C_L=200pF to 600pF; 1.5 kΩ pull up on D- enabled; 10 to 90% of $\|V_{OH} - V_{OL}\|$	75		300	ns
t_{LF}	Fall Time	C_L=200pF to 600pF; 1.5 kΩ pull up on D- enabled; 10 to 90% of $\|V_{OH} - V_{OL}\|$	75		300	ns
LRFM	Differential Rise Time / Fall Time Matching	Excluding First Transition from Idle State	80.0		125	%
Serial Mode Driver Timing						
t_{PLHDS}	Driver Serial Mode Propagation Delay (LOW to HIGH)	TX_DAT [D1], TX_SE0 [D2] to D+/D-			20	ns
t_{PHLDS}	Driver Serial Mode Propagation Delay (HIGH to LOW)	TX_DAT [D1], TX_SE0 [D2] to D+/D-			20	ns
$t_{PHZLZDS}$	Driver Serial Mode Disable Delay	TX_ENABLE [D0] to D+/D-			12	ns
$t_{PZHZLDS}$	Driver Serial Mode Enable Delay	TX_ENABLE [D0] to D+/D-			20	ns

Continued on the following page…

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Dynamic Characteristics (Continued)

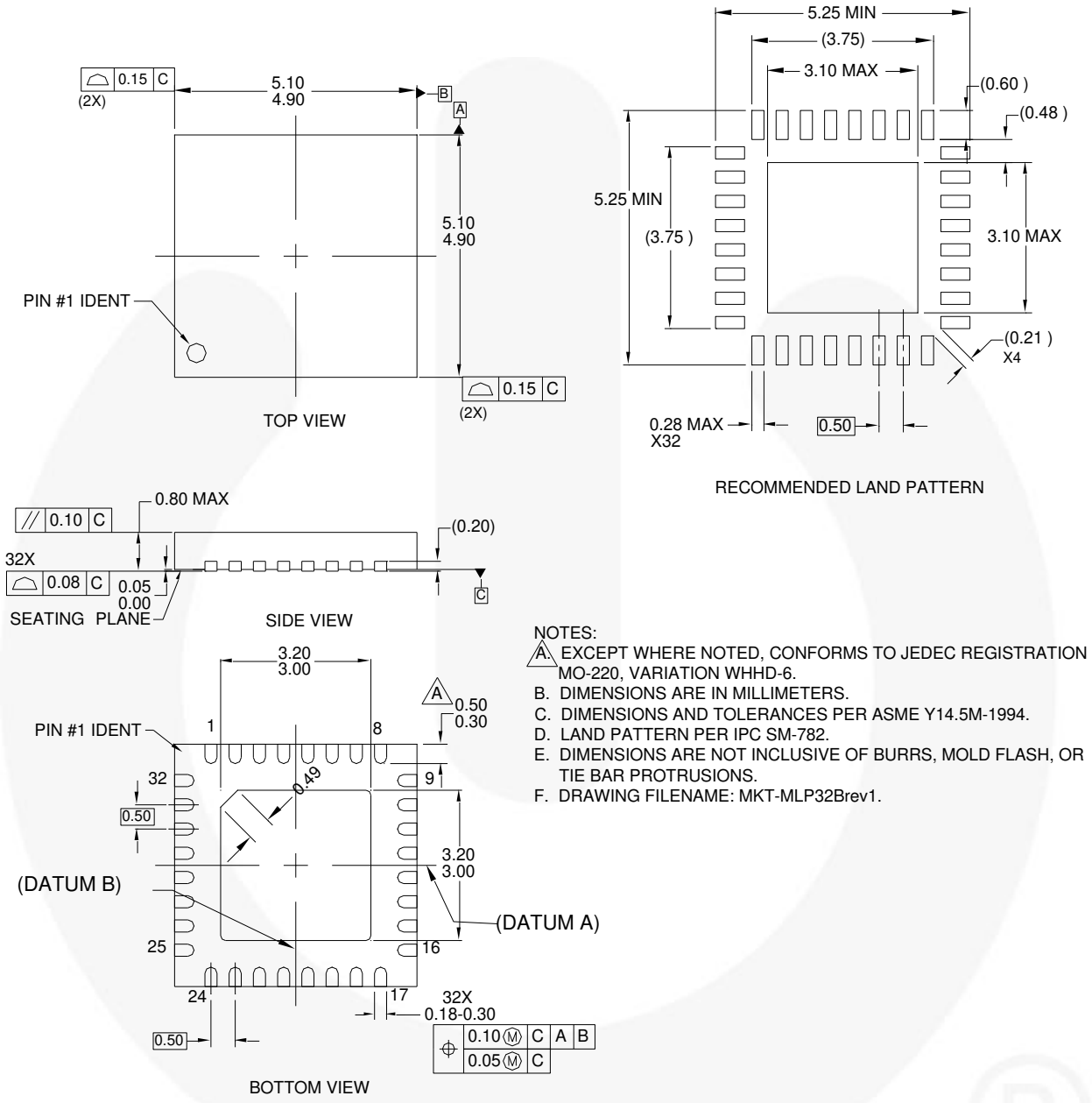
V_{CC3V3}= V_{CC}-0.1 to 3.6 V; V_{DD1V2}=1.1 V to 1.25 V; V_{IO}=1.65 V to 1.95 V; T_J=-40°C to +85°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Serial Mode Receiver Timing						
t_{PLHRS}	Receiver Serial Mode Propagation Delay (LOW to HIGH)	D+/D- to RX_RCV [D6]			20	ns
t_{PHLRS}	Receiver Serial Mode Propagation Delay (HIGH to LOW)	D+/D- to RX_RCV [D6]			20	ns
t_{PLHPS}	Single Ended V_P Serial Mode Propagation Delay (LOW to HIGH)	D+ to RX_DP [D4]			20	ns
t_{PHLPS}	Single Ended V_P Serial Mode Propagation Delay (HIGH to LOW)	D+ to RX_DP[D4]			20	ns
t_{PLHMS}	Single Ended V_M Serial Mode Propagation Delay (LOW to HIGH)	D- to RX_DM [D5]			20	ns
t_{PHLMS}	Single Ended V_M Serial Mode Propagation Delay (HIGH to LOW)	D- to RX_DM [D5]			20	ns

Note:

32. This parameter is guaranteed by design.

Physical Dimensions



NOTES:

A. EXCEPT WHERE NOTED, CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WHHD-6.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
D. LAND PATTERN PER IPC SM-782.
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F. DRAWING FILENAME: MKT-MLP32Brev1.

Figure 23. 32-Lead, Molded Leadless Package (MLP)

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