FUSB303B Autonomous USB Type-C™ Port Controller with I²C and GPIO Control

FUSB303B



QFN12
CASE 722AG

MARKING DIAGRAM



UN	= FUSB303B Device Code
KK	= Lot Trace Code
_	= Pin #1 Identifier
XY	= Two Digit Date Code
Z	= Assembly Plant Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 17 of this data sheet.

Description

The FUSB303B device is a fully autonomous USB Type−C™ controller optimized for 15 W or less applications. The FUSB303B offers CC logic detection for Source Port role, Sink Port role, DRP, and accessory detection support, as well as Dead Battery support as defined in USB−C specifications. The FUSB303B features configurable address I²C access to support multiple ports per system or it can operate autonomously configured by just pins. The FUSB303B features ultra−low power during operation, and an ultra−thin, 12−Lead QFN package.

Features

- Fully Autonomous USB−C™ Port Controller
- Supports Latest Type−C™ Specification Release 1.3
- Source, Sink, and DRP Port role Configuration with Optional Accessory Support
- Try.SRC and Try.SNK modes for Preferring Source Role or Sink Role Respectively
- V_{DD} Operating Range, 2.85−5.5 V
- Typical Low Power Operation: I_{CC} < 10 μA
- GPIO and I²C Configuration
- Max 28 V DC Tolerance on ID, VBUS_DET, CC1 and CC2
- Dead Battery Support (Sink Port role when No Power Applied)
- 4 kV HBM ESD Protection for Connector Pins
- Small Packaging, 12 Lead QFN (1.6 mm × 1.6 mm × 0.375 mm)

Applications

- Smartphones
- Tablets
- Laptops
- Accessoires
- Industrial
- Power Banks

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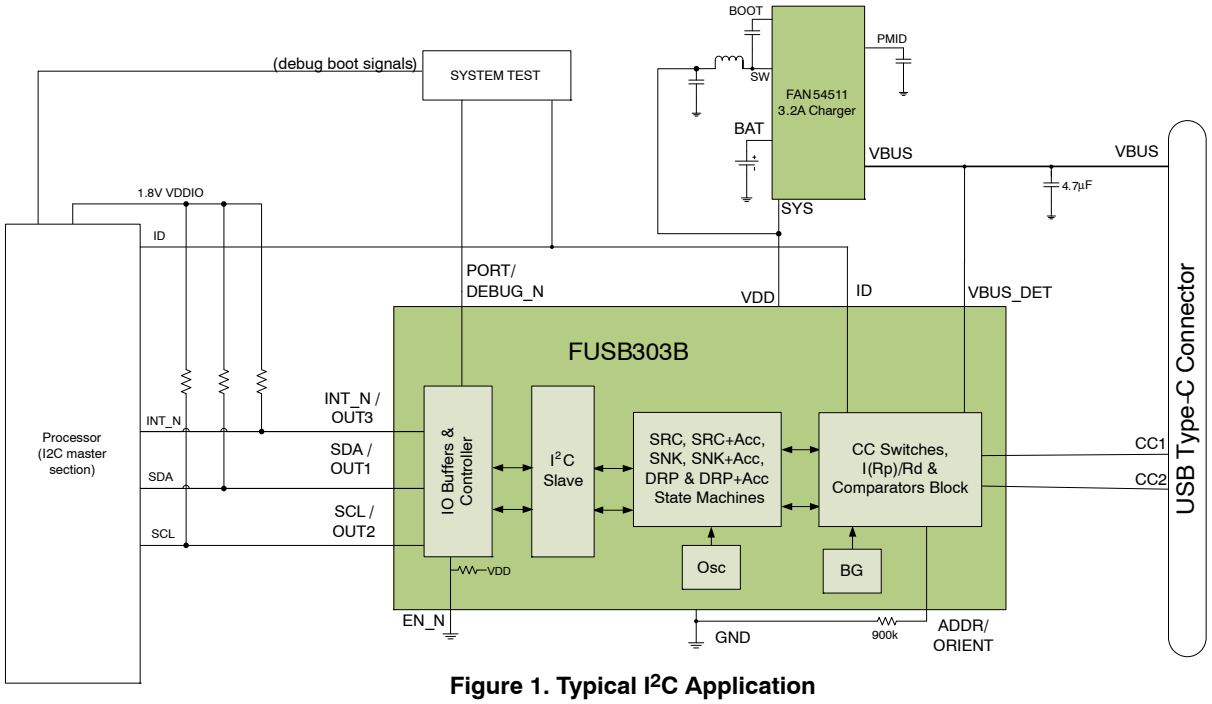


Figure 1. Typical I²C Application

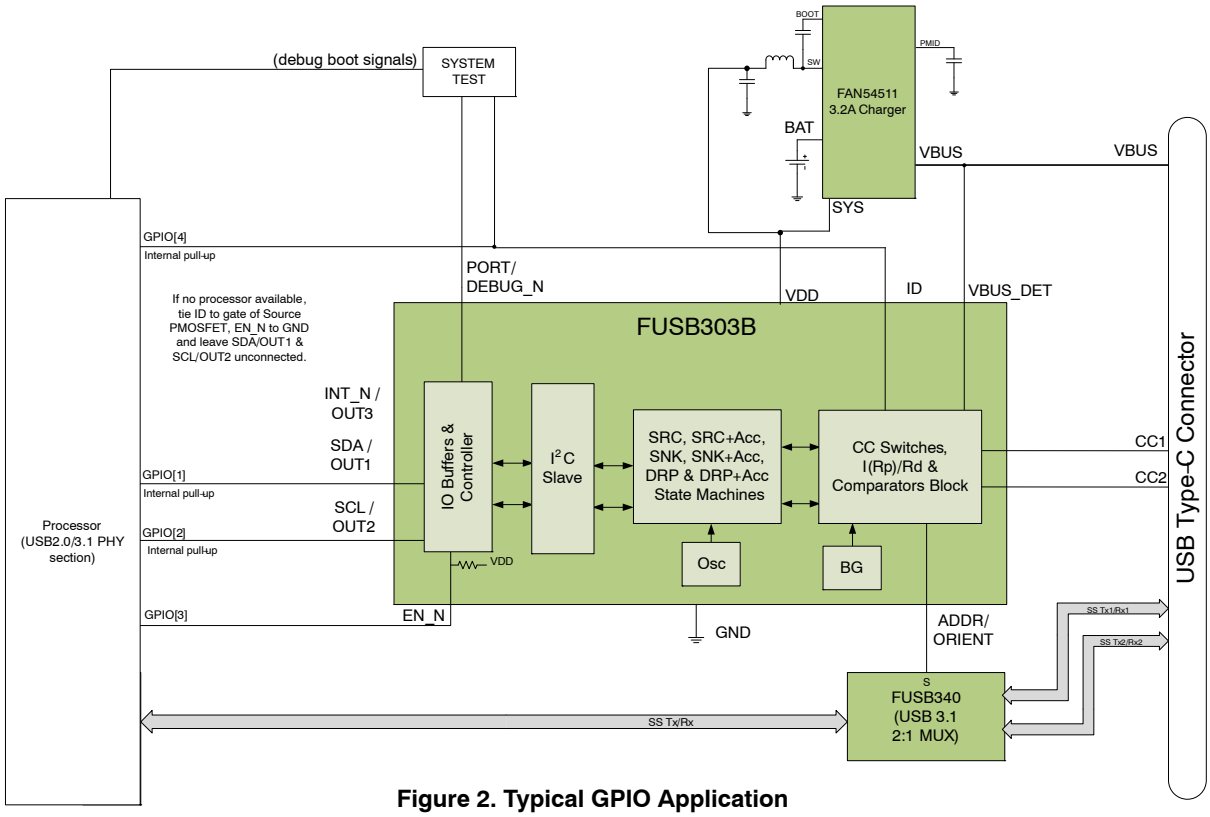


Figure 2. Typical GPIO Application

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BLOCK DIAGRAM

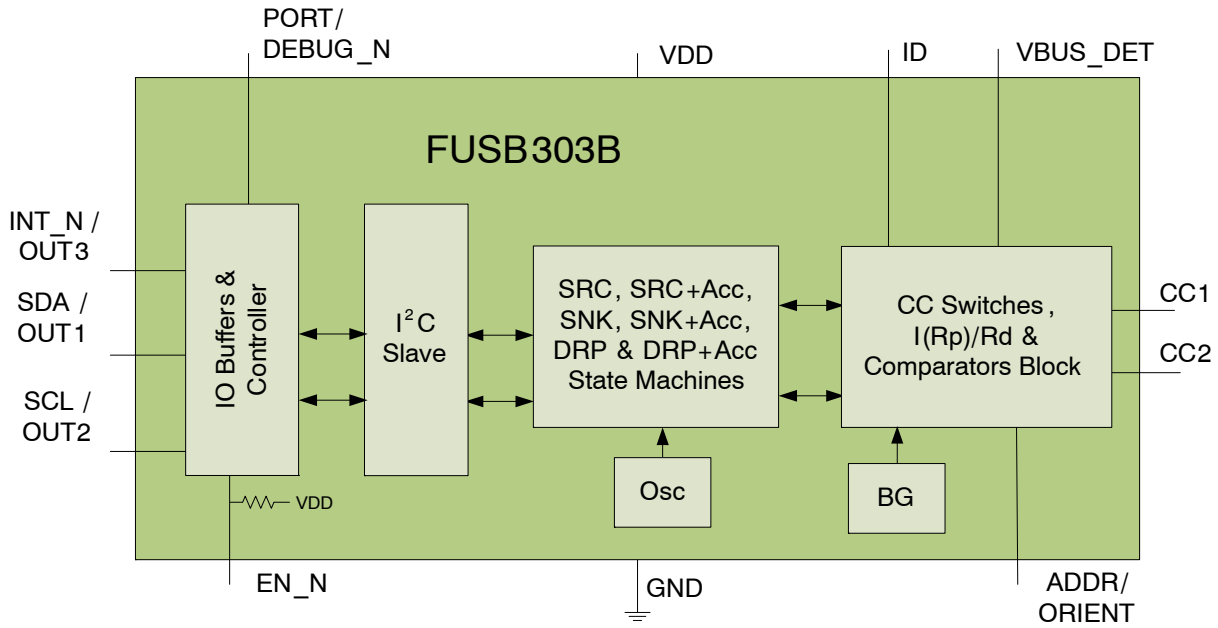


Figure 3. FUSB303B Block Diagram

PIN CONFIGURATION

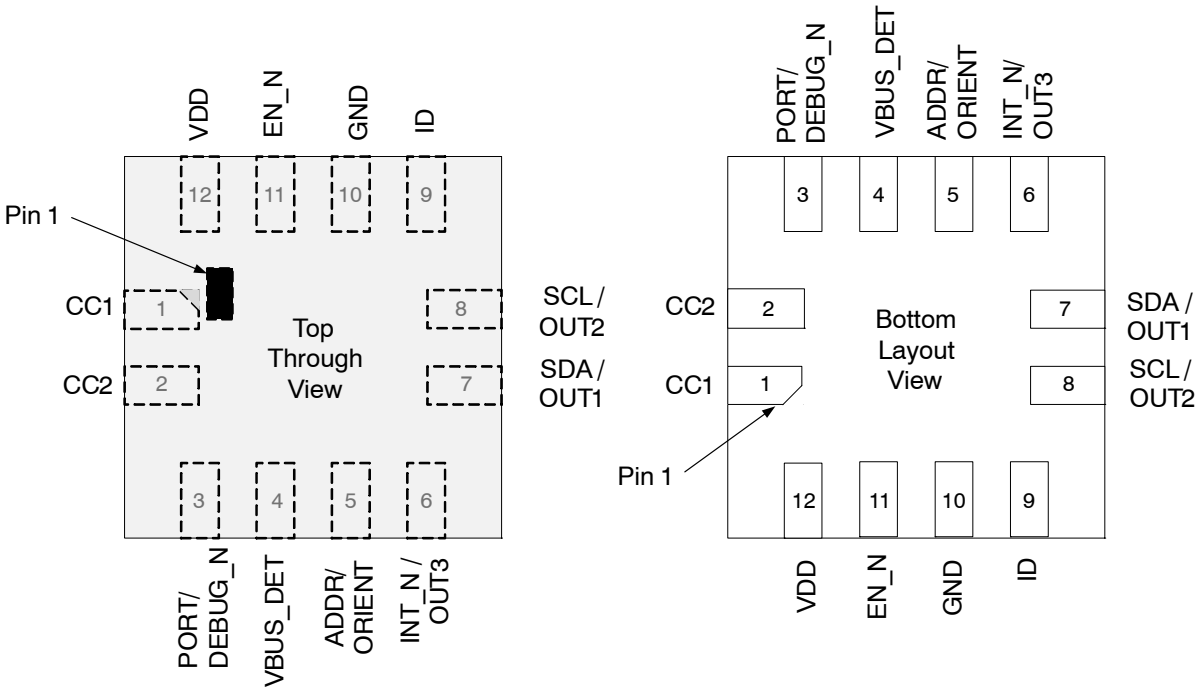


Figure 4. FUSB303B Pin Assignment (Top Through and Bottom Views)

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PIN DESCRIPTIONS

Table 1. PIN DESCRIPTIONS

<table>
<tr><th>Pin #</th><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">USB TYPE−C CONNECTOR INTERFACE</td></tr>
<tr><td>1, 2</td><td>CC1, CC2</td><td>I/O</td><td>Type−C Configuration Channel pins used for USB−C receptacles</td></tr>
<tr><td>4</td><td>VBUS_DET</td><td>Input</td><td>VBUS input pin for attach and detach detection</td></tr>
<tr><td colspan="4">POWER AND GROUND</td></tr>
<tr><td>10</td><td>GND</td><td>Ground</td><td>Ground</td></tr>
<tr><td>12</td><td>VDD</td><td>Power</td><td>Input Supply Voltage</td></tr>
<tr><td colspan="4">I²C SIGNAL INTERFACE</td></tr>
<tr><td>6</td><td>INT_N/OUT3</td><td>Open−Drain Output</td><td>INT_N/OUT3 is a dual function pin. When in I²C mode (see ADDR/ORIENT pin), it is the active LOW open drain interrupt output used to prompt the processor to read the I²C register bits.
When the device is in GPIO mode (see ADDR/ORIENT pin), this pin is OUT3, an open drain output
LOW = Audio Accessory detected
HIGH−Z = Audio Accessory not detected</td></tr>
<tr><td>7</td><td>SDA/OUT1</td><td>Open Drain I/O</td><td rowspan="2">SDA/OUT1 and SCL/OUT2 are dual function pins. When in I²C mode (see ADDR/ORIENT pin), SDA/OUT1 is the SDA data signal and SCL/OUT2 is the SCL clock signal of the I²C interface.
When the device is in GPIO mode (see ADDR/ORIENT pin), these pins are OUT1 and OUT2 inputs (I) or outputs (O) are shown below:
<table>
<tr><th>ID pin</th><th>OUT1 (I/O)</th><th>OUT2 (I/O)</th><th>Functionality</th></tr>
<tr><td>HIGH−Z</td><td>HIGH−Z (O)</td><td>LOW (O)</td><td>No Device Attached</td></tr>
<tr><td>HIGH−Z</td><td>HIGH−Z (O)</td><td>HIGH−Z (O)</td><td>Sink with Default Current</td></tr>
<tr><td>HIGH−Z</td><td>LOW (O)</td><td>HIGH−Z (O)</td><td>Sink with 1.5 A Current</td></tr>
<tr><td>HIGH−Z</td><td>LOW (O)</td><td>LOW (O)</td><td>Sink with 3 A Current</td></tr>
<tr><td>LOW</td><td>HIGH (I)</td><td>HIGH (I)</td><td>Source with Default Current</td></tr>
<tr><td>LOW</td><td>LOW (I)</td><td>HIGH (I)</td><td>Source with 1.5 A Current</td></tr>
<tr><td>LOW</td><td>LOW (I)</td><td>LOW (I)</td><td>Source with 3 A Current</td></tr>
<tr><td>LOW</td><td>HIGH (I)</td><td>LOW (I)</td><td>Reserved (Do Not Use)</td></tr>
</table></td></tr>
<tr><td>8</td><td>SCL/OUT2</td><td>Open Drain I/O</td></tr>
<tr><td colspan="4">GPIO PIN INTERFACE</td></tr>
<tr><td>3</td><td>PORT/ DEBUG_N</td><td>Input then Push/Pull Output</td><td>PORT/DEBUG_N is a dual function pin: 3 state input to set the port role. On the falling edge of EN_N and when VDD is active or during power up when EN_N is LOW, the state of this pin is sampled. This pin is also sampled on a SW_RES soft reset via I²C.
HIGH = FUSB303B as a Source Only port
Float = FUSB303B as a Dual Role Port (DRP)
LOW = FUSB303B as a Sink Only port
Note: a 900 kΩ resistor should be used when connecting to VDD or GND to reduce standby current.
Subsequently, this pin is the DEBUG_N push−pull output
LOW = Debug Accessory detected
HIGH = Debug Accessory not detected</td></tr>
<tr><td>5</td><td>ADDR/ ORIENT</td><td>Input then Push/Pull Output</td><td>ADDR/ORIENT is a dual function pin: 3 state input to set to I²C mode and the I²C address or for GPIO mode. On the falling edge of EN_N and when VDD is active or during power up when EN_N is LOW, the state of this pin is sampled. This pin is also sampled on a SW_RES soft reset via I²C.
HIGH = I²C mode with address 62h
Float = GPIO mode
LOW = I²C mode with address 42h
Note: a 900 kΩ resistor should be used when connecting to VDD or GND to reduce standby current.
Subsequently, this pin is the ORIENT push−pull output
LOW = CC is CC1 or A5 of the USB−C receptacle
HIGH = CC is CC2 or B5 of the USB−C receptacle</td></tr>
<tr><td>9</td><td>ID</td><td>Open−Drain Output</td><td>Open drain output that indicate FUSB303B’s detection state as a Source or Sink
LOW = FUSB303B attached as a Source
HIGH−Z = FUSB303B attached as a Sink</td></tr>
<tr><td>11</td><td>EN_N</td><td>Input</td><td>Active LOW device enable input (has internal pull up resistor)
Note: CONTROL1.ENABLE must be asserted if I²C mode is selected.</td></tr>
</table>

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Table 2. ORIENT PIN VERSUS ORIENT [1:0] REGISTER BITS MAPPING

CC1 (A5)	CC2 (B5)	STATUS. ORIENT[1] Bit	STATUS. ORIENT[0] Bit	ADDR/ORIENT pin Output
FUSB303B CONNECTED AS A SINK				
SNK. Open	SNK. Open	0	0	LOW
SNK. Open	SNK. Rp	1	0	HIGH
SNK. Rp	SNK. Open	0	1	LOW
SNK. Rp (Note 2)	SNK. Rp	0	1	LOW
SNK. Rp	SNK. Rp (Note 2)	1	0	HIGH
FUSB303B CONNECTED AS SOURCE				
SRC. Open	SRC. Open	0	0	LOW
SRC. Open or SRC. Ra	SRC. Rd	1	0	HIGH
SRC. Rd	SRC. Open or SRC. Ra	0	1	LOW
SRC. Rd (Note 1)	SRC.Rd	0	1	LOW
SRC. Rd	SRC. Rd (Note 1)	1	0	HIGH

1. Orientation decoded on this pin after a Sink Debug Test System (DTS) attached to FUSB303B.
2. Orientation decoded on this pin after a Source Debug Test System (DTS) attached to FUSB303B.

High Voltage Tolerance on CCx and VBUS Pins

The FUSB303B has additional protection for the type C connector pins where it can tolerate up to 28 V on VBUS, CC1 and CC2 to protect against any misbehaving Type C device connect to the FUSB303B. If VBUS tolerance is needed higher than 28 V, a 900 kΩ resistor can be used externally along with a Transient Voltage Suppressor (TVS) to achieve almost any higher voltage tolerance dictated by the TVS chosen.

Dead Battery

If power is not applied to FUSB303B and it is attached to a Source device, then the Source would pull up the CC line connected through the cable. The FUSB303B in response will turn on the pull−down that will bring the CC voltage to a range that the Source can detect an attached device and turn on VBUS.

GPIO Mode, Debug and Audio Accessories

When VDD is active and on the trailing edge of EN_N, the FUSB303B will sample PORT/DEBUG_N to determine if the FUSB303B operates as a Source (HIGH), Sink (LOW) or DRP (floating). Subsequently the PORT/DEBUG_N will be set LOW when a Debug Test System is detected.

If the FUSB303B is configured as a Sink (PORT/DEBUG_N = LOW upon enable), the FUSB303B will detect a Debug Test System if Rp is detected on both CC1 and CC2. Devices that support orientation detection will also have ADDR/ORIENT set based on the levels detected for CC1 and CC2. ID will be set HIGH−Z.

If the device is configured as a Source (PORT/DEBUG_N = HIGH upon enable), the FUSB303B will detect a Debug Test System if Rd is detected on both CC1 and CC2. Devices that support orientation detection will also have ADDR/ORIENT set based on the levels detected for CC1 and CC2. ID will be set LOW.

The FUSB303B also supports DRP toggling for detecting debug test systems. When PORT/DEBUG_N= float upon enable, the FUSB303B can detect both Source and Sink debug test systems depending on how it resolves its role as a Source or Sink. Then it acts either as a Source or Sink as described above.

The FUSB303B will report Debug Test System detection via the Type I^2C register as well. The detection is the same as described above except Source, Sink and DRP roles are configured via the Portrole register. This Portrole register setting has higher priority over the PORT/DEBUG_N pin state for Source/Sink/DRP port role.

The FUSB303B will set INT_N/OUT3 = LOW in GPIO mode when an Audio Accessory is detected. The FUSB303B will report Audio Accessory detection via the Type I^2C register as well when Audio Accessory detection is configured via the Portrole register.

FORCE.SNK and FORCE.SRC Functionality

In some cases, a device may need to force its role to a Sink or a Source especially if two DRP devices are connected together and they have connected in the wrong device role. In that case, the FUSB303B has incorporated a function that allows it to be forced into either Sink or Source. However, if it cannot complete this role change, the FUSB303B will resume its previous role and flag success or failure with I_FRC_SUCC and I_FRC_FAIL interrupts respectively.

Remedial Actions

In some cases, a device may start to detect a Source or Sink but get caught in a loop trying to resolve the detected device. In that case the FUSB303B provides functionality to resolve

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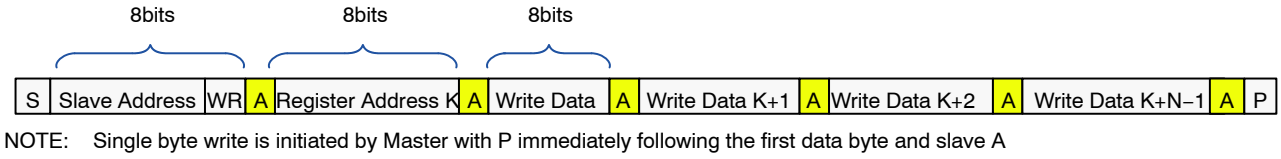
to a stable attached state. This functionality can be turned on and off via the REMEDY_EN and DCABLE_EN bits. Multiple cases are tried and some of the register settings will be changed to try to achieve stable attach. The I_REMEDY interrupt will allow the processor to know that this functionality has been triggered.

AUTOSNK Mode

When the FUSB303B is powered directly from VBAT the AUTO_SNK_EN mode can be used to prevent the application from attaching as a Source when the battery is weak or disconnect and attach as a Sink. With AUTO_SNK_EN enabled the port will attempt to configure as a Sink when attached to another DRP. If connected to another Sink, the port will detach. The threshold at which AUTOSNK can be triggered can be programmed via the AUTO_SNK_TH bits. The I_AUTOSNK interrupt is triggered whenever this functionality is invoked.

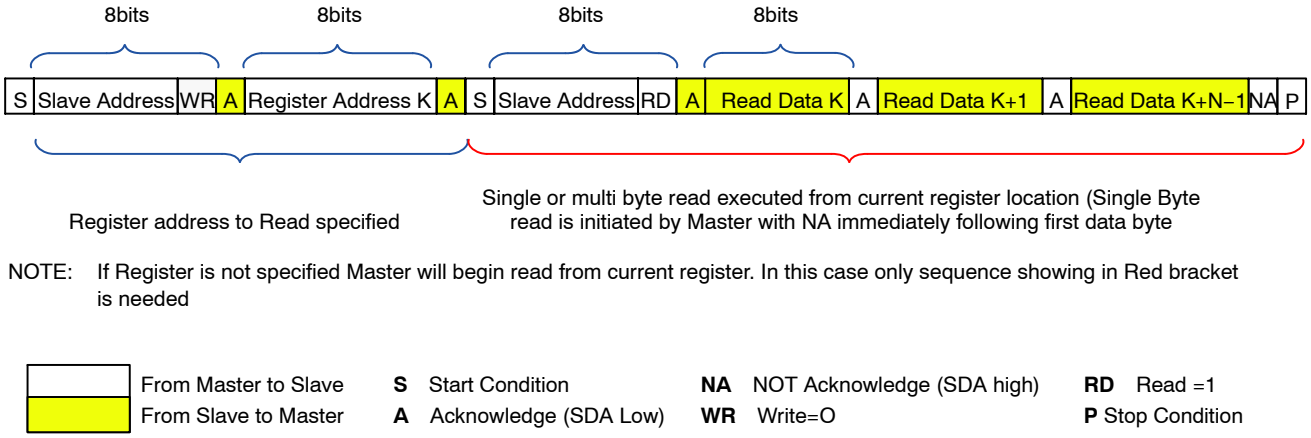
Power Up, Initialization and Reset, Interrupt Operation, I²C Interface

The FUSB303B includes a full I²C slave controller. The I²C slave fully complies with the I²C specification version 6 requirements. This block is designed for fast mode. Examples of an I²C write and read sequence are shown Figure 5 and Figure 6 respectively.



NOTE: Single byte write is initiated by Master with P immediately following the first data byte and slave A

Figure 5. I²C Write Example



NOTE: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed

Figure 6. I²C Write Example

When power is first applied, the FUSB303B will power up in the configuration set by the PORT/DEBUG_N input with Audio Accessory Support enabled and all interrupts masked. If the ADDR/ORIENT input is HIGH or LOW (I²C mode) the local processor can then re−configure the FUSB303B to the desired mode and clear the global interrupt mask bit, INT_MASK using the I²C interface. To enable device function in I²C mode, the register bit ENABLE in CONTROL1 must also be asserted. The INT_N/OUT3 pin is an active LOW, open drain output. This pin indicates to the host processor that an interrupt has occurred in the FUSB303B which needs attention. The INT_N/OUT3 pin is in a high impedance state by default after power−up or device reset, and the global interrupt mask (INT_MASK in Control register) is set. After INT_MASK bit is cleared by the local processor, the INT_N/OUT3 pin stays high impedance in preparation of future interrupts. When an interruptible event occurs, INT_N/OUT3 is driven LOW and is in a high impedance state again when the processor clears the interrupt by writing a one in the position of the interrupt bit that was set. Subsequent to the initial power up or reset; if the processor writes a “1” to global interrupt mask bit when the system is already powered up, the INT_N/OUT3 pin stays in a high impedance state and ignores all interrupts until the global interrupt mask bit is cleared. If an event happens that would ordinarily cause an interrupt when the global interrupt mask bit is set, the INT_N/OUT3 pin goes LOW when the global interrupt mask is cleared.

Interrupt bits hold their value and to clear a specific interrupt, a “1” needs to be written to that interrupt bit.

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I²C Address

The ADDR/ORIENT bit HIGH or LOW is indicated in bit 5 of the slave address shown in Table 3.

Table 3. FUSB303B I²C SLAVE ADDRESS

Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave Address	8	0	1	ADDR/ORIENT state	0	0	0	1	R/W

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter			Min.	Max.	Unit
V_{VDD}	Supply Voltage from V_{DD}			−0.5	6.0	V
V_{CON}	ID, VBUS_DET, CC1 and CC2 voltage			−0.5	28.0	V
V_{IO}	EN_N, PORT/DEBUG_N, ADDR/ORIENT, INT_N/OUT3, SDA/OUT1, SCL/OUT2 pins voltage			−0.5	6.0	V
$T_{STORAGE}$	Storage Temperature Range			−65	+150	C
T_J	Maximum Junction Temperature				+150	C
T_L	Lead Temperature (Soldering, 10 seconds)				+260	C
ESD	IEC 61000−4−2 System ESD with external TVS	Connector Pins (VBUS, CC1 & CC2)	Air Gap	15		kV
			Contact	8		
	Human Body Model, JEDEC JESD22−A114	Connector Pins (VBUS_DET, CC1 and CC2)		4		kV
		Others		2		
	Charged Device Model, JEDEC LESD22−C101	All Pins		1		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 5. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{BUS}	VBUS_DET Voltage	4.0	5.0	22	V
V_{DD}	Supply Voltage	2.85	3.3	5.5	V
T_A	Operating Temperature	−40		+85	C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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Table 6. DC AND TRANSIENT CHARACTERISTICS

(Unless otherwise specified: Recommended T_A and T_J temperature ranges. All typical values are at T_A = 25°C and V_{DD} = 3.3 V unless otherwise specified.)

Symbol	Parameter	T_A = −40 to +85°C, T_J=−40 to +125°C			Unit
		Min.	Typ.	Max	
TYPE C SPECIFIC PARAMETERS					
I_{80_CCX}	Source 80 μA CC Current (Default) HOST_CUR1 = 0, HOST_CUR0 = 1 or via GPIO mode	64	80	96	μA
I_{180_CCX}	Source 180 μA CC Current (1.5 A) HOST_CUR1 = 1, HOST_CUR0 = 0 or via GPIO mode	166	180	194	μA
I_{330_CCX}	Source 330 μA CC Current (3 A) HOST_CUR1 = 1, HOST_CUR0 = 1 or via GPIO mode (Note 3)	304	330	356	μA
V_{SNKDB}	Sink Pull−Down Voltage in Dead Battery Under all Pull−up Source Loads			2.18	V
Rd	Sink Pull−Down Resistance when VDD is within Operating Range	4.6	5.1	5.6	kΩ
zOPEN	CC Resistance for Disabled State	126			kΩ
vRa−SRCdef	Ra Detection Threshold for CC Pin for Source for Default Current on VBUS (HOST_CUR1/0 = 01) or via GPIO mode	0.15	0.20	0.25	V
vRa−SRC1.5A	Ra Detection Threshold for CC Pin for Source for 1.5 A Current on VBUS (HOST_CUR1/0 = 10) or via GPIO mode	0.35	0.40	0.45	V
vRa−SRC3A	Ra Detection Threshold for CC Pin for Source for 3 A Current on VBUS (HOST_CUR1/0 = 11) or via GPIO mode	0.75	0.80	0.85	V
vRd−SRCdef	Rd Detection Threshold for Source for Default Current (HOST_CUR1/0 = 01) or via GPIO mode	1.50	1.60	1.65	V
vRd−SRC1.5A	Rd Detection Threshold for Source for 1.5 A Current (HOST_CUR1/0 = 10) or via GPIO mode	1.50	1.60	1.65	V
vRd−SRC3A	Rd Detection Threshold for Source for 3 A Current (HOST_CUR1/0 = 11) or via GPIO mode (Note 3)	2.45	2.60	2.75	V
vRa−SNK	Ra Detection Threshold for CC Pin for Sink	0.15	0.20	0.25	V
vRd−def	Rd Default Current Detection Threshold for Sink	0.61	0.66	0.70	V
vRd−1.5A	Rd 1.5 A Current Detection Threshold for Sink	1.16	1.23	1.31	V
vRd−3.0A	Rd 3 A Current Detection Threshold for Sink	2.04	2.11	2.18	V
vVBUSthr	VBUS_DET Threshold when VBUSOK is deasserted	2.9	3.3	3.67	V
tVBUSdeb	VBUS_DET debounce time before VBUSOK is deasserted only (see tDeb below for VBUSOK being asserted)	10		20	ms
vVBthLH	VBUS_DET Threshold when VBUSOK is asserted	3.67	4.07	4.48	V
tDeb	VBUS_DET debounce time before VBUSOK is asserted	250		500	μs
vVSAFEthr	vSafe0V VBUS_DET Threshold			0.8	V
vVSAFEthrhys	VSAFE0V VBUS_DET Threshold hysteresis		50		mV
rVBUSleak	Leakage between VBUS and GND when VBUS not sourced	72.4			kΩ
rVBUSdschg	Effective resistance from VBUS and GND when VBUS is being discharged from vSafe5V V_{DD} (V) = 2.85 to 5.5			2	kΩ
rPullup	Pull up resistor to VDD value on EN_N pin V_{DD} (V) = 2.85 to 5.5		6		MΩ
vAUTOSNKthr	Weak Battery VDD Threshold	−3%	AUTO SNK_TH	+3%	V
Ra	Resistor for discharging VCONN V_{DD} (V) = 2.85 to 5.5		1		kΩ

3. VDD = 3 V when 3 A current advertised.

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Table 7. CURRENT CONSUMPTION

Symbol	Parameter	VDD (V)	Conditions	TA = −40 to +85°C TJ=−40 to +125°C			Unit
				Min.	Typ.	Max.	
Idisable	Disabled Current	2.85 to 4.35	Disabled State EN N = HIGH or not connected			5	μA
Istby	Unattached Sink (3.3 V I²C mode without AUTOSNK or accessories)	2.85 to 4.35	Nothing attached		5	10	μA
	Unattached DRP or Source (3.3 V I²C mode without AUTOSNK or accessories)		Nothing attached, Internally Toggling		10	15	μA
Iattach	Attached Source or Sink (3.3 V I²C mode without AUTOSNK or accessories. Not including Ixxx_CCX current)	2.85 to 4.35	Attached as a Sink or Source		10	15	μA

Table 8. TIMING PARAMETERS

Symbol	Parameter		T_A = −40 to +85°C T_J=−40 to +125°C			Unit
			Min.	Typ.	Max.	Unit
tCCDebounce	Debounce Time for CC Attach Detection (TCCDEB[2:0] = 011)		−33%	TCCDEB	+33%	ms
tPDDebounce	Time a Sink port shall wait before it can determine it is detached		10	15	20	ms
tTryCCDebounce	Time a port shall wait before it can determine it is re−attached during the try−wait process		10		20	ms
tRpValueChange	Time a Sink port shall wait before it can determine there has been a change in Rp		10		20	ms
tSRCDisconnect	Time a Source shall detect the SRC.Open state		10		20	ms
tErrorRecovery	Time staying in the ErrorRecovery State if sent there via the ERROR_REC bit or by a change of port roles		25	50	100	ms
tDRPTry	Time staying in the Try.SRC/SNK prior to transition to TryWait.SRC/SNK State		75		150	ms
tTryTimeout	Time to discharge VBUS before giving up for cases where VBUS is always on.		550		1100	ms
tDRP	Sum of tDRPTogSNK and tDRPTogSRC		−33%	T_DRP	+33%	ms
tDRPTransition	Time DRP shall complete transitions between Source and Sink roles		0		1	ms
tDRPTogSNK	For DRP Operation, Time Spent in Unattached.SNK before going to Unattached.SRC State	DRPTOGGLE = 00 (Note 4)		70		%
		DRPTOGGLE = 01		60		%
		DRPTOGGLE = 10		50		%
		DRPTOGGLE = 11		40		%
tDRPTogSRC	For DRP Operation, Time Spent in Unattached.SRC before going to Unattached.SNK State	DRPTOGGLE = 00 (Note 4)		30		%
		DRPTOGGLE = 01		40		%
		DRPTOGGLE = 10		50		%
		DRPTOGGLE = 11		60		%
tEN	Time from EN_N LOW and VDD active to I²C access available	2.85 to 5.5			100	ms

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Table 9. TIMING PARAMETERS (continued)

Symbol	Parameter		T_A = −40 to +85°C, T_J=−40 to +125°C Min.	Typ.	Max.	Unit
tRESET	Soft Reset Duration	2.85 to 5.5			100	ms
tAUTOSNK	Debounce time to detect Weak Battery VDD Threshold to trigger I_AUTOSNK if AUTOSNK mode enabled for both entering AUTOSNK and exiting AUTOSNK V_{DD} (V) = 2.85 to 5.5		10	15	20	ms

4. Default Value when Configured in GPIO Mode (ADDR/ORIENT = Float)

Table 9. IO SPECIFICATIONS

Symbol	Parameter	V_{DD} (V)	Conditions	T_A = −40 to +85°C, T_J=−40 to +125°C Min.	Typ.	Max.	Unit
OPEN DRAIN OUTPUT PINS (ID, INT_N/OUT3)							
V_{OLID}	Output Low Voltage	2.85 to 5.5	I_{OL} = 4 mA			0.4	V
INPUT PIN (EN_N)							
V_{ILEN}	Low−Level Input Voltage	2.85 to 5.5				0.4	V
V_{IHEN}	High−Level Input Voltage	2.85 to 5.5		1.2			V
I_{CCTEN}	VDD Current when EN_N is HIGH	2.85 to 5.5	Worst Input Voltage			2	μA
3−STATE INPUT AND PUSH/PULL OUTPUT PINS (PORT/DEBUG_N, ADDR/ORIENT)							
V_{ILADDR}	Low−Level Input Voltage	2.85 to 5.5				$0.2V_{DD}$	V
V_{IMADDR}	Middle−Level Input Voltage	2.85 to 5.5		$0.4V_{DD}$		$0.6V_{DD}$	V
V_{IHADDR}	High−Level Input Voltage	2.85 to 5.5		$0.8V_{DD}$			V
Zfloat	Impedance to VDD or GND detected as a FLOAT including when VDD = 0	2.85 to 5.5		1		4	MΩ
V_{OLOUT}	Low−Level Input Voltage	2.85 to 5.5	I_{OL} = 1 mA			$0.2V_{DD}$	V
V_{OHOUT}	High−Level Input Voltage	2.85 to 5.5	I_{OL} = −1 mA	$0.8V_{DD}$			V
I^2C INTERFACE PINS – FAST MODE SDA/OUT1, SCL/OUT2							
V_{ILI2C}	Low−Level Input Voltage	2.85 to 5.5				0.4	V
V_{IHI2C}	High−Level Input Voltage	2.85 to 5.5		1.2			V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	2.85 to 5.5		0.2			V
I_{i2C}	Input Current of SDA/OUT1and SCL/OUT2 Pins,	2.85 to 5.5	Input Voltage 0 V to 3.6 V			2	μA
I_{CCTI2C}	VDD Current when SDA/OUT1or SCL/OUT2 is HIGH	2.85 to 5.5	Worst Input Voltage			2	μA
V_{OLSDA}	Low−Level Output Voltage at 2 mA Sink Current (Open−Drain)	2.85 to 5.5	I_{OL} = 2 mA			0.3	V
I_{OLSDA}	Low−Level Output Current (Open−Drain)	3.0 to 5.5	V_{OLSDA} = 0.4 V	20			mA
C_I	Capacitance for Each I/O Pin	2.85 to 5.5			5		pF

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Table 10. FAST MODE I²C TIMING SPECIFICATIONS (see Figure 7)

Symbol	Parameter	Fast Mode		
		Min.	Max.	Unit
f_{SCL}	SCL/OUT2 Clock Frequency		400	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.6		μs
t_{LOW}	Low Period of SCL/OUT2 Clock	1.3		μs
t_{HIGH}	High Period of SCL/OUT2 Clock	0.6		μs
$t_{SU;STA}$	Set−up Time for Repeated START Condition	0.6		μs
$t_{HD;DAT}$	Data Hold Time		0.9	μs
$t_{SU;DAT}$	Data Set−up Time (Note 5)	100		ns
t_r	Rise Time of SDA/OUT1 and SCL/OUT2 Signals (Note 6)	20×(V_{DD}/5.5 V)	250	ns
t_f	Fall Time of SDA/OUT1 and SCL/OUT2 Signals (Note 6)	20×(V_{DD}/5.5 V)	250	ns
$t_{SU;STO}$	Set−up Time for STOP Condition	0.6		μs
t_{BUF}	Bus−Free Time between STOP and START Conditions	1.3		μs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter		50	ns

5. A fast−mode I²C−bus device can be used in a standard−mode I²C−bus system, but the requirement $t_{SU;DAT}$ ⍁ 250 ns must be met. This is automatically the case if the device does not stretch the LOW period of the SCL/OUT2 signal. If such a device does stretch the LOW period of the SCL/OUT2 signal, it must output the next data bit to the I²C_ line tr_max + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard−mode I²C bus specification) before the SCL/OUT2 line is released
6. Cb equals the total capacitance of one bus line in pF. If mixed with high−speed devices, faster fall times are allowed according to the I²C specification

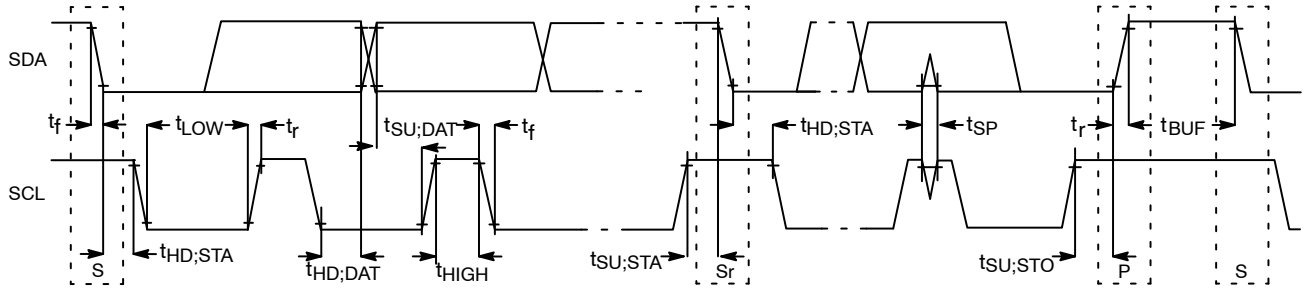


Figure 7. Definition of Timing for Full/Speed Mode Devices on the I²C Bus

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REGISTER DEFINITIONS

Table 11. REGISTER MAP

Address	Register Name	Type	Default	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	Reserved	N/A	N/A	Do Not Use							
01h	Device ID	R	10h	VER_ID[3:0]				REV_ID[3:0]			
02h	Device Type	R	03h	DEVICE_TYPE[7:0]							
03h	Portrole	R/W	4nh (see below)		ORIENTDEB	TRY[1:0]		AUDIOACC	DRP	SNK	SRC
04h	Control	R/W	43h	T_DRP		DRPTOGGLE[1:0]		DCABLE_EN	HOST_CUR[1:0]		INT_MASK
05h	Control1	R/W	23h	REMEDY_EN	AUTO_SNK_TH[1:0]		AUTO_SNK_EN	ENABLE	TCCDEB[2:0]		
06h-08h	Reserved	N/A	N/A	Do Not Use							
09h	Manual	W/C & R/W	00h			FORCE_SRC	FORCE_SNK	UNATT_SNK	UNATT_SRC	DISABLED	ERROR_REC
0Ah	Reset	W/C	00h								SW_RES
0Bh-0Dh	Reserved	N/A	N/A	Do Not Use							
0Eh	Mask	R/W	00h		M_ORIENT	M_FAULT	M_VBUS_CHG	M_AUTOSNK	M_BC_LVL	M_DETACH	M_ATTACH
0Fh	Mask1	R/W	00h		M_REM_VBOFF	M_REM_VBON		M_REM_FAIL	M_FRC_FAIL	M_FRC_SUCC	M_REMEDY
10h	Reserved	N/A	N/A	Do Not Use							
11h	Status	R	40h	AUTOSNK	VSAFE0V	ORIENT[1:0]		VBUSOK	BC_LVL[1:0]		ATTACH
12h	Status1	R	00h							FAULT	REMEDY
13h	Type	R	00h		DEBUGSRC	DEBUGSNK	SINK	SOURCE	ACTIVECABLE	AUDIOVBUS	AUDIO
14h	Interrupt	R/W1C	00h		I_ORIENT	I_FAULT	I_VBUS_CHG	I_AUTOSNK	I_BC_LVL	I_DETACH	I_ATTACH
15h	Interrupt1	R/W1C	00h		I_REM_VBOFF	I_REM_VBON		I_REM_FAIL	I_FRC_FAIL	I_FRC_SUCC	I_REMEDY
16h-1Fh	Reserved	N/A	N/A	Do Not Use							

7. Do not use registers that are blank
8. Values read from undefined register bits are not defined and invalid. Do not write to undefined registers

Table 12. DEVICE ID (Address: 01h, Reset Value: 0001_0000b, Type: Read Only)

Bit #	Name	Size (Bits)	Bit#: Default	Description
7:4	VER_ID	4	7:4 01h	Device version ID by Trim, etc. A_[REV_ID]: 0001 (FUSB303B A)
3:0	REV_ID	4	3:0 00h	Revision History of each version [VER_ID]_revA: 0000

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Table 13. DEVICE TYPE (Address: 02h, Type: Read Only)

Bit #	Name	Size (Bits)	Bit#: Default	Description
7:0	DEVICE_TYPE[7:0]	8	7:0 03h	03h: FUSB303B

Table 14. PORTROLE (See Note 9)
(Address: 03h, Reset Value: 0100_1nnnb (Reset value for bits nnn will be set by the state of the PORT/DEBUG_N pin either during power up when EN_N is LOW or when Vdd is valid and EN_N goes HIGH to LOW) or when SW_RES is set HIGH. In dead battery mode, nnn = 010 or configured as SNK) Type: Read/Write)

Bit #	Name	Size (Bits)	Bit#: Default	Description
7	Reserved	1	7 0b	Do Not Use
6	ORIENTDEB	1	6 1b	1: When a Debug Accessory is found, continue to orientation detection if CC is on CC1 or CC2 (result is in Status.Orient[1:0])
5:4	TRY[1:0]	2	5:4 00b	00: Disable (normal DRP detection for DRPs) 01: Enable Try.SNK state machine detection for DRP only 10: Enable Try.SRC state machine detection for DRP only 11: Disable (cannot have Try.SNK and Try.SRC active together)
3	AUDIOACC	1	3 1b	1: Enable Audio Accessory Support (Debug Accessory support is always enabled)
2	DRP	1	2 n	1: Configure device as a Dual Role Port (see reset value text above)
1	SNK	1	1 n	1: Configure device as a Sink (see reset value text above)
0	SRC	1	0 n	1: Configure device as a Source (see reset value text above)

9. If DRP bit, SNK bit and SRC bit are all set to 1, then the priority of which Portrole the FUSB303B assumes is first priority is DRP, second priority is SNK and last priority is SRC. See Manual register note below for priority between Manual register bits and Portrole register.

Table 15. CONTROL
Address: 04h, Reset Value: 0100_0011b, Type: Read/Write

Bit #	Name	Size (Bits)	Bit#: Default	Description
7:6	T_DRP[:0]	2	7:6 01b	Sets the total period of the DRP toggle cycle (i.e. Unattached.SNK period + Unattached.SRC period): 00: 60 ms 01: 70 ms 10: 80 ms 11: 90 ms
5:4	DRPTOGGLE[1:0]	2	5:4 00b	Selects different timing for Dual Role Port Toggle between Unattached.SNK State and Unattached.SRC State. 00: 60% in Unattached.SNK and 40% in Unattached.SRC 01: 50% in Unattached.SNK and 50% in Unattached.SRC 10: 40% in Unattached.SNK and 60% in Unattached.SRC 11: 30% in Unattached.SNK and 70% in Unattached.SRC
3	DCABLE_EN	1	3 0b	1: Enable Dangling Cable internal methods to achieve a stable attach
2:1	HOST_CUR[1:0]	2	2:1 01b	Controls the pull−up current when device enabled as a Source 00: Reserved. Do not use. 01: 80 μA – Default USB Power 10: 180 μA – Medium Current Mode: 1.5 A 11: 330 μA – High Current Mode: 3 A
0	INT_MASK	1	1b	1: Global interrupt mask to mask all interrupts

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Table 16. CONTROL1
(Address: 05h, Reset Value: 0010_0011b, Type: Read/Write)

Bit #	Name	Size (Bits)	Bit#: Default	Description
7	REMEDY_EN	1	7 0b	1: Enable the Remedy detection to employ internal methods to achieve stable attach
6:5	AUTO_SNK_TH[1:0]	2	6:5 01b	Sets the weak battery VDD threshold voltage when AUTO_SNK_EN is enabled. 00: 3.0 V 01: 3.1 V 10: 3.2 V 11: 3.3 V
4	AUTO_SNK_EN	1	4 0b	1: Enable automatic Sink port role based on weak battery VDD threshold in bits AUTO_SNK_TH in Control register below
3	ENABLE	1	3 0b	1: Enable the FUSB303B if the external EN_N pin is LOW in I^2C mode (that is, not in GPIO mode)
2:0	TCCDEB[2:0]	3	2:0 011b	Controls debounce time for attaching a device 000: 120 ms 001: 130 ms 010: 140 ms 011: 150 ms 100: 160 ms 101: 170 ms 110: 180 ms 111: Reserved

Table 17. Manual (Note 10)
(Address: 09h, Reset Value: 0000_0000b, Type: Read/Write (see bits below: W/C = Write one self clearing, R/W = Read/Write and N/A = Not Applicable)

Bit #	Name	R/W/C	Size (Bits)	Bit#: Default	Description
7:6	Reserved	N/A	2	7:6 00b	Do Not Use
5	FORCE_SRC	W/C	1	5 0b	1: Forces the FUSB303B to behave as a Source
4	FORCE_SNK	W/C	1	4 0b	1: Forces the FUSB303B to behave as a Sink
3	UNATT_SNK	W/C	1	3 0b	1: Put device in Unattached.SNK State as defined in the Type C spec
2	UNATT_SRC	W/C	1	2 0b	1: Put device in Unattached.SRC state as defined in the Type C spec
1	DISABLED (Note 11)	R/W	1	1 0b	1: Put device in Disabled state as defined in the Type C spec
0	ERROR_REC	W/C	1	0 0b	1: Put device in ErrorRecovery state as defined in the Type C spec

10. If more than one bit is set to 1b simultaneously then an order of priority will be used. First priority is DISABLED, second is ERROR_REC, third is FORCE_SRC, fourth is FORCE_SNK, fifth is UNATT_SRC, last is UNATT_SNK. The highest priority bit will take precedence and all other bits will be cleared automatically.
11. The DISABLED bit must be manually cleared. Also DISABLED bit has a higher priority over Portrole register since the DISABLED bit has to be cleared in order to execute the new Portrole register settings. However, all other Manual register bits don't have a lot of meaning if the Portrole register is changed and so Portrole register setting should have higher priority than all bits except for DISABLED bit.

Table 18. RESET
(Address: 0Ah, Reset Value: 0000_0000b, Type: Write/Clear)

Bit #	Name	Size (Bits)	Bit#: Default	Description
7:1	Reserved	7	7:1 00h	Do Not Use
0	SW_RES	1	0 0b	1: Reset the FUSB303B and I^2C Registers

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Table 19. MASK

(Address: 0Eh, Reset Value: 0000_0000b, Type: Read/Write)

Bit #	Name	Size (Bits)	Bit#: Default	Description
7	Reserved	1	7 0b	Do Not Use
6	M_ORIENT	1	6 0b	1: Mask the I_ORIENT interrupt bit from asserting INT_N pin
5	M_FAULT	1	5 0b	1: Mask the I_FAULT interrupt bit from asserting INT_N pin
4	M_VBUS_CHG	1	4 0b	1: Mask the I_VBUS interrupt bit from asserting INT_N pin
3	M_AUTOSNK	1	3 0b	1: Mask the I_AUTOSNK interrupt bit from asserting INT_N pin
2	M_BC_LVL	1	2 0b	1: Mask the I_BC_LVL interrupt bit from asserting INT_N pin
1	M_DETACH	1	1 0b	1: Mask the I_DETACH interrupt bit from asserting INT_N pin
0	M_ATTACH	1	0 0b	1: Mask the I_ATTACH interrupt bit from asserting INT_N pin

12. Masking the interrupt just does not cause INT_N to be asserted. The interrupt bit will still be asserted in the Interrupt register and so that an all zeroes Interrupt register value is not needed for INT_N to be deasserted.

Table 20. MASK1

(Address: 0Fh, Reset Value: 0000_0000b, Type: Read/Write)

Bit #	Name	Size (Bits)	Bit#: Default	Description
7	Reserved	1	7 0b	Do Not Use
6	M_REM_VBOFF	1	6 0b	1: Mask the I_REM_VBOFF interrupt bit from asserting INT_N pin
5	M_REM_VBON	1	5 0b	1: Mask the I_REM_VBON interrupt bit from asserting INT_N pin
4	Reserved	1	4 0b	Do Not Use
3	M_REM_FAIL	1	3 0b	1: Mask the I_REM_FAIL interrupt bit from asserting INT_N pin
2	M_FRC_FAIL	1	2 0b	1: Mask the I_FRC_FAIL interrupt bit from asserting INT_N pin
1	M_FRC_SUCC	1	1 0b	1: Mask the I_FRC_SUCC interrupt bit from asserting INT_N pin
0	M_REMEDY	1	0 0b	1: Mask the I_REMEDY interrupt bit from asserting INT_N pin

13. Masking the interrupt just does not cause INT_N to be asserted. The interrupt bit will still be asserted in the Interrupt register and so that an all zeroes Interrupt register value is not needed for INT_N to be deasserted.

Table 21. STATUS

(Address: 11h, Reset Value: 0000_0000b, Type: Read Only)

Bit #	Name	Size (Bits)	Bit#: Default	Description
7	AUTOSNK	1	7 0b	1:AUTOSNK mode is activated since the VDD voltage is lower than AUTO_SNK_TH voltage
6	VSAFE0V	1	6 0b	1: Status to indicate VBUS_DET is below vSafe0V max of 0.8 Vpin
5:4	ORIENT[1:0]	2	5:4 00b	Status to indicate which CCx pins has the cable CC connection 00: No or unresolved connection detected 01: Cable CC is connected through the CC1 (A5) pin 10: Cable CC is connected through the CC2 (B5) pin 11: A fault has occurred during the detection
3	VBUSOK	1	3 0b	1: Status to indicate VBUS_DET is in the valid VBUS 5V range
2:1	BC_LVL[1:0]	2	2:1 00b	Thresholds that allow detection of current advertisement on CC line 00: (Ra or unattached) Sink or unattached Source 01: Rd threshold for Sink default current advertisement 10: Rd threshold for Sink 1.5 A current advertisement 11: Rd threshold for Sink 3 A current advertisement
0	ATTACH	1	0 0b	1: Attached to a device or accessory of a type shown in the Type register

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Table 22. STATUS1
(Address: 12h, Reset Value: 0000_0000b, Type: Read Only)

Bit #	Name	Size (Bits)	Bit#: Default	Description
7:2	Reserved	6	7:2 00h	Do Not Use
1	FAULT	1	1 0b	1: Status to indicate that as a Sink, CC has exceed the normal vRd voltage range
0	REMEDY	1	0 0b	1: Status to indicate that FUSB303B is employing internal methods to achieve a stable attach

Table 23. TYPE
(Address: 13h, Reset Value: 0000_0000b, Type: Read Only)

Bit #	Name	Size (Bits)	Bit#: Default	Description
7	Reserved	1	7 0b	Do Not Use
6	DEBUGSRC	1	6 0b	1: FUSB303B is attached as a Source Debug Accessory ([Unoriented/Oriented]DebugAccessory.SRC)
5	DEBUGSNK	1	5 0b	1: FUSB303B is attached as a Sink Debug Accessory (DebugAccessory.SNK)
4	SINK	1	4 0b	1: FUSB303B is attached as a Sink (Attached.SNK)
3	SOURCE	1	3 0b	1: FUSB303B is attached as a Source (Attached.SRC)
2	ACTIVECABLE	1	2 0b	1: FUSB303B is attached to an Active Cable (Ra detected)
1	AUDIOVBUS	1	1 0b	1: Indicates an Audio Accessory with VBUS has been detected (AudioAccessory with VBUS)
0	AUDIO	1	0 0b	1: Indicates an Audio Accessory without VBUS has been detected (AudioAccessory without VBUS)

Table 24. INTERRUPT
(Address: 14h, Reset Value: 0000_0000b, Type: Read/Write 1 to Clear)

Bit #	Name	Size (Bits)	Bit#: Default	Description
7	Reserved	1	7 0b	Do Not Use
6	I_ORIENT	1	6 0b	1: Interrupt flagged whenever ORIENT changes from 0,0 to 0,1 or 1,0 but not 1,1. Interrupt not flagged when ORIENT is cleared.
5	I_FAULT	1	5 0b	1: Interrupt flagged when CC1 or CC2 voltage exceeds normal Rd range when FUSB303B has Rd termination on CC1 and/or CC2
4	I_VBUS_CHG	1	4 0b	1: Interrupt flagged when VBUS has crossed vVBUSthr or vVBthLH thresholds
3	I_AUTOSNK	1	3 0b	1: Interrupt flagged when AUTOSNK mode has been activated or deactivated
2	I_BC_LVL	1	2 0b	1: Interrupt flagged when a change in BC_LVL[1:0] advertised current level has occurred
1	I_DETACH	1	1 0b	1: Interrupt flagged when a device or accessory has been detached
0	I_ATTACH	1	0 0b	1: Interrupt flagged when a device or accessory of type indicated in the Type register has been attached

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Table 25. INTERRUPT1

(Address: 15h, Reset Value: 0000_0000b, Type: Read/Write 1 to Clear)

Bit #	Name	Size (Bits)	Bit#: Default	Description
7	Reserved	1	7 0b	Do Not Use
6	I_REM_VBOFF	1	6 0b	1: Interrupt to request VBUS be turned off and discharged while executing internal methods to achieve stable attach
5	I_REM_VBON	1	5 0b	1: Interrupt to request VBUS be turned on while executing internal methods to achieve stable attach
4	Reserved	1	4 0b	Do Not Use
3	I_REM_FAIL	1	3 0b	1: Interrupt to indicate that internal methods to achieve stable attach have failed.
2	I_FRC_FAIL	1	2 0b	1: Interrupt to indicate that FORCE_SRC or FORCE_SNK has failed to execute either because it was being forced into a state it was already in or for other reasons
1	I_FRC_SUCC	1	1 0b	1: Interrupt to indicate that FORCE_SRC or FORCE_SNK has successfully being executed.
0	I_REMEDY	1	0 0b	1: Interrupt to indicate that detection issues caused FUSB303B to employ internal methods to achieve stable attach

ORDERING INFORMATION TABLE

Table 26. AVAILABLE PART NUMBERS

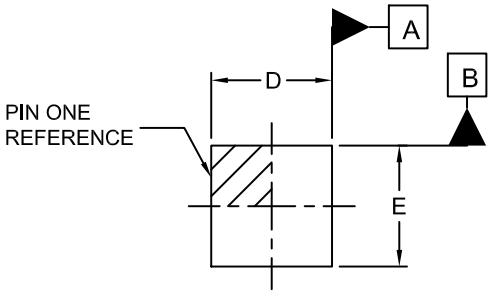
Part Number	Top Mark	Operating Temperature Range	Package	Packing Method†
FUSB303BTMX	UN	−40 to 85°C	12−Lead Ultra−thin Molded Leadless Package (QFN) 1.6 mm x 1.6 mm x 0.375 mm	Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

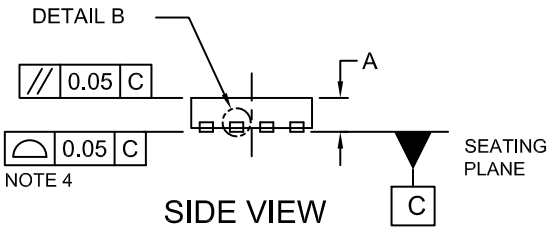
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X2QFN12 1.6x1.6, 0.4P
CASE 722AG
ISSUE A

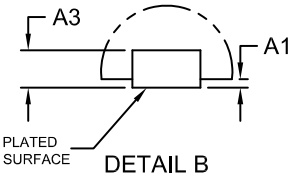
DATE 26 SEP 2017



TOP VIEW



SIDE VIEW

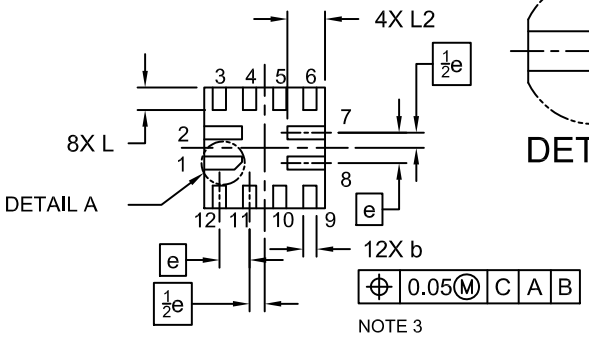


DETAIL B

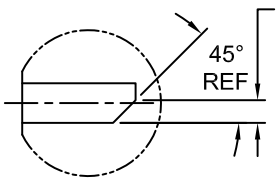
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINALS AND IS MEASURED BETWEEN 0.10 AND 0.20mm FROM THE TERMINAL TIP.
4. PROFILE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

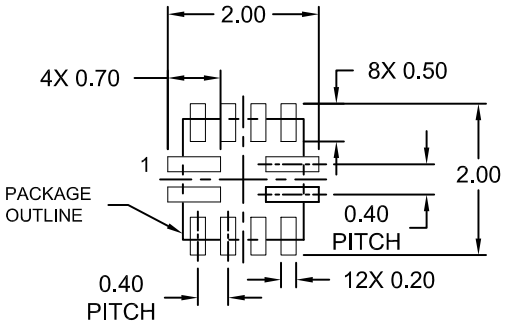
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.34	0.37	0.40
A1	---	---	0.05
A3		0.127 REF	
b	0.15	0.175	0.20
D	1.55	1.60	1.65
E	1.55	1.60	1.65
e		0.40 BSC	
L	0.25	0.30	0.35
L2	0.45	0.50	0.55



BOTTOM VIEW



DETAIL A



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