HD3SS212 5.4Gbps DisplayPort 1.2 2-to-1 Differential Switch

1 Features

- Compatible with DisplayPort 1.2 electrical standard
- 2:1 switching supporting data rates up to 5.4Gbps
- Supports HPD switching
- Wide -3dB differential BW of over 5.4 GHz
- Excellent dynamic characteristics (at 2.7GHz)
  - Crosstalk = –50dB
  - Isolation = –22dB
  - Insertion loss = –1.4dB
  - Return loss = –11 dB
  - Max bit-bit skew = 4 ps
- VDD operating range 3.3 V ±10%
- Small 5 mm x 5 mm x 1 mm, 48-ball nFBGA package
- Output enable (oe) pin disables switch to save power
- Power consumption
  - HD3SS212 <10mW (standby <30µW when OE = L)

2 Applications

- PC & notebooks
- Tablets
- Connected peripherals & printers

3 Description

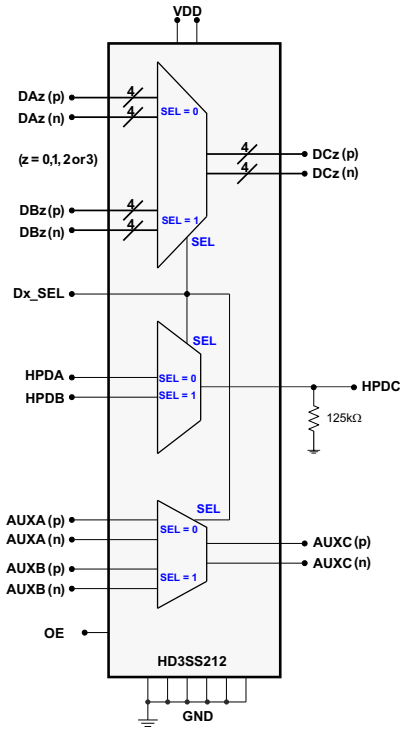
The HD3SS212 is a high-speed passive switch capable of switching two full DisplayPort 4 lane ports from one of two sources to one target location in an application. For DisplayPort applications that HD3SS212 also supports switching of the Auxiliary (AUX) and Hot Plug Detect (HPD) signals. HPD path is a buffer which requires a 125kΩ pull-down resistor on the HPDC line.

A typical application would be a mother board that includes two GPUs that need to drive one DisplayPort sink. The GPU is selected by the Dx_SEL pin. The HD3SS212 is offered in a 48-ball bfBGA package and specified to operate from a single supply voltage of 3.3V over full industrial temperature range of –40°C to 105°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
HD3SS212	nFBGA (48)	5.00 mm x 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Functional Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2016) to Revision D (December 2020) **Page**

- NOTE: The device in the MicroStar Jr. BGA packaging were redesigned using a laminate nFBGA package. This nFBGA package offers datasheet-equivalent electrical performance. It is also footprint equivalent to the MicroStar Jr. BGA. The new package designator in place of the discontinued package designator will be updated throughout the datasheet....1
- Changed u*jr BGA to nFBGA....1
- Changed u*jr ZQE to nFBGA ZXH. Updated thermal information....5
- Corrected typo from HD3SS3412 to HD3SS212....16

Changes from Revision B (January 2014) to Revision C (October 2016) **Page**

- Added Device Information table, ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. 1
- Deleted Ordering Information table. See POA at the end of the datasheet. 1

Changes from Revision A (March 2012) to Revision B (January 2014) **Page**

- Changed $\overline{OE}$ to OE throughout document....1

Changes from Revision * (December 2011) to Revision A (March 2012) **Page**

- Changed Description From: full industrial temperature range of –40°C to 85°C To: full industrial temperature range of –40°C to 105°C....1
- Added Operating Temperature to the Abs Max Table....5
- Changed the Operating free-air temperature From MAX = 85°C To: 105°C....5
- Changed the values of ψ_{JT} and ψ_{JB} in the Thermal Information table....5
- Changed the MAX value of Leakage current (Dx_SEL), VDD = 0 V From: 8µA To: 10µA....6

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5 Pin Configuration and Function

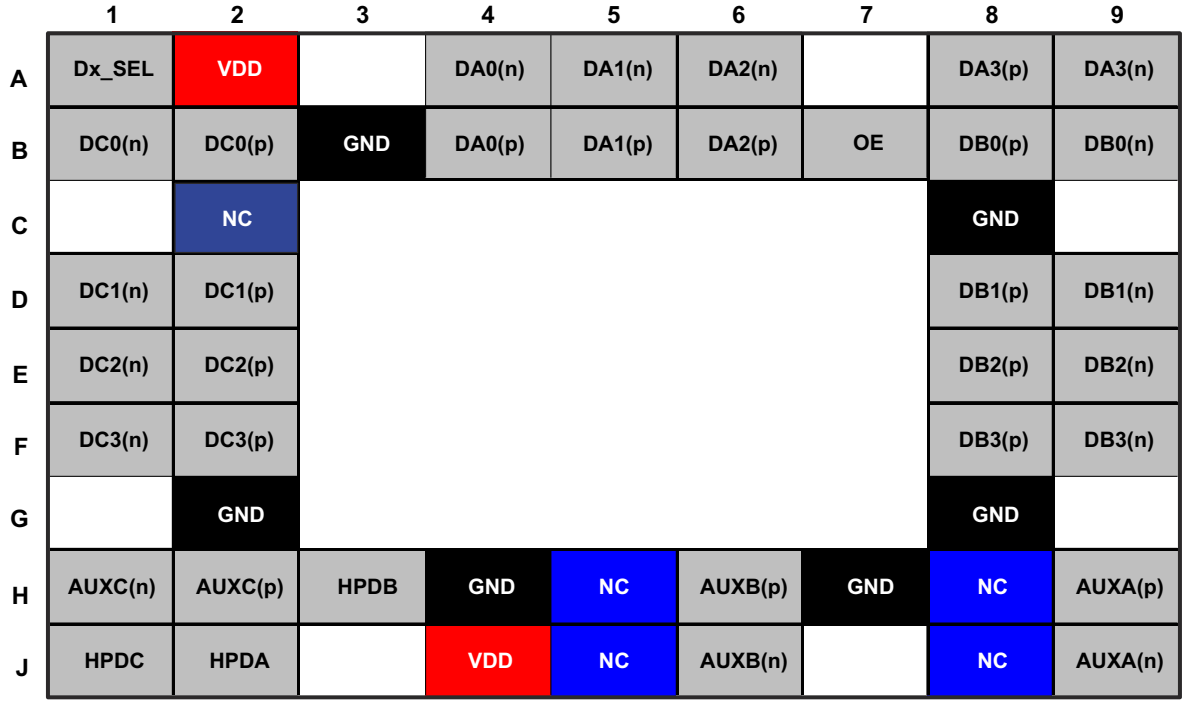

Table 5-1. Pin Functions

PIN	PIN NAME	I/O	DESCRIPTION
A1	Dx_SEL	Control I	High Speed Port Selection Control Pins
B4 A4	DA0(p) DA0(n)	I/O	Port A, Channel 0, High Speed Positive Signal Port A, Channel 0, High Speed Negative Signal
B5 A5	DA1(p) DA1(n)	I/O	Port A, Channel 1, High Speed Positive Signal Port A, Channel 1, High Speed Negative Signal
B6 A6	DA2(p) DA2(n)	I/O	Port A, Channel 2, High Speed Positive Signal Port A, Channel 2, High Speed Negative Signal
A8 A9	DA3(p) DA3(n)	I/O	Port A, Channel 3, High Speed Positive Signal Port A, Channel 3, High Speed Negative Signal
B8 B9	DB0(p) DB0(n)	I/O	Port B, Channel 0, High Speed Positive Signal Port B, Channel 0, High Speed Negative Signal
D8 D9	DB1(p) DB1(n)	I/O	Port B, Channel 1, High Speed Positive Signal Port B, Channel 1, High Speed Negative Signal
E8 E9	DB2(p) DB2(n)	I/O	Port B, Channel 2, High Speed Positive Signal Port B, Channel 2, High Speed Negative Signal
F8 F9	DB3(p) DB3(n)	I/O	Port B, Channel 3, High Speed Positive Signal Port B, Channel 3, High Speed Negative Signal
B2 B1	DC0(p) DC0(n)	I/O	Port C, Channel 0, High Speed Positive Signal Port C, Channel 0, High Speed Negative Signal
D2 D1	DC1(p) DC1(n)	I/O	Port C, Channel 1, High Speed Positive Signal Port C, Channel 1, High Speed Negative Signal
E2 E1	DC2(p) DC2(n)	I/O	Port C, Channel 2, High Speed Positive Signal Port C, Channel 2, High Speed Negative Signal
F2 F1	DC3(p) DC3(n)	I/O	Port C, Channel 3, High Speed Positive Signal Port C, Channel 3, High Speed Negative Signal
H9 J9	AUXA(p) AUXA(n)	I/O	Port A AUX Positive Signal Port A AUX Negative Signal
H6 J6	AUXB(p) AUXB(n)	I/O	Port B AUX Positive Signal Port B AUX Negative Signal

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Table 5-1. Pin Functions (continued)

PIN	PIN NAME	I/O	DESCRIPTION
H2 H1	AUXC(p) AUXC(n)	I/O	Port C AUX Positive Signal Port C AUX Negative Signal
J2, H3, J1	HPDA/B/C	I/O	Port A/B/C Hot Plug Detect
B7	OE	I	Output Enable
A2, J4	VDD	Supply	3.3V Positive power supply voltage
B3, C8, G2, G8, H4, H7	GND	Supply	Negative power supply voltage
C2, H5, H8, J5, J8	NC		Electrically not connected

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Supply voltage range(3)	VDD	–0.5	4	V
Voltage range	Differential I/O	–0.5	4	V
	Control pin	–0.5	VCC +0.5	V
Operating free-air temperature		–40	105	°C
Continuous power dissipation		See Section 6.4		
Storage temperature		–55	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) (1)	±4000	V
		Charged-device model (CDM) (2)	±1000	

(1) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(2) Tested in accordance with JEDEC Standard 22, Test Method A115-A

6.3 Recommended Operating Conditions

Nominal values for all parameters are at V_{CC} = 3.3V and T_A = 25°C, all temperature limits are specified by design

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		3.0	3.3	3.6	V
V_{IH}	Input high voltage	Control Pins, Signal Pins (Dx_SEL, OE) (HPDC, 5V Tolerant)	2.0		VDD	V
V_{IL}	Input low voltage	Control Pins, Signal Pins (Dx_SEL, OE, HPDC)	–0.1		0.8	V
V_{I/O_Diff}	Differential voltage (Dx, AUXx)	Switch I/O diff voltage	0		1.8	Vpp
V_{I/O_CM}	Common voltage (Dx, AUXx)	Switch I/O common mode voltage	0		2.0	V
	Operating free-air temperature		–40		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		HD3SS212 nFBGA (ZXH) 48-Ball	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	64.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	28.7	°C/W
θ_{JB}	Junction-to-board thermal resistance	36.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

under recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE PARAMETERS						
I_{IH}	Input high current (Dx_SEL)	VDD = 3.6 V, VIN = VDD		3	10	µA
I_{IL}	Input low current (Dx_SEL)	VDD = 3.6 V, VIN = GND		0.01	1	µA
I_{LK}	Leakage current (Dx_SEL)	VDD = 3.3 V, Vi = 2V, OE = 3.3V		2	5	µA
		VDD = 0 V, Vi = 2 V, OE = 3.3 V		6	10	
	Leakage current (HPDA)	VDD = 3.3 V, Vi = 2 V, OE = 3.3 V; Dx_SEL=3.3 V		0.01	2	
	Leakage current (HPDB)	VDD = 3.3 V, Vi = 2 V, OE = 3.3 V; Dx_SEL=GND		0.01	2	
I_{off}	Device shut down current	VDD = 3.6 V, OE = GND			5	µA
I_{DD}	Supply current	VDD = 3.6 V, Dx_SELx = VCC/GND; Outputs floating		2.5	5	mA
DA, DB, DC HIGH SPEED SIGNAL PATH						
C_{ON}	Outputs ON capacitance	Vi = 0 V, Outputs open, Switch ON		1.5		pF
C_{OFF}	Outputs OFF capacitance	Vi = 0 V, Outputs open, Switch OFF		1		pF
R_{ON}	Output ON resistance	VDD = 3.3 V, VCM = 0.5V - 1.5 V, I_O = –40 mA		6.5	10	Ω
ΔR_{ON}	On resistance match between pairs of the same channel	VDD = 3.3 V; -0.35V ≤ VI ≤ 1.2 V; I_O = –40 mA			1.5	Ω
R_{FLAT_ON}	On resistance flatness ($R_{ON\ (MAX)} – R_{ON\ (MAIN)}$)	VDD = 3.3 V; -0.35 V ≤ VI ≤ 1.2 V		1.3		Ω
AUXx SIGNAL PATH						
C_{ON}	Outputs ON capacitance	Vi = 0 V, Outputs open, Switch ON		9		pF
C_{OFF}	Outputs OFF capacitance	Vi = 0 V, Outputs open, Switch OFF		3		pF
R_{ON}	Output ON resistance	VDD = 3.3 V, VCM = 0.5 V - 1.5 V, I_O = -40 mA		7	12	Ω
DEVICE PARAMETERS (under recommended operating conditions; R_L, R_{sc} = 50 Ω unless otherwise noted						
t_{PD}	Switch propagation delay	R_{sc} and RL = 50 Ω, See Figure 7-2			200	ps
T_{on}	Dx_SEL -to-Switch Ton (Data and AUX)	R_{sc} and RL = 50 Ω, See Figure 7-1		175	250	ns
T_{off}	Dx_SEL -to-Switch Toff (Data and AUX)			175	250	
T_{on}	Dx_SEL -to-Switch Ton (HPD)	RL = 50 Ω, See Figure 7-1		275	350	ns
T_{off}	Dx_SEL -to-Switch Toff (HPD)			275	350	
$T_{SK(O)}$	Inter-pair output skew (CH-CH)	R_{sc} and RL = 1 kΩ, See Figure 7-2			50	ps
$T_{SK(b-b)}$	Intra-pair output skew (bit-bit)			1	4	
RL	Dx Differential return loss(1)	1.35 GHz, See *Section 6.6*		–17		dB
		2.7 GHz, See *Section 6.6*		–11		
X_{TALK}	Dx Differential crosstalk(1)	2.7 GHz		–50		
O_{IRR}	Dx Differential off-isolation(1)	2.7 GHz, See *Section 6.6*		–22		
I_L	Dx Differential insertion loss(1)	f = 1.35 GHz, See *Section 6.6*		–0.7		dB
		f = 2.7 GHz, See *Section 6.6*		–1.4		
		f = 5.4 GHz, See *Section 6.6*		–1.7		
	AUX Differential insertion loss(1)	f = 360 MHz		–1		dB

(1) For Return Loss, Crosstalk, Off-Isolation, and Insertion Loss values the data was collected on a Rogers material board with minimum length traces on the input and output of the device under test.

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6.6 Typical Characteristics

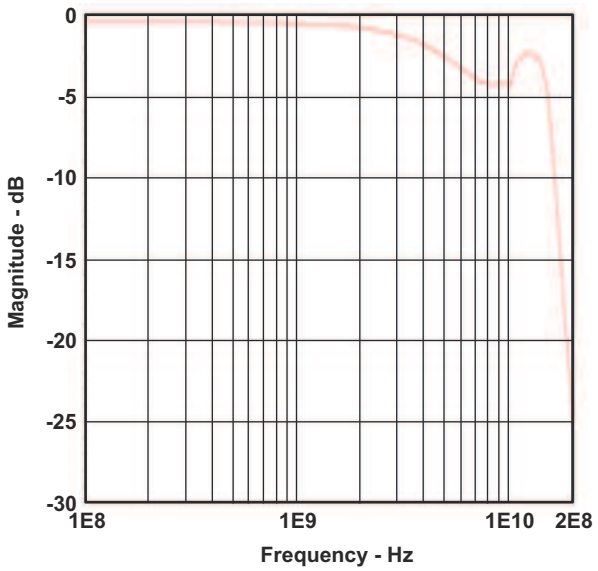

Figure 6-1. Insertion Loss and -3dB Bandwidth

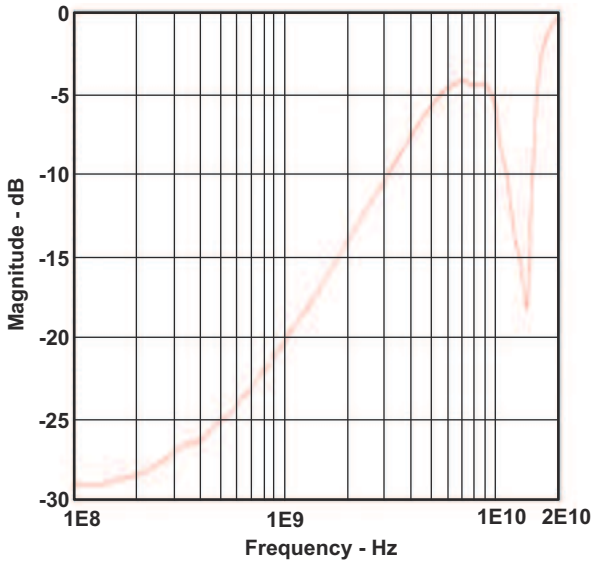

Figure 6-2. Return Loss

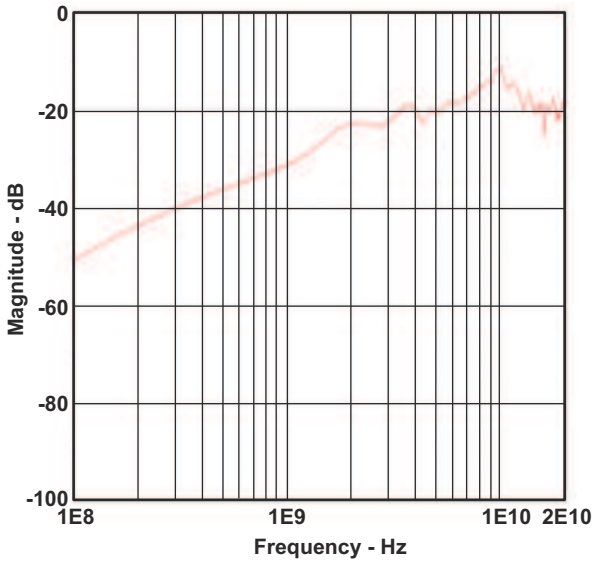

Figure 6-3. OF Isolation

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7 Parameter Measurement Information

7.1 Test Timing Diagrams

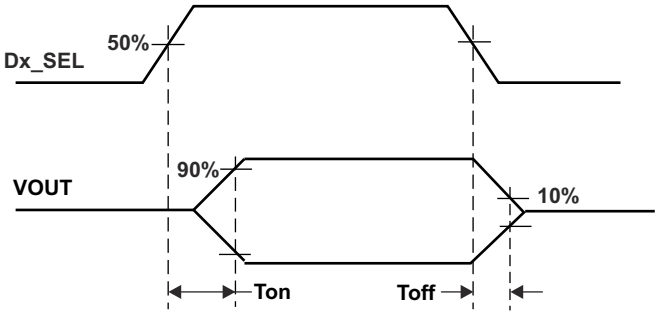

Figure 7-1. Select to Switch T_{on} and T_{off}

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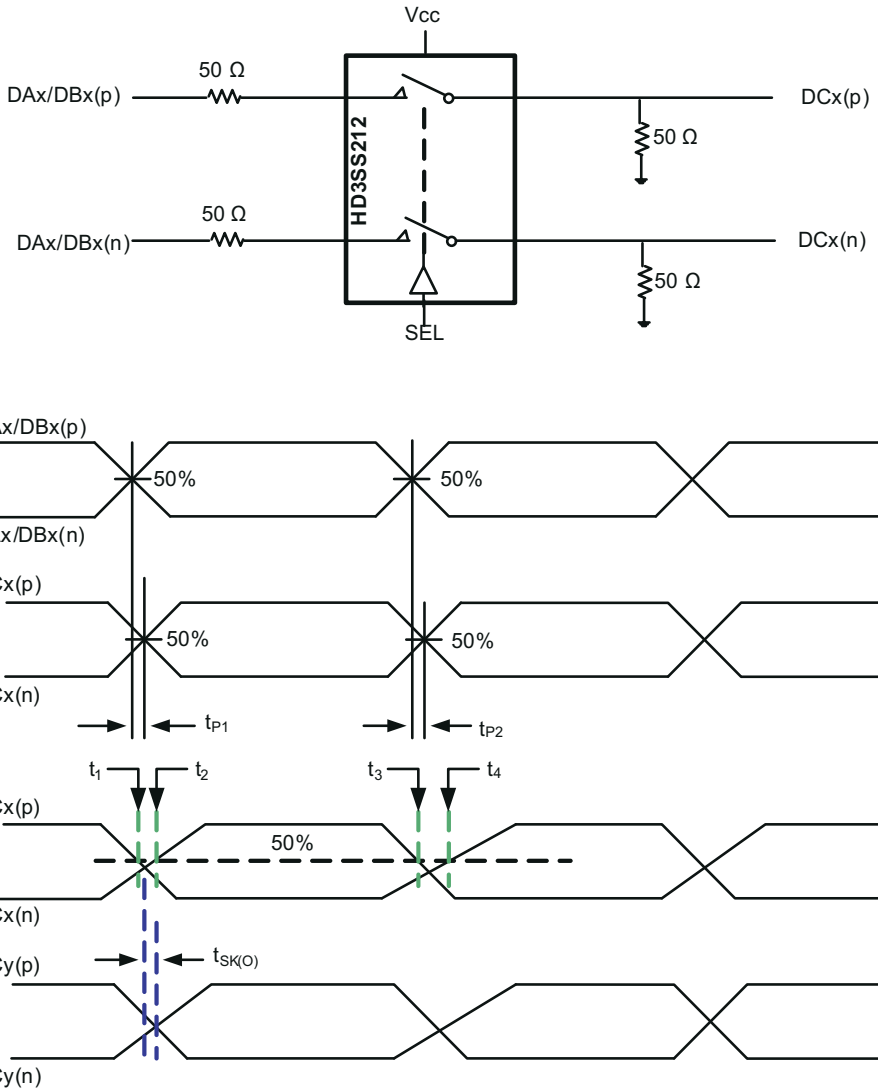


t_{PD} = Max(t_{p1}, t_{p2})

$t_{SK(O)}$ = Difference between t_{PD} for any two pairs of outputs

$t_{SK(b\text{-}b)}$ = 0.5 X |(t_4 – t_3) + (t_1 – t_2)|

Figure 7-2. Propagation Delay and Skew

8 Detailed Description

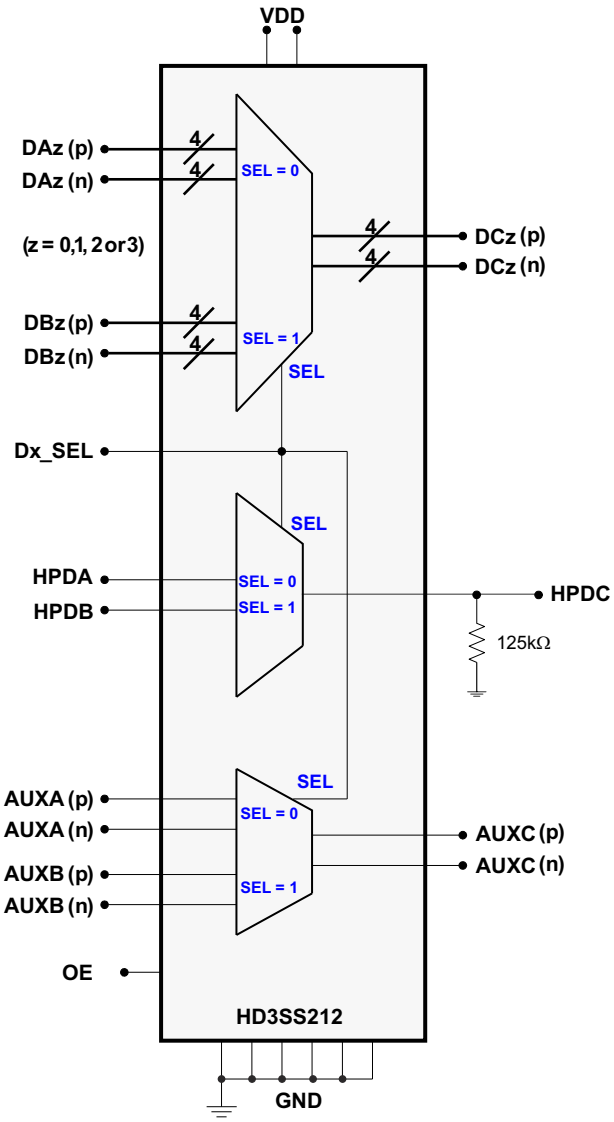
8.1 Overview

The HD3SS212 is a high-speed passive switch offered in an industry standard 48-pin u*BGA package available in a common footprint shared by several other vendors. The device is specified to operate from a single supply voltage of 3.3 V over the industrial temperature range of -40°C to 105°C.

The HD3SS212 is a generic 4-CH high-speed mux/demux type of switch that can be used for routing high-speed signals between two different locations on a circuit board. The HD3SS212 will also support several other high-speed data protocols with a differential amplitude of < 1800 mVpp and a common-mode voltage of < 2.0 V, as with USB 3.0 and DisplayPort 1.2. For Display Port Applications the HD3SS212 also supports switching of both the Auxiliary and Hot Plug Detect signals.

The device's High Speed Port Selection Control input (Dx_SEL) pin can easily be controlled by an available GPIO pin within a system.

8.2 Functional Block Diagram



8.3 Feature Description

Refer to *Section 8.2*.

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The HD3SS212 behaves as a two to one using high bandwidth pass gates. The input port is selected using the Dx_SEL pin according to Table 8-1.

Table 8-1. Switch Control Logic

CONTROL LINES	SWITCHED I/O PINS(1) (2)				
Dx_SEL	DCz(p) PIN z = 0, 1, 2 or 3	DCz(n) PIN z = 0, 1, 2 or 3	HPDC PIN	AUXC(p) PIN	AUXC(n) PIN
L	DAz(p)	DAz(n)	HPDA	AUXA(p)	AUXA(n)
H	DBz(p)	DBz(n)	HPDB	AUXVB(p)	AUXVB(n)

(1) OE pin - For nomal operation, drive OE high. Driving the OE pin low will disable the switch to enable power savings.
(2) The ports which are not selected by the Control Lines will be in High Impedance State.

8.4 Device Functional Modes

The HD3SS212 can be operated in normal operation mode or in shut down mode. In normal operation, the input ports of the HD3SS212 are routed to the output ports according to Table 8-1. In shut down mode the HD3SS212 is disabled to enable power savings with a typical current consumption of 5 µA. The functional mode is selected through the OE input pin with High for normal operation and LOW for shut down.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 AC Coupling Caps

Many interfaces require AC coupling between the transmitter and receiver. The 0402 capacitors are the preferred option to provide AC coupling, and the 0603 size capacitors also work. The 0805 size capacitors and C-packs should be avoided. When placing AC coupling capacitors symmetric placement is best. A capacitor value of 0.1 µF is best and the value should be match for the ± signal pair. The placement should be along the TX pairs on the system board, which are usually routed on the top layer of the board. There are several placement options for the AC coupling capacitors. Because the switch requires a bias voltage, the capacitors must only be placed on one side of the switch. If they are placed on both sides of the switch, a biasing voltage should be provided. A few placement options are shown below. In Figure 9-1, the coupling capacitors are placed between the switch and endpoint. In this situation, the switch is biased by the system/host controller.

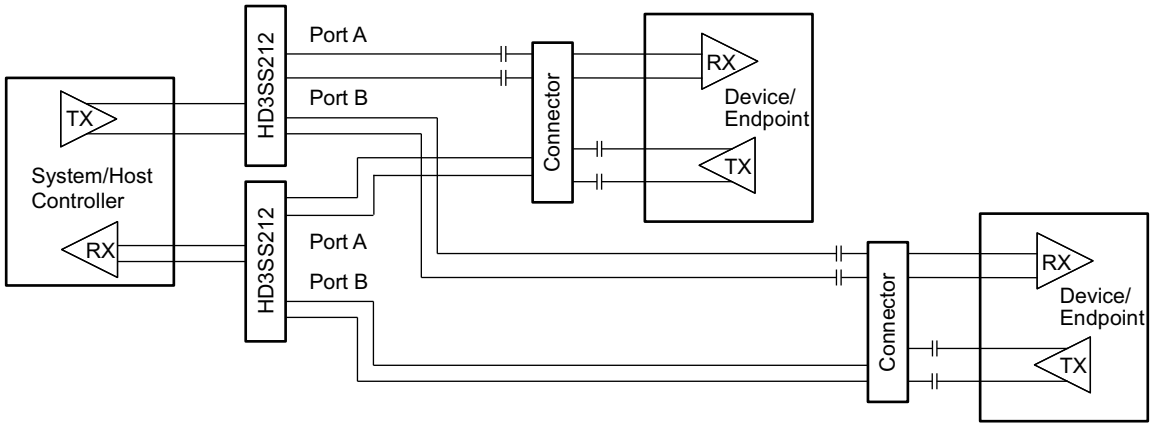

Figure 9-1. AC Coupling Capacitors Between Switch TX and Endpoint TX

In Figure 9-2, the coupling capacitors are placed on the host transmit pair and endpoint transmit pair. In this situation, the switch on the top is biased by the endpoint and the lower switch is biased by the host controller.

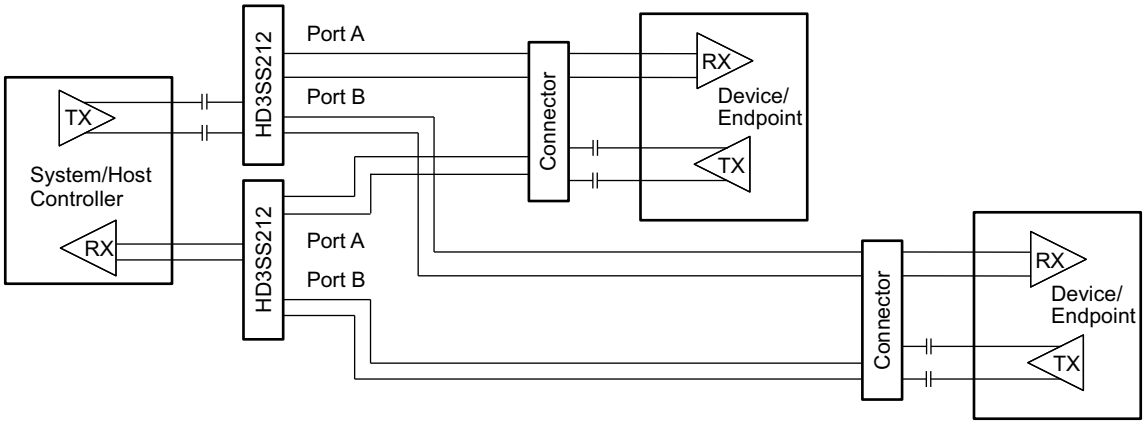

Figure 9-2. AC Coupling Capacitors on Host TX and Endpoint TX

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If the common-mode voltage in the system is higher than 2 V, the coupling capacitors are placed on both sides of the switch (shown in Figure 9-3). A biasing voltage of less than 2 V is required in this case.

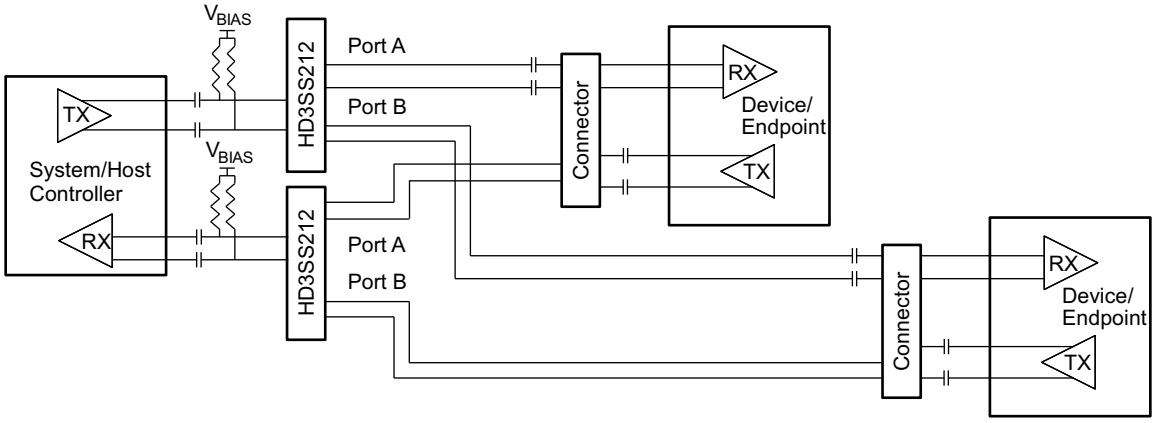

Figure 9-3. AC Coupling Capacitors on Both Sides of Switch

9.2 Typical Application

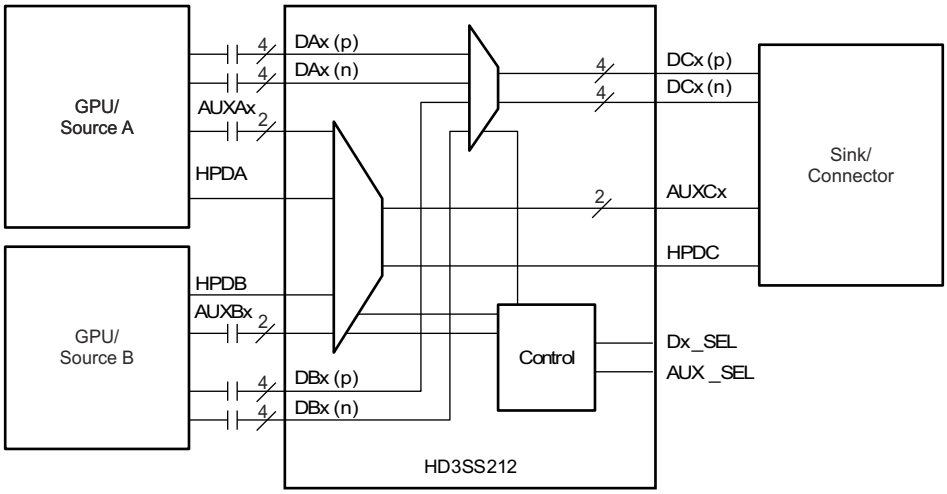

Figure 9-4. Dual Source Connection Block Diagram

9.2.1 Design Requirements

Table 9-1 lists the design parameters.

Table 9-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	3.3 V
Decoupling capacitors	0.1 µF
AC capacitors	75 nF – 200 nF (100 nF shown) USBAA TX p and AC capacitors n lines require AC capacitors. Alternate mode signals may or may not require AC capacitors

9.2.2 Detailed Design Procedure

- Connect VDD and GND pins to the power and ground planes of the printed circuit board, with 0.1-µF bypass capacitor
- Use +3.3-V TTL/CMOS logic level at SEL

- Use controlled-impedance transmission media for all the differential signals
- Ensure the received complimentary signals are with a differential amplitude of < 1800 mVpp and a common-mode voltage of < 2V.

9.2.3 Application Curves

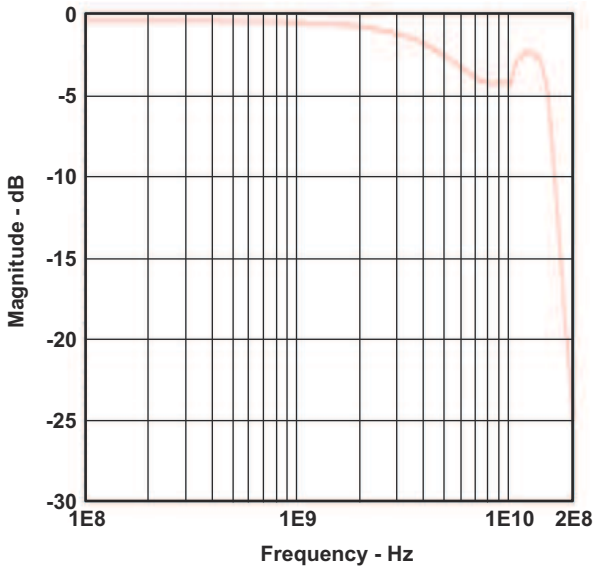

Figure 9-5. Insertion Loss and -3dB Bandwidth

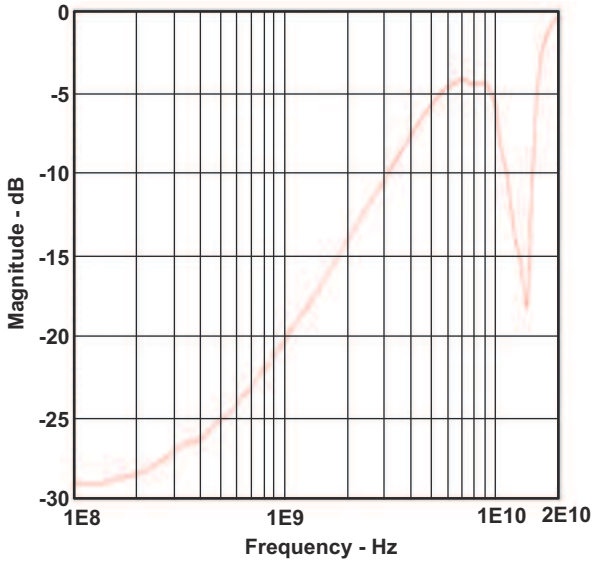

Figure 9-6. Return Loss

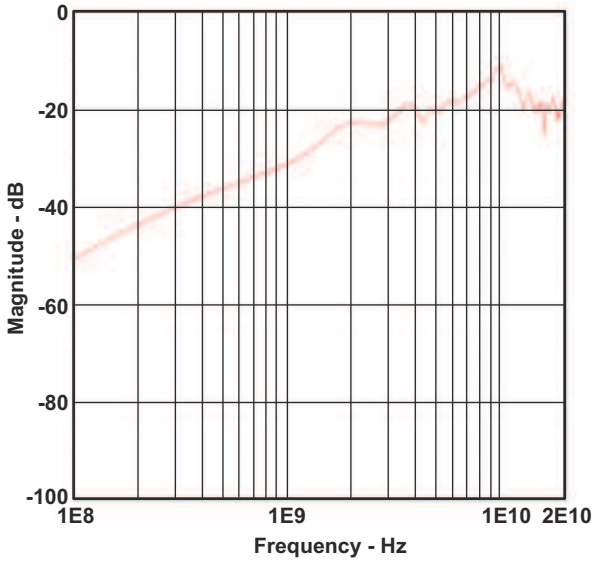

Figure 9-7. OF Isolation

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Power Supply Recommendations

The HD3SS212 requires +3.3-V digital power sources. VDD 3.3 supply must have 0.1-µF bypass capacitors to VSS (ground) in order for proper operation. The recommendation is one capacitor for each power terminal. Place the capacitor as close as possible to the terminal on the device and keep trace length to a minimum. Smaller value capacitors like 0.01-µF are also recommended on the digital supply terminals.

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10 Layout

10.1 Layout Guidelines

- Decoupling caps should be placed next to each power terminal on the HD3SS212. Take care to minimize the stub length of the race connecting the capacitor to the power pin.
- Avoid sharing vias between multiple decoupling caps
- Place vias as close as possible to the decoupling cop solder pad
- Widen VDD/GND planes to reduce effect if static and dynamic IR drop
- The VBUS traces/planes must be wide enough to carry maximum of 2-A current

10.2 Layout Example

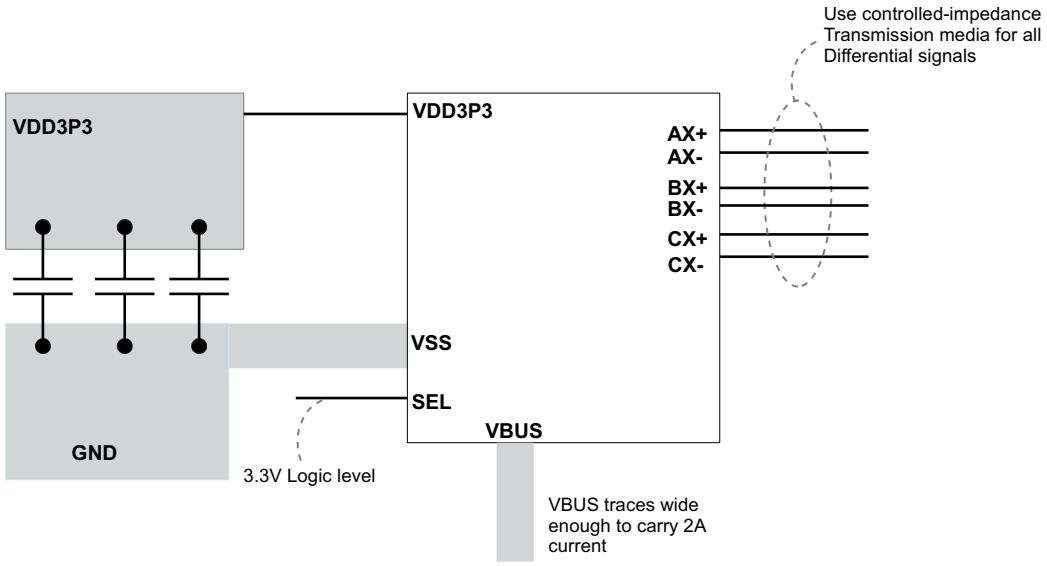

Figure 10-1. Layout Example

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11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resource

11.3 Trademarks

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
HD3SS212ZXHR	Active	Production	NFBGA (ZXH) | 48	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 105	HD3SS212
HD3SS212ZXHR.B	Active	Production	NFBGA (ZXH) | 48	2500 | LARGE T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 105	HD3SS212
HD3SS212ZXHT	Active	Production	NFBGA (ZXH) | 48	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 105	HD3SS212
HD3SS212ZXHT.B	Active	Production	NFBGA (ZXH) | 48	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 105	HD3SS212

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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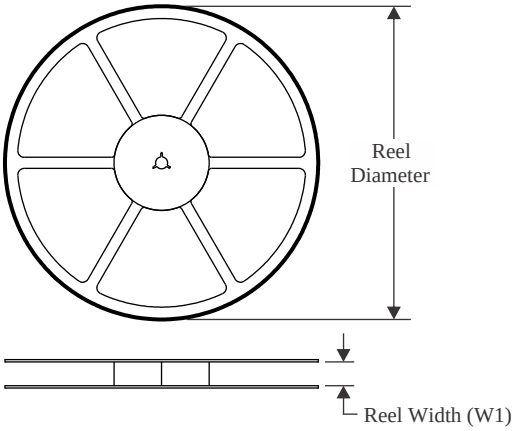
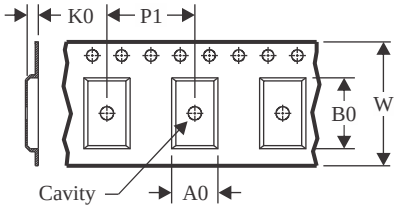
TAPE AND REEL INFORMATION

REEL DIMENSIONS

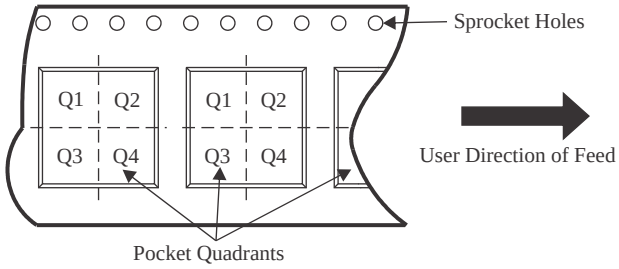


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

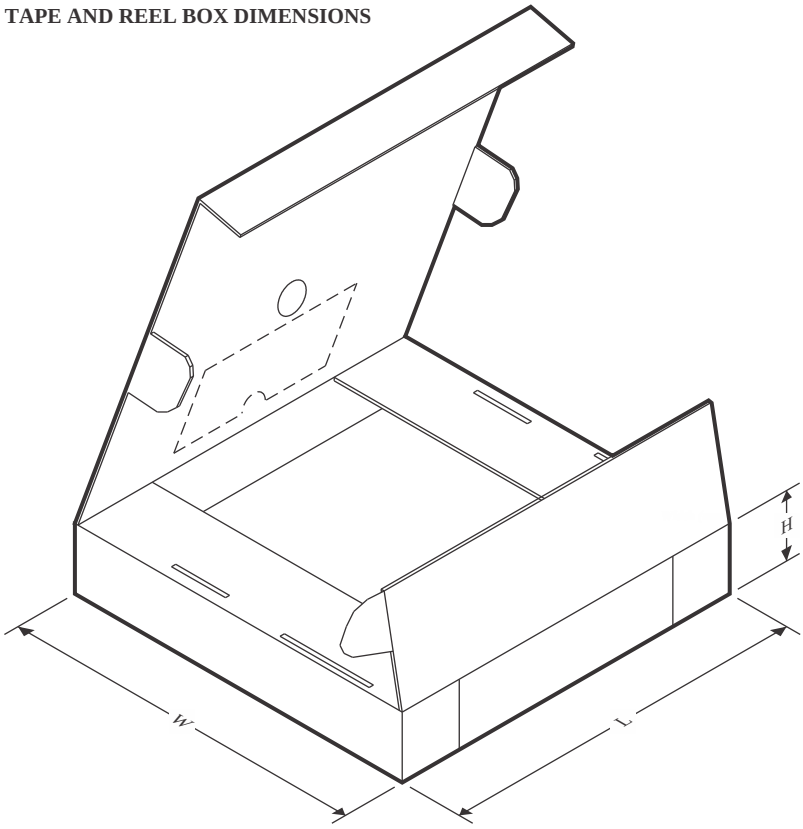
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

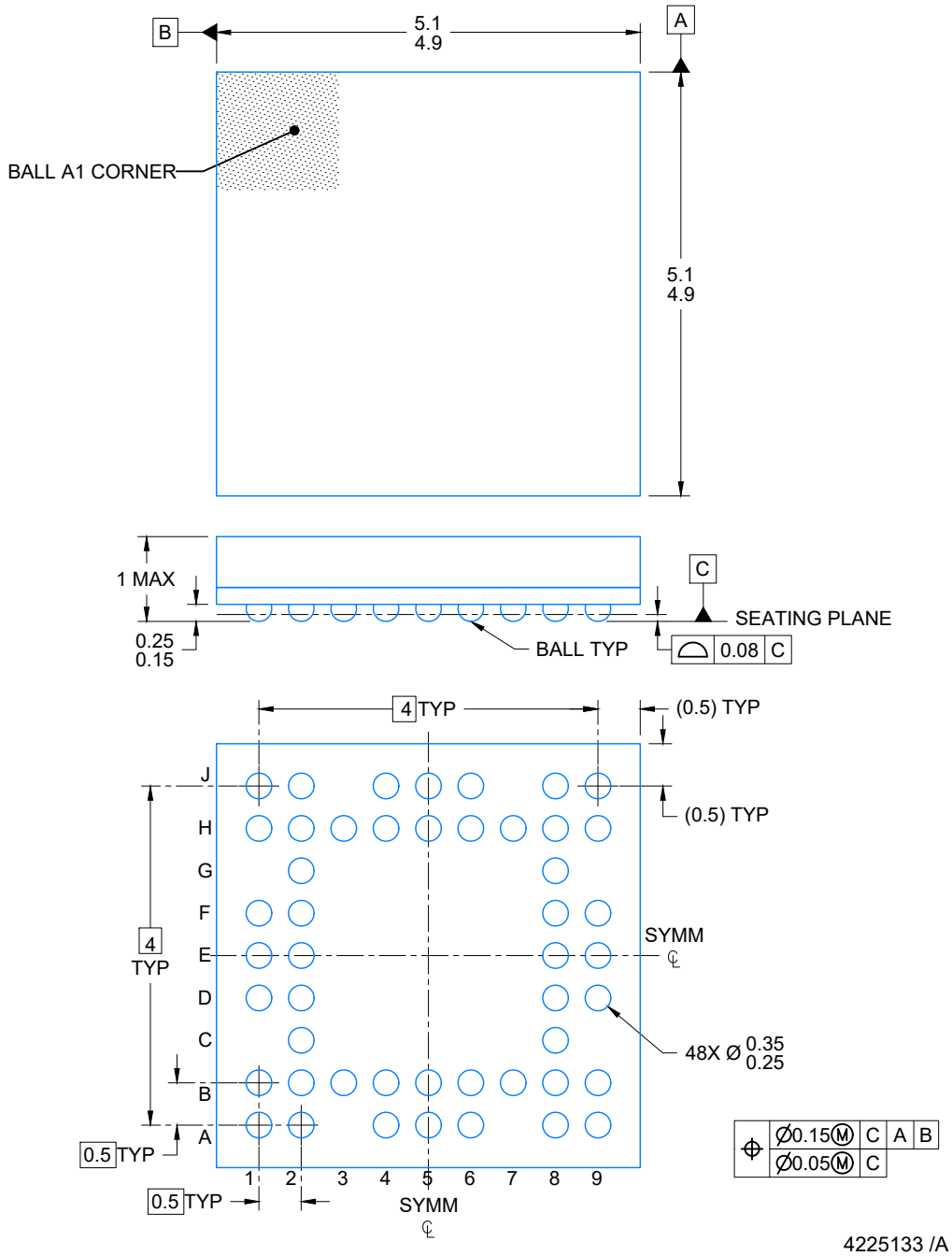
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS212ZXHR	NFBGA	ZXH	48	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1
HD3SS212ZXHT	NFBGA	ZXH	48	250	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS212ZXHR	NFBGA	ZXH	48	2500	336.6	336.6	31.8
HD3SS212ZXHT	NFBGA	ZXH	48	250	336.6	336.6	31.8



NOTES:

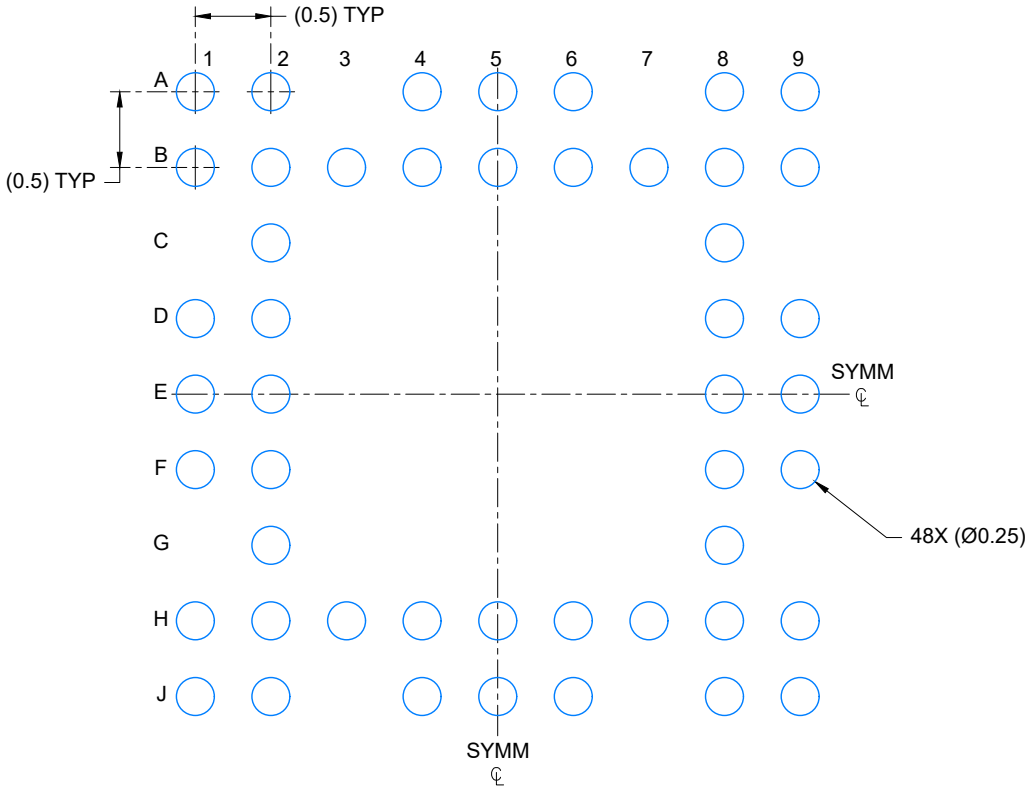
NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

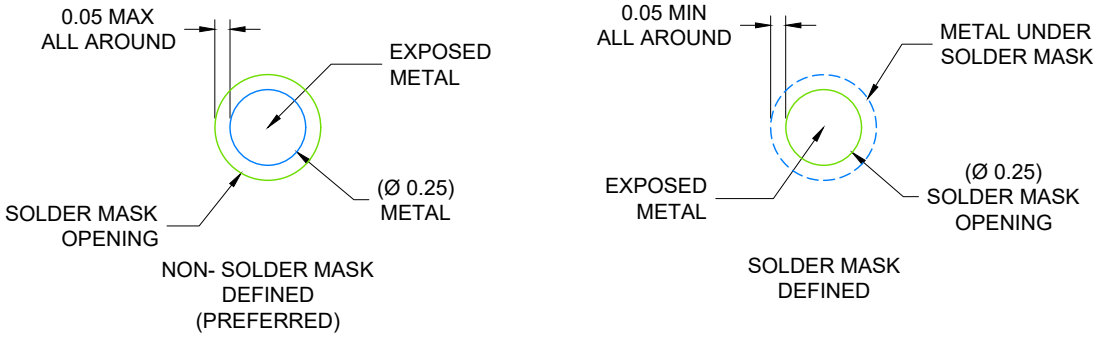
EXAMPLE BOARD LAYOUT

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE: 20X



SOLDER MASK DETAILS
NOT TO SCALE

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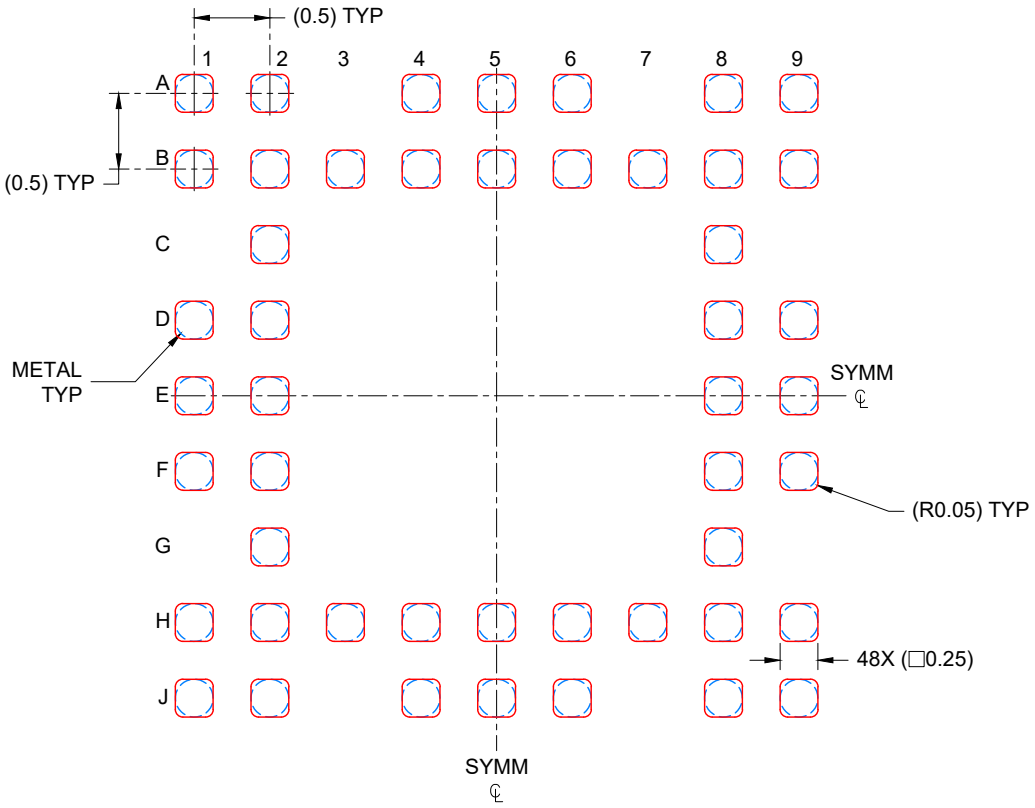
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 20X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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