HMC702LP6CE

v10.0812

14 GHz 16-BIT FRACTIONAL-N PLL

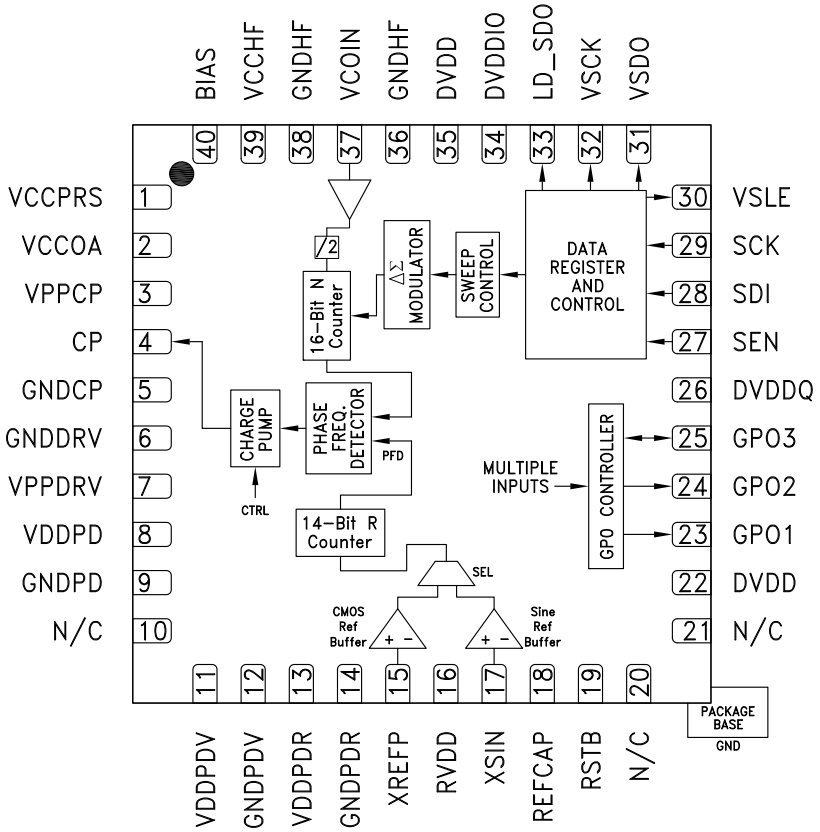
Features

- Fractional or Integer Modes
- 14 GHz, 16-Bit RF N-Counter
- 24-Bit Step Size Resolution, 6 Hz typ
- Ultra Low Phase Noise 12 GHz, 50 MHz Ref. -98 / -103 dBc/Hz @ 20 kHz (Frac / Integer)
- Reference Path Input: 200 MHz
- 14-Bit Reference Path Divider
- Low Fractional Spurious
- Reference spurs: -90 dBc typ
- Auto and Triggered Sweeper Functions
- Cycle Slip Prevention (CSP) for fast settling
- Auxiliary Clock Source
- 40 Lead 6x6mm SMT Package: 36mm²

Typical Applications

- Base Stations for Mobile Radio (GSM, PCS, DCS, CDMA, WCDMA)
- Wireless LANs, WiMax
- Communications Test Equipment
- CATV Equipment
- FMCW Sensors
- Automotive Radar
- Phased-Array Systems

Functional Diagram



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General Description

The HMC702LP6CE is a SiGe BiCMOS fractional-N PLL. The fractional-N PLL includes a fixed divide by 2 followed by a 8GHz 16-bit RF N-Divider, a 24-bit delta-sigma modulator, a very low noise digital phase frequency detector (PFD), and a precision controlled charge pump.

The fractional-N PLL features an advanced delta-sigma modulator design that allows ultra-fine frequency step sizes. The fractional-N PLL features the ability to alter both the phase-frequency detector (PFD) gain and the cycle slipping characteristics of the PFD. This feature can reduce the time to arrive at the new frequency by 50% vs. conventional PFDs. Ultra low in-close phase noise also allows wider loop bandwidths for faster frequency hopping.

The fractional-N PLL contains a built-in linear sweeper function, which allows it to perform frequency chirps with a wide variety of sweep times, polarities and dwells, all with an external or automatic sweep trigger.

In addition the fractional-N PLL has a number of auxiliary clock generation modes that can be accessed via the GPO.

Electrical Specifications, T_A = +25°C

VCCHF = VCCPRS = RVDD = +3.3V
VPPCP = VCCOA = VDDPDR = VPPDRV = VDDPD = VDDPDV = +5V
DVDD = DVDDIO = DVDDQ = +3.3V
GNDDRV = GNDCP = GNDPD = GNDPDV = GNDPDR = 0V

Table 1. Electrical Specifications

Parameter	Conditions / Notes	Min	Typ	Max	Units
Prescaler Characteristics					
Max RF Input Frequency (3.3V)		12	14		GHz
Max RF Input Frequency (2.7 - 3.3V)		12	13		GHz
Min RF Input Frequency		0.1			MHz
RF Input Power	Fmin<Fvco<10 GHz Fvco>10 GHz	-10 0	-6	10	dBm
16-bit N-Divider Range (Integer)	16-Bit divider and fixed divide-by-2 step of 2	64		131,070	
16-bit N-Divider Range (Fractional)	Fraction Nominal Divide ratio varies (-6 / +8) dynamically max	72		131,062	
REF Input Characteristics					
Max Ref Input Frequency (pin XREFP)		250			MHz
Max Ref Input Frequency (pin XSIN)		250			MHz
Min Ref Input Frequency	XSIN minimum 20MHz due to phase noise degradation	100			kHz
Ref Input Voltage Range (pin XREFP)	AC Coupled	1.5	2.0	3.3	Vpp
Ref Input Power Range (pin XSIN)	50 Ω Source	-6	0	12	dBm
Ref Input Capacitance				5	pF
14-Bit R-Divider Range		1		16,383	

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Table 1. Electrical Specifications *(Continued)*

Parameter	Conditions / Notes	Min	Typ	Max	Units
Phase Detector					
Fractional Mode					
Phase Detector Frequency		0.1		70	MHz
Integer Mode					
Phase Detector Frequency		0.1		100	MHz
Charge Pump					
Max Output Current			4		mA
Min Output Current			125		µA
Charge Pump Gain Step Size (5-bits)			125		µA
Charge Pump Trim Step Size (3-bits)			14		µA
Charge Pump Offset Step Size (4-bits)			29		µA
PFD / Charge Pump Noise (Integer)	6 GHz, 50 MHz Ref, Input referred				
1 kHz			-141		dBc/Hz
10 kHz			-149		dBc/Hz
100 kHz			-155		dBc/Hz
Compliance Voltage	Less than 3 dB degradation typ. at these limits				
	-406 µA Offset	0.4		VPPCP-0.8	V
	-406 µA Offset	0.8		VPPCP-0.4	V
Logic Inputs					
VIH Input High Voltage		VDDIO-0.4			V
VIL Input Low Voltage				0.4	V
Logic Outputs					
VIH Output High Voltage		VDDIO-0.1			V
VIL Output Low Voltage				0.1	V
Power Supply Voltages					
VCC - Analog 3V Supplies	VCCPRS, RVDD, VCCHF	3	3.3	3.45	V
DVDD - Digital Internal Supply	DVDD, DVDDQ	3	3.3	3.45	V
DVDDIO - Digital I/o Supply	DVDDIO	3	3.3	3.45	V
Analog 5V Supplies	VCCOA, VPPCP, VPPDRV, VDDPD, VDDPDV, VDDPDR	4.5	5.0	5.5	V
Power Supply Current (6 GHz Fractional Mode, 50 MHz PFD)					
Analog +5V	VCCOA, VPPCP, VPPDRV, VDDPD, VDDPDV, VDDPDR		26		mA
Analog +3.3V	VCCPRS, RVDD, VCCHF		116		mA
Digital +3.3V	DVDD, DVDDIO, DVDDQ		19		mA
Power Down - Crystal Off	Reg 01h = 0 Crystal not clocked		10		µA
Power Down - Crystal On, 100 MHz	Reg 01h = 0 Crystal clocked 100 MHz		20	200	µA
Temperature Sensor (3-bit)					
Min Temperature	Readout: 000		-32		°C

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Table 1. Electrical Specifications (Continued)

Parameter	Conditions / Notes	Min	Typ	Max	Units
Max Temperature	Readout: 111		+82		°C
Temp Change / LSB			17.5		°C/LSB
Worst Case Absolute Temp Error			±10		°C
Current Consumption (when Enabled)			2		mA
Power on Reset All digital inputs must be <0.7V prior to application of power for proper reset					
Typical Reset Voltage on DVDD			700		mV
Min DVDD Voltage for No Reset		1.5			V
Closed Loop Phase Noise					
12 GHz VCO, Integer, 100 MHz PFD	1 kHz offset		-96		dBc/Hz
12 GHz VCO, Integer, 100 MHz PFD	10 kHz offset		-105		dBc/Hz
12 GHz VCO, Integer, 100 MHz PFD	100 kHz offset		-111		dBc/Hz
12 GHz VCO, Fractional, 50 MHz PFD	1 kHz offset		-92		dBc/Hz
12 GHz VCO, Fractional, 50 MHz PFD	10 kHz offset		-98		dBc/Hz
12 GHz VCO, Fractional, 50 MHz PFD	100 kHz offset		-103		dBc/Hz
Closed Loop Phase Noise	Normalized to 1 Hz				
Integer Mode	Measured with 50 MHz PFD		-227		dBc/Hz
Fractional Mode	Measured with 50 MHz PFD		-221		dBc/Hz

Table 2. Absolute Maximum Ratings

Parameter	Rating
RVDD, VCCHF, DVDD, DVDDQ, VCCPRS	-0.3 to +3.6V
VCCOA, VPPCP, VPPDRV, VDDPD, VDDPDV, VDDPDR, DVDDIO	-0.3 to +6V
Operating Temperature	-40 to +85 °C
Storage Temperature	-65 to +120 °C
Maximum Junction Temperature	+125 °C
Thermal resistance (Rth) (Junction to ground paddle)	25°C/W
Reflow Soldering	
Peak Temperature	260 °C
Time at Peak Temperature	40 sec
ESD Sensitivity (HBM)	Class 1B

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Table 3. Pin Description

Pin No.	Pin Name	PIn Type	Description
1	VCCPRS	Supply	RF Prescaler Power Supply. Nominally +3.3V
2	VCCOA	Supply	ChargePump OpAmp Power Supply. Nominally +5V
3	VPPCP	Supply	Power Supply for Charge Pump. Nominally +5V
4	CP	Analog O/P	Charge Pump output
5	GNDCP	GND	Power Supply GND for Charge Pump
6	GNDDRV	GND	Charge Pump GND
7	VPPDRV	Supply	Power supply for Charge Pump, Nominally +5V
8	VDDPD	Supply	Power Supply for Phase Detectors, Nominally +5V
9	GNDPD	GND	Power Supply GND for Phase Detector
10, 20, 21	N/C	N/C	No Connection
11	VDDPDV	Supply	Power Supply for Phase Detector VCO Path, Nominally +5V
12	GNDPDV	GND	Power Supply GND for Phase Detector VCO Path
13	VDDPDR	Supply	Power Supply for Phase Detector Ref Path, Nominally +5V
14	GNDPDR	GND	Power Supply GND for Phase Detector Ref Path
15	XREFP	Analog I/P	Square Wave Crystal Ref Input
16	RVDD	Supply	Power Supply for Ref Path, Nominally +3.3V
17	XSIN	Analog I/P	Sinusoidal Crystal reference input
18	REFCAP	Analog I/O	Reference Path bypass
19	RSTB	CMOS I/P	Reset Input (active low). Cycle low for >Tref to reset. Recommended after power-up
22	DVDD	Supply	Digital Power Supply, Nominally +3.3V
23	GPO1	DO	General Purpose Output 1 with Tristate
24	GPO2	DO	General Purpose Output 2 with Tristate
25	GPO3	DIO	General Purpose Input/Output with Tristate may be configured for External Ramp trigger Input. See register REG 14h[5]
26	DVDDQ	Supply	Quiet Supply, Nominal +3.3V, Zero Current
27	SEN	CMOS I/P	Main Serial port enable input
28	SDI	CMOS I/P	Main Serial port data input
29	SCK	CMOS I/P	Main Serial port clock input
30	VSLE	DO	Leave pin disconnected.
31	VSDO	DO	Leave pin disconnected.
32	VSCK	DO	Leave pin disconnected.
33	LD_SDO	CMOS O/P	Lock Detect or Main Serial Port Data Output
34	DVDDIO	Supply	Power Supply for digital I/O, matches external Digital Supply in 1.8V to 5.5V range
35	DVDD	Supply	Internal Digital Power Supply. Nominally 3.3V
36	GNDHF	GND	Ground for RF
37	VCOIN	RF I/P	Input to the RF prescaler
38	GNDHF	GND	Ground for RF Input
39	VCCHF	Supply	RF Section Power Supply. Nominally 3.3V
40	BIAS	Analog I/P	Decoupling Pin for RF section, nominally external 1nF bypassed to VCCHF

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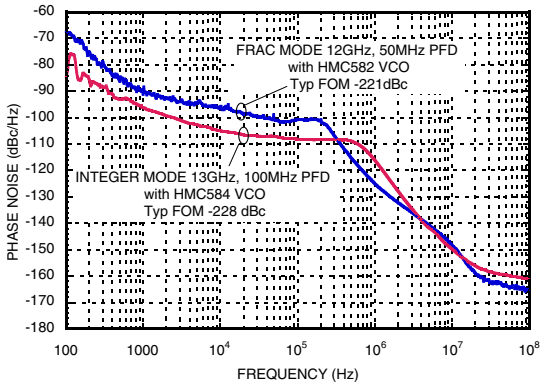
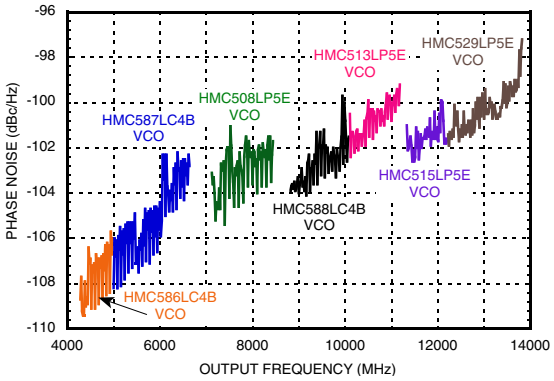
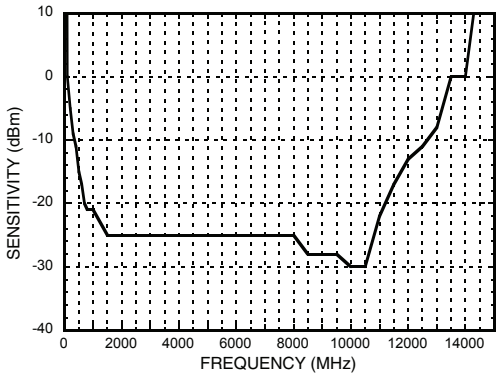
Typical Phase Noise



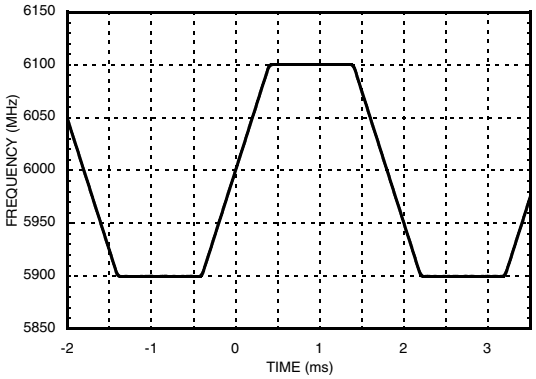
Typical Phase Noise @ 30 kHz Offset - Fractional Mode



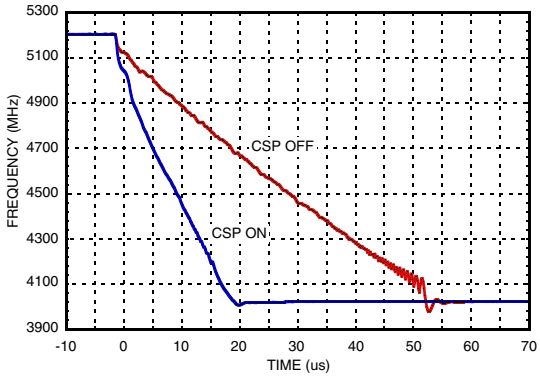
RF Divider Sensitivity



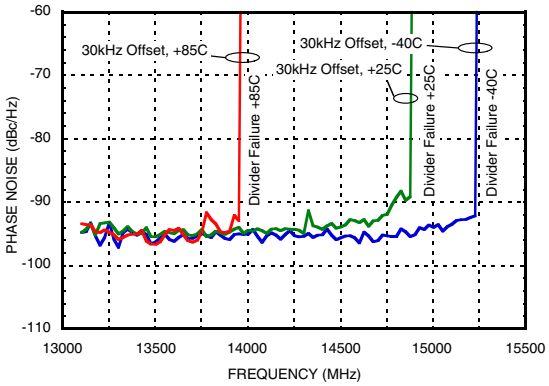
Frequency Sweep



Cycle Slip Prevention: Frequency Hop from 5200 MHz to 3950 MHz



Typical Max Frequency vs. Temperature -6 dBm, 3.3V



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Theory of Operation

The HMC702LP6CE synthesizer consists of the following functional blocks

1. Reference Path Input Buffers
2. Reference Path Divider
3. VCO Path Input Buffer
4. VCO Path Multi-Modulus Prescaler/Divider
5. ΔΣ Fractional Modulator
6. Phase Frequency Detector
7. Charge Pump
8. Main Serial Port
9. Auxiliary Serial Port
10. Temperature Sensor
11. Power On Reset Circuit
12. CW Sweeper Subsystem
13. Auxiliary Clock Generator
14. General Purpose Output (GPO) Bus
15. Multiple VCO Controller

Each of these blocks is described briefly in the following section.

Reference Path

The full Reference Path block diagram is shown in Figure 1. The ultra low noise phase detector requires the best possible reference signal. Since a given application may desire to use a square wave or a 50 Ohm sinusoidal crystal source, HMC702LP6CE offers two input ports, each one optimized for the lowest possible noise for the source type being used.

For absolute best low noise performance, the sine wave path should be used.

The user should use only one Ref path input, that is the input that matches their reference source type. Note the input is defaulted to the square wave input on power up. Should the sine reference path be used, it is necessary to enable the sine input, shut down the square wave input and set the mux (*rfp_buf_sin_en=1, rfp_buf_sq_en=0, rfp_buf_sin_sel=1*, Table 7). The unused port should be left open.

The reference path supports input frequencies of up to 250 MHz typical, however the maximum frequency at the phase detector (PFD) depends upon the mode of operation, worst case at +85°C, 70 MHz in fractional mode and 100 MHz in integer mode. Hence reference inputs of greater than the PFD maximum frequency must use the appropriate R divider setting.

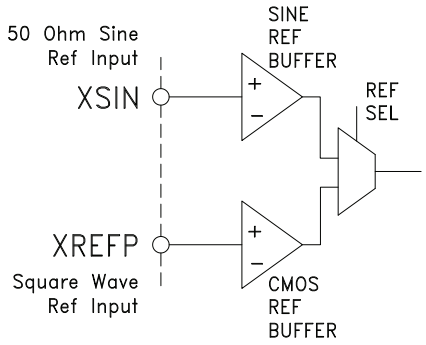

Figure 1. Reference Sine Input Stages

The unused reference port is normally not connected.

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Sine Reference Input

The crystal reference sine input stage is shown in Figure 2. This is the lowest noise reference path. This is a common emitter single ended bipolar buffer. The XSIN input pin is DC coupled and has about 950 mV bias on it. Expected input is a 0 dBm sinusoid from a 50 Ohm source. Normally the input should be AC coupled externally. The sine buffer input impedance is dominated by a 25 Ohm shunt resistor in series with a 50 pF on chip cap. Should a lower input impedance be needed, an external 50 Ohm shunt resistor can be used, DC isolated by an external bypass cap. The sine input reference path phase noise floor is approximately equivalent to -159 dBc/Hz. For best performance care should be taken to provide a crystal reference source with equivalent or better phase noise floor.

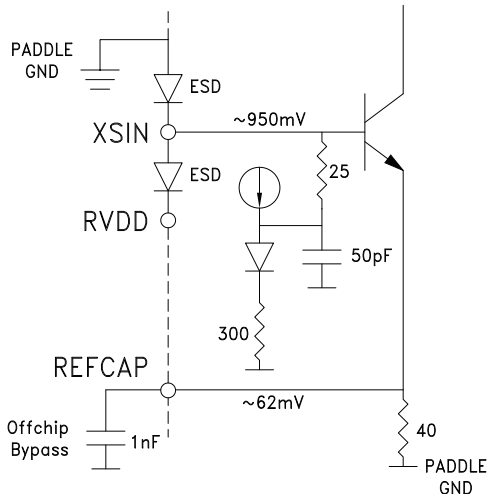

Figure 2. Ref Sine Input

Square Wave Reference Input

The square wave Ref Input stage is shown in Figure 3. The stage is designed to accept square wave inputs from CML to CMOS levels. Slightly degraded phase noise performance may be obtained with quasi sine 1 Vpp inputs. It may be necessary to attenuate very large CMOS levels if absolute best in close phase noise performance is required. Input reference should have a noise floor better than -160 dBc/Hz to avoid degradation of the input reference path.

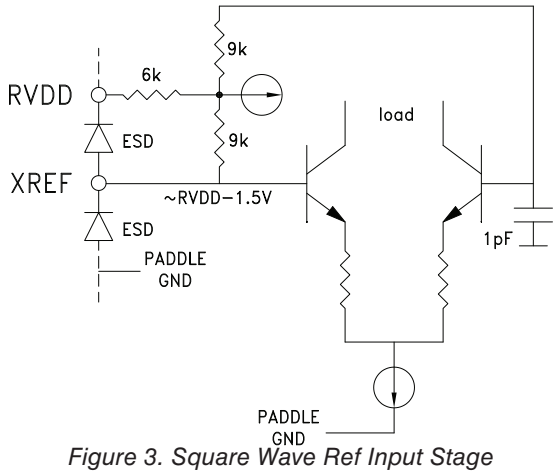

Figure 3. Square Wave Ref Input Stage

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Reference Path 'R' Divider

The referenced path features a 14-bit divider (*rfp_div_ratio, Reg03h<13:0>* Table 9) and can divide input signals at up to 250 MHz by numbers from 1 to 16,383. The selected input reference source may be divided or bypassed (*rfp_div_select*), and applied to the phase detector reference input.

Reference Path Test Features

A fractional synthesizer is a complex combination of a low phase noise analog oscillator running in close proximity with a nearly randomly modulated delta-sigma digital modulator.

Clean spur free operation of the synthesizer requires proper board layout of power and grounds. Spurious sources are often difficult to identify and may be related to harmonics of the digital modulation which land near the operating frequency of the VCO, or they may arise from repeating patterns in the digital modulation itself . The loop filter and the fractional modulator are designed to suppress these fractional spurs, but it is sometimes the case that the isolation of the spurious products comes from layout issues. The problem is how to identify the sources of spurious products if they occur?

The reference path of the HMC702LP6CE features some interesting test options for clocking the digital portion of the synthesizer which may provide for a better understanding of the source of reference spurs should they occur. See Figure 4, Table 7 and Table 24 for more register details.

For normal operation, Reg3h[15]=1. When Reg3h[15]=1, (rfp_auto_refdiv select enabled) then Reg 3 [14] & Reg 1 [2] are ignored. If Reg 3 [13:0] is programmed to >=2, RefDiv will be enabled and the divided output will be fed to the PFD. If Reg 3 [13:0] is programmed to 1, RefDiv will be disabled and the undivided reference signal will be fed to the PFD.

When Reg3h[15]=0 (rfp_auto_refdiv select disabled), then the state of the RefDiv is controlled by Reg 3 [14] & Reg 1 [2]. Then to enable RefDiv Reg 1 [2] = 1. To pass the divided reference signal to the PFD, Reg 3 [14]=1. If Reg 3 [14]=0, the undivided reference is passed directly to the PFD. This configuration would typically only be used for engineering test. It allows the RefDiv to be running while the PFD is operating with the undivided reference. This allows inspection for spurs that may be manifest from the divider running.

It is possible for example to set the synthesizer to integer mode of operation, where the digital harmonics normally fall directly on the VCO frequency. We might chose for example to use the sine source (*rfp_buf_sine_sel=1, div_todig_en=0*) to drive the reference divider. In such a case the delta sigma modulator is not normally used, however if we wish to test the effects of the digital power supply isolation, we could input a 2nd reference source on the square wave input, enable its buffer (*rfp_buf_sq_en=1*), and enable the 2nd crystal to clock the unused delta sigma modulator (*sqr_todig_en=1* and *dsm_xref_sin_select=0*). This would allow the square wave clock to be set independently of the locked integer mode VCO, and hence measure the coupling of the digital to the sidebands of the VCO at various frequencies. Such a test can help in identifying and debugging grounding and layout issues in the application circuit related to the digital portion of the PCB should they occur. In general it is recommended to follow the suggested layout closely to avoid any such problems.

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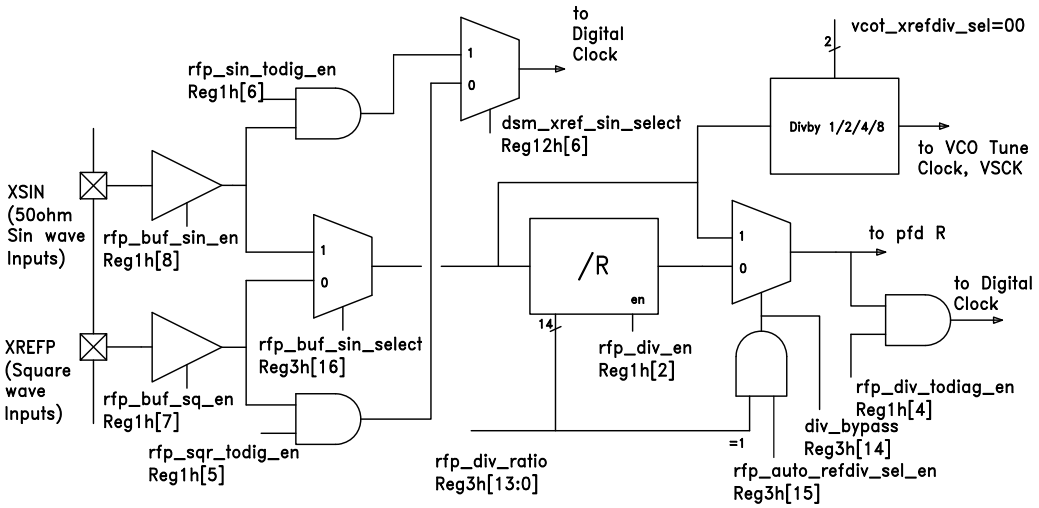

Figure 4. Reference Path Block Diagram

VCO Path

The RF path from the VCO to the phase detector, is referred to as the VCO path. The VCO path consists of an input isolation buffer and a multi-modulus prescaler, or simply the N divider. The N divider is controlled by the fractional modulator. This path operates with inputs directly from the external VCO.

RF Input Stage

The synthesizer RF input stage routes the external VCO to the phase detector via a 16-bit fractional divider. The input is protected by ESD diodes as shown in Figure 5.

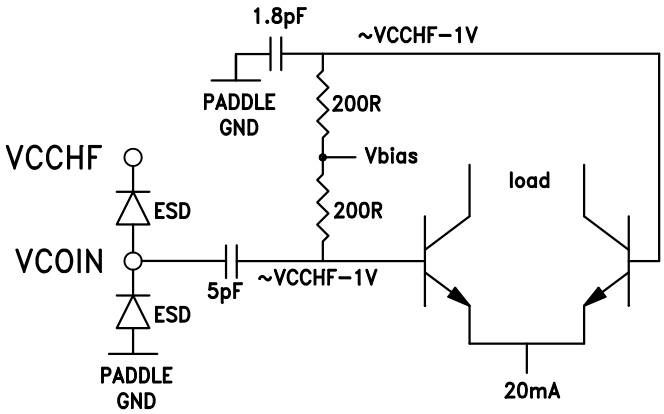

Figure 5. RF Input Stage

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RF Path 'N' Divider

The main RF path divider including a fixed divide-by-2, is capable of average divide ratios of even numbers between 131,062 and 72 in fractional mode, and 131,070 to 64 in integer mode. The reason for the difference between integer and fractional modes is that the fractional divider actually divides by up to ±4 from the average divide number. Actual division ratios when used with a given VCO will depend upon the reference frequency used and the desired output band.

General Purpose Output (GPO) Interface

The HMC702LP6CE features a 3-wire General Purpose Output (GPO) interface. GPO registers are described in *Reg1Bh* Table 32. The GPO is a flexible interface that supports a number of different functions and real time waveform access including:

a. General Data Output from SPI register gpo_sel_0_data *(gpo_sel=0)*

b. Prescaler & reference path outputs *(gpo_sel=1)*

c. Lock Detect Windows *(gpo_sel=2)*

d. Anti-cycle Slip waveforms *(gpo_sel=3)*

e. Internal synchronized frac strobe with clocks *(gposel=4)*

f. ΔΣ Modulator Phase Accumulator *(gposel=6)*

g. Auxiliary oscillators *(gposel=7)*

h. Multiple VCO Control, Latch Enables *(gposel=9)*

i. ΔΣ Modulator Outputs *(gposel=10)*

General Data to GPO *(gpo_sel=0)*

Setting register *gpo_sel=0 in* Table 32 assigns the 3-bit data from register *gpo_sel_0_data Reg1B<6:4>* to the GPO bus.

Prescaler and Reference Path Outputs *(gpo_sel = 1)*

Setting register *gpo_sel=1* (*Reg1B<3:0>* Table 32) results in the input crystal being buffered out to GPO3 as shown in Figure 6. This is useful for example to generate a copy of the input crystal signal to drive other circuits in the application, while at the same time isolating the noisy circuits from the sensitive crystal output. Often only the synthesizer requires very low phase noise from the crystal, hence it is desirable to isolate other circuits from the crystal itself and allow the synthesizer sole use of the low phase noise crystal.

gpo_sel=1 also routes the 250 MHz 14-bit reference path divider to GP02 and the 16-bit 14 GHz VCO path prescaler output to GP01. This option allows the synthesizer to function as a stand alone fractional or integer prescaler and provides visibility into the prescaler and reference path timing for sensitive applications.

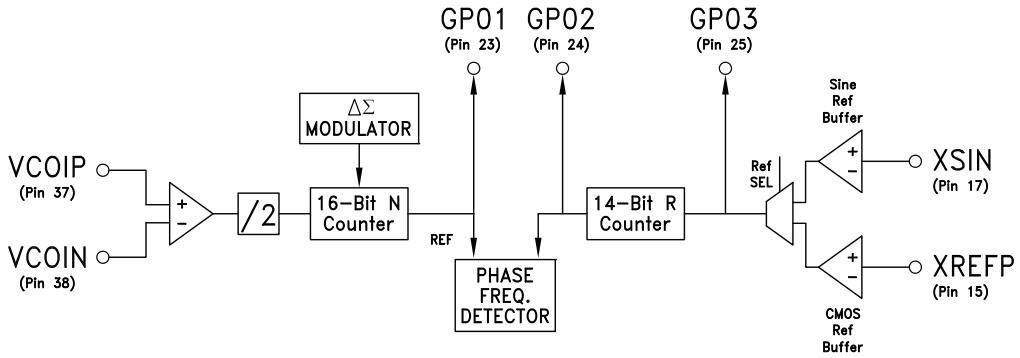

Figure 6. gpo_01 Outputs

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Lock Detect Windows (gpo_sel=2)

Setting register *gpo_sel = 2* (*Reg1Bh<3:0>* Table 32) results in the lock detect window (Figure 12) and the phase frequency detector UP and DN output control signals (Figure 15) to be routed to pins GPO1, GPO3 and GPO2 respectively. This option gives insight into the Lock Detection Process and could allow the synthesizer to be used with an external charge pump.

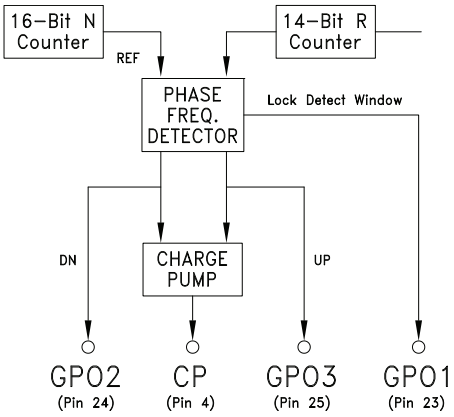

Figure 7. gpo_02 Outputs

Anti-cycle Slip Waveforms (gpo_sel = 3)

Setting register *gpo_sel=3* (*Reg1Bh<3:0>* Table 32) gives visibility into the anti-cycle slipping function of the PFD as described in section *Cycle Slip Prevention* (CSP). Three waveforms, reference path freq > VCO path freq, vco path freq > ref path freq, and a PFD strobe which holds the PFD at maximum gain, are routed to GPO3, GPO2, and GPO1 respectively. These lines will be active during frequency pull-in and will indicate instantaneously which signal, reference or vco path is greater in frequency. The PFD strobe gives insight into when the PFD is near maximum gain at 2π. The PFD strobe will be active until the VCO pulls into lock.

Internal Synchronized Frac strobe with clocks (gpo_sel= 4)

Setting register *gpo_sel=4* in (*Reg1Bh<3:0>* Table 32) gives visibility into the internally synchronized strobe that is generated when commanding a frequency change by writing to the frac register. The internal strobe initiates the update to the fractional modulator. The internal frac strobe, the ref path divider output and the sine reference input are buffered out to GPO1, GPO2 and GPO3 respectively as shown in Figure 8. In this mode, GPO1 may be used to trigger an external instrument when doing frequency hopping tests for example.

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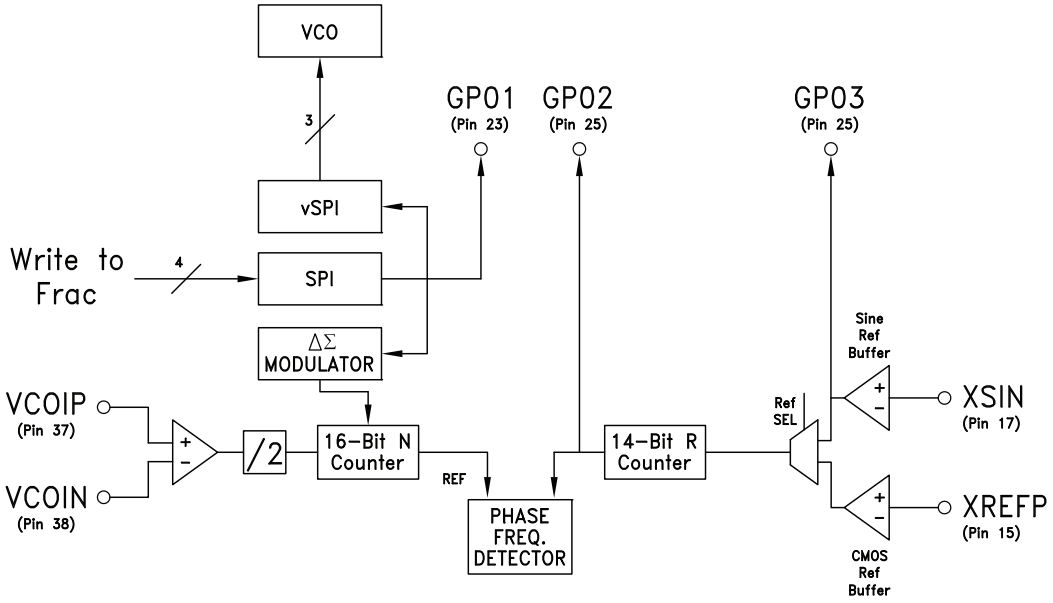

Figure 8. gpo_04 Outputs

Δ∑ ***Modulator Phase Accumulator*** *(gpo_sel=6)*

Setting register *gpo_sel=6* (*Reg1Bh<3:0>* Table 32) assigns the three msb's of the delta sigma modulator first accumulator to GPO<3:1> , where GPO3 is the msb. This feature provides insight into the phase of the VCO.

Auxiliary Oscillators *(gpo_sel=7)*

Setting register *gpo_sel=7* (*Reg1Bh<3:0>* Table 32) assigns an auxiliary clock, an internal ring oscillator, and the internal sigma delta clock to GPO3, 2, 1 respectively. The control of the auxiliary clock is determined by Reg18h Table 29 and *Reg19h* Table 30. In general terms, this highly flexible clock source allows the selection of one of the various VCO or crystal related clocks inside the synthesizer or the selection of a flexible unstabilized auxiliary ring oscillator clock. Any of the sources may be routed out via gpo_sel=7. Additional *Reg18h* Table 29 clock controls allow the aux clock to be delayed by a variable amount *(auxclk_modesel Reg18h<3:2>)*, or to be divided down by even values from 2 to 14 *(auxclk_divsel Reg18h<6:4>)*.

Δ∑ ***Modulator Outputs*** *(gpo_sel=10)*

Setting register *gpo_sel=10* (*Reg1B<3:0>* Table 32) assigns the three lsb's of the delta sigma modulator output to GPO<3:1>, where GPO1 is the lsb. This feature allows the possibility of using the HMC702LP6CE as a general purpose digital delta sigma modulator for many possible applications.

External VCO

The HMC702LP6CE is targeted for ultra low phase noise applications with an external VCO. The synthesizer has been designed to work with VCOs that can be tuned nominally over 0.5 to 4.5 Volts on the varactor tuning port with a +5V charge pump supply voltage. Slightly wider ranges are possible with a +5.5V charge pump supply or with slightly degraded performance.

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External VCO with Active Inverting OpAmp Loop Filter

An external opamp active filter is required to support external VCOs with tuning voltages above 5V. If an inverting opamp is used with a positive slope VCO, phase_sel Reg05h <0> = 1 Table 11 must be set to invert the PFD phase polarity and obtain correct closed loop operation.

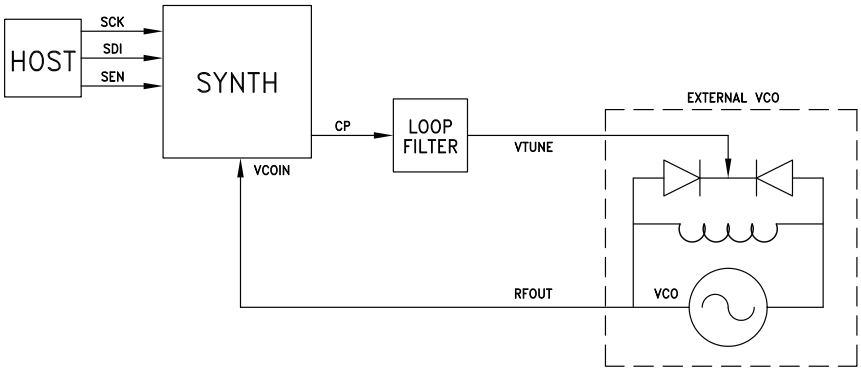

Figure 9. Conventional Synthesizer with VCO

Temperature Sensor

The HMC702LP6CE features a built in temperature sensor which may be used as a general purpose temperature sensor.

The temperature sensor is enabled via *tsens_spi_enable* (*Reg1Eh=1* Table 35) and when enabled draws 2 mA. The temperature sensor features a built in 3-bit quantizer that allows the temperature to be read in register *tsens_temperature* (*Reg21h* Table 38). The temperature sensor data converter is not clocked. Updates to the temperature sensor register are made by strobing register *tsens_spi_strobe* (Reg00h<3> Table 6). The 3-bit quantizer operates over a -40°C to +100°C range as follows:

Tn = floor {(Temperature +40) / 17.5 where T_n is the decimal value of register *tsens_temperature}* (EQ 7)

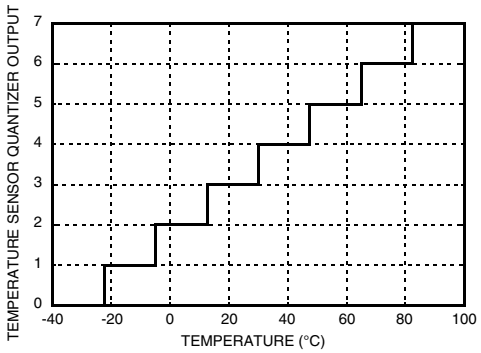

Figure 10. Typical Temperature Sensor Quantizer output

Temperature sensor slope is 17.5 mV/lsb. Absolute tolerances on the temperature sensor thresholds may vary by up to ±10°C worst case.

Nominal temperature is given by:

$$Temperature = 17.5T_n - 31.25 \pm 8.75 \quad (^{o}C) \qquad \text{(EQ 8)}$$

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Charge Pump & Phase Frequency Detector (PFD)

The Phase Frequency Detector or PFD has two inputs, one from the reference path divider and one from the VCO path divider. The PFD compares the phase of the VCO path signal with that of the reference path signal and controls the charge pump output current as a linear function of the phase difference between the two signals. The output current varies linearly over a full ±2π radians input phase difference.

PFD Functions

phase_sel (*Reg05h<0>* Table 11) inverts the phase detector polarity for use with an inverting opamp or negative slope VCO

upout_en in *Reg05h<1>* Table 11 allows masking of the PFD up output, which effectively prevents the charge pump from pumping up.

dnout_en in *Reg05h<2>* Table 11 allows masking of the PFD down output, which effectively prevents the charge pump from pumping down.

Charge Pump Tri-State

De-asserting both *upout_en* and *dnout_en* effectively tri-states the charge pump while leaving all other functions operating internally.

PFD Jitter & Lock Detect Background

In normal phase locked operation the divided VCO signal arrives at the phase detector in phase with the divided crystal signal, known as the reference signal. Despite the fact that the device is in lock, the phase of the VCO signal and the reference signal vary in time due to the phase noise of the crystal and VCO oscillators, the loop bandwidth used and the presence of fractional modulation or not. The total integrated noise on the VCO path normally dominates the variations in the two arrival times at the phase detector if fractional modulation is turned off.

If we wish to detect if the VCO is in lock or not we need to distinguish between normal phase jitter when in lock and phase jitter when not in lock.

First, we need to understand what is the jitter of the synthesizer, measured at the phase detector in integer or fractional modes.

The standard deviation of the arrival time of the VCO signal, or the jitter, in integer mode may be estimated with a simple approximation if we assume that the locked VCO has a constant phase noise, $\Phi^2(f_0)$, at offsets less than the loop 3 dB bandwidth and a 20 dB per decade roll off at greater offsets. The simple locked VCO phase noise approximation is shown on the left of Figure 11.

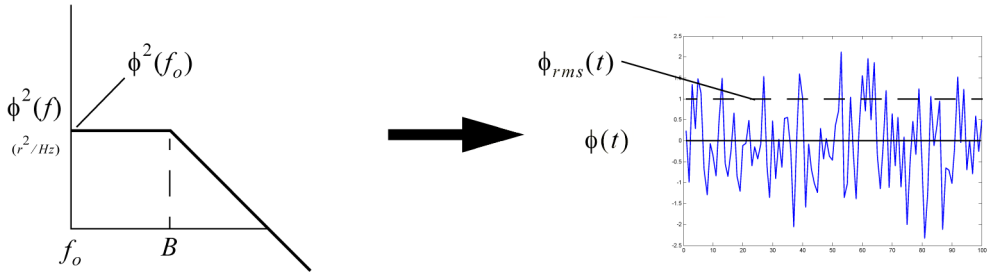

Figure 11. Synthesizer Phase Noise & Jitter

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With this simplification the single sideband integrated VCO phase noise, Φ^2 , in rads^2 at the phase detector is given by

$$\phi_{SSB}{}^2 = \left(\phi^2(f_o)B\frac{\pi}{2}\right)/N^2 \qquad \text{(EQ 9)}$$

where

$\Phi^2{}_{SSB}(f_0)$ is the single sideband phase noise in rads^2/Hz inside the loop bandwidth, B is the 3 dB corner frequency of the closed loop PLL and N is the division ratio of the prescaler

The rms phase jitter of the VCO in rads, Φ , results from the power sum of the two sidebands:

$$\Phi = \sqrt{2\Phi^2{}_{SSB}} \qquad \text{(EQ 10)}$$

Since the simple integral of (EQ 9) is just a product of constants, we can easily do the integral in the log domain. For example if the VCO phase noise inside the loop is -100 dBc/Hz at 10 kHz offset and the loop bandwidth is 100 kHz, and the division ratio N=100, then the integrated single sideband phase noise at the phase detector in dB is given by $\Phi^2{}_{dB} = 10\log(\Phi^2(f_0)B\pi/N^2) = -100 + 50 + 5 - 40 = -85$ dBrads, or equivalently $\Phi = 10^{-82/20} = 56$ urads rms or 3.2 milli-degrees rms.

While the phase noise reduces by a factor of 20logN after division to the reference, the jitter is a constant.

The rms jitter from the phase noise is then given by $T_{jnp} = T_{ref}\,\Phi / 2\pi$

In this example if the reference was 50 MHz, T_{ref} = 20 nsec, and hence T_{jpn} = 178 femto-sec.

A normal 3 sigma peak-to-peak variation in the arrival time therefore would be

$$\pm 3\sqrt{2}T_{jpn} = 0.756\ ps$$

If the synthesizer was in fractional mode, the fractional modulation of the VCO divider will dominate the jitter. The exact standard deviation of the divided VCO signal will vary based upon the modulator chosen, however a typical modulator will vary by about ±3 VCO periods, ±4 VCO periods, worst case.

If, for example, a nominal VCO at 5 GHz is divided by 100 to equal the reference at 50 MHz, then the worst case division ratios will vary by 100±4. Hence the peak variation in the arrival times caused by $\Delta\Sigma$ modulation of the fractional synthesizer at the reference will be

$$T_{j\Delta\Sigma pk} = \pm T_{vco}\cdot(N_{max} - N_{min})/2 \qquad \text{(EQ 11)}$$

PFD Jitter and Lock Detect Background *(Continued)*

In this example, $T_{j\Delta\Sigma pk}$ = ±200 ps(108-92)/2 = ±1600 psec. If we note that the distribution of the delta sigma modulation is approximately gaussian, we could approximate $T_{j\Delta\Sigma pk}$ as a 3 sigma jitter, and hence we could estimate the rms jitter of the $\Delta\Sigma$ modulator as about 1/3 of $T_{j\Delta\Sigma pk}$ or about 532 psec in this example.

Hence the total rms jitter T_j, expected from the delta sigma modulation plus the phase noise of the VCO would be given by the rms sum , where

$$T_j = \sqrt{T_{jpn}^2 + \left(\frac{T_{j\Delta\Sigma pk}}{3}\right)^2} \qquad \text{(EQ 12)}$$

In this example the jitter contribution of the phase noise calculated previously would add only 0.764psec more jitter at the reference, hence we see that the jitter at the phase detector is dominated by the fractional modulation.

Bottom line, we have to expect about ±1.6 nsec of normal variation in the phase detector arrival times when in fractional mode. In addition, lower VCO frequencies with high reference frequencies will have much larger variations., for example, a 1 GHz VCO operating at near the minimum nominal divider ratio of 72, would, according to (EQ 11), exhibit about ±4 nsec of peak variation at the phase detector, under normal operation. The lock detect circuit must not confuse this modulation as being out of lock.

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PFD Lock Detect

lkd_en (*Reg01h<11>* Table 7) enables the lock detect functions of the HMC702LP6CE.

The Lock Detect circuit in the HMC702LP6CE places a one shot window around the reference. The one shot window may be generated by either an analog one shot circuit or a digital one shot based upon an internal ring oscillator timer. Clearing *lkd_ringosc_mono_select* (*Reg1Ah<14>* Table 31) will result in a nominal 10nsec 'analog' window of fixed length, as shown in Figure 12. Setting *lkd_ringosc_mono_select* will result in a variable length 'digital' widow. The digital one shot window is controlled by *lkd_ringosc_cfg (Reg1Ah<16:15>* Table 31*)*. The resulting lock detect window period is then generated by the number of ring oscillator periods defined in *lkd_monost_duration Reg1Ah<18:17>* (Table 31). The lock detect ring oscillator may be observed on the GPO2 port by setting *ringosc_testmode* (*Reg1Ah<19>* Table 31) and configuring the *gpo_sel<3:0>* = 0111 in (*Reg1Bh* Table 32). Lock detect does not function when this test mode is enabled.

lkd_wincnt_max (*Reg1Ah<9:0>* Table 31) defines the number of consecutive counts of the VCO that must land inside the lock detect window to declare lock. If for example we set *lkd_wincnt_max* = 1000 , then the VCO arrival would have to occur inside the selected lock widow 1000 times in a row to be declared locked. When locked the Lock Detect flag *ro_lock_detect* (*Reg1Fh<0>* Table 36) will be set. A single occurrence outside of the window will result in clearing the Lock Detect flag, *ro_lock_detect*.

The Lock Detect flag *ro_lock_detect* (*Reg1Fh<0>* Table 36) is a read only register, readable from the serial port. The Lock Detect flag is also output to the *LD_SDO* pin according to *lkd_to_sdo_always (Reg1Ah<13>)* and *lkd_to_sdo_automux_en (Reg1Ah<12>)*, both in Table 31. Setting *lkd_to_sdo_always* will always display the Lock Detect flag on *LD_DSO*. Clearing *lkd_to_sdo_always* and setting *lkd_to_sdo_automux_en* will display the Lock Detect flag on *LD_SDO* except when a serial port read is requested, in which case the pin reverts temporarily to the Serial Data Out pin, and returns to the lock detect function after the read is completed.

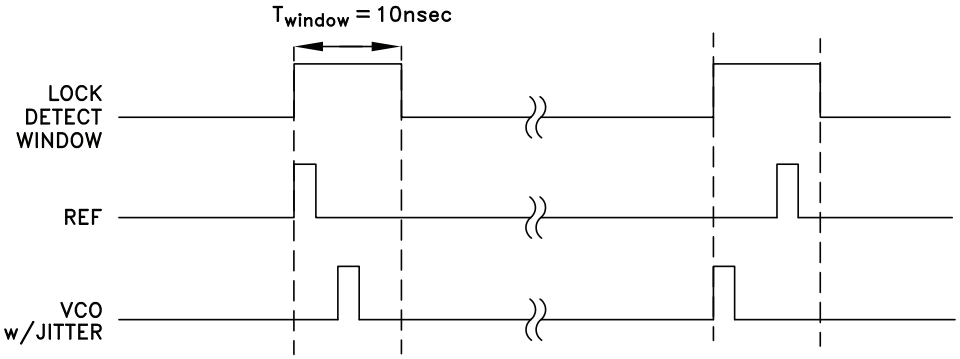

Figure 12. Normal Lock Detect Window

Lock Detect with Phase Offset

When operating in fractional mode the linearity of the charge pump and phase detector are more critical than in integer mode. The phase detector linearity is worse when operated with zero phase offset. Hence in fractional mode it is necessary to offset the phase of the reference and the VCO at the phase detector. In such a case, for example with an offset delay, as shown in Figure 13, the mean phase of the VCO will always occur after the reference. The lock detect circuit window can be made more selective with a fixed offset delay by setting *win_asym_enable* and *win_asym_up_select* (*Reg1Ah<11>* Table 31). Similarly the offset can be in advance of the reference by clearing *win_asym_up_select* while leaving *win_asym_enable Reg1Ah<10>* set both in Table 31.

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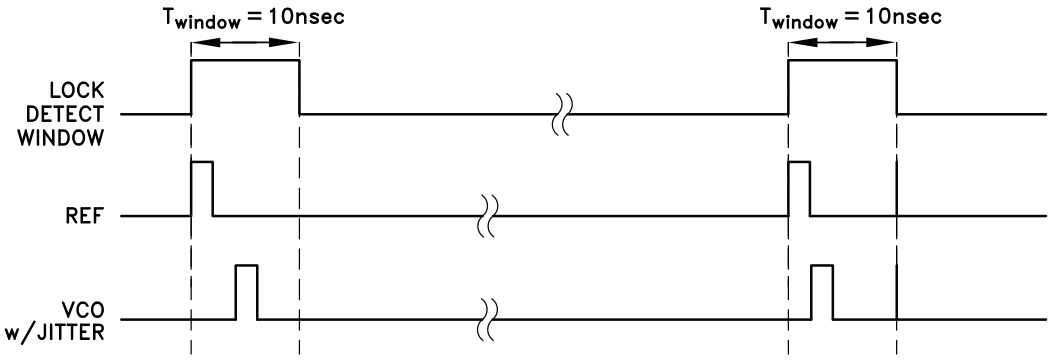

Figure 13. Delayed Lock Detect Window

For most applications the analog one shot window is sufficient. To determine the required Lock Detect one shot window size:

Required LD One Shot Window = (CP Phase Offset (ns) + 8xTvco) x 1.3.

Cycle Slip Prevention (CSP)

When changing frequencies the VCO is not yet locked to the reference and the phase difference at the PFD varies rapidly over a range much greater than ±2π radians. Since the gain of the PFD varies linearly with phase up to ±2π, the gain of conventional PFDs will cycle from high gain, when the phase difference approaches a multiple of 2π, to low gain, when the phase difference is slightly larger than a multiple of 0 radians. This phenomena is known as cycle slipping. Cycle slipping causes the pull-in rate during the locking phase to vary cyclically as shown in the red curve in Figure 14. Cycle slipping increases the time to lock to a value far greater than that predicted by normal small signal Laplace analysis.

The HMC702LP6CE PFD features Cycle Slip Prevention (CSP), an ability to virtually eliminate cycle slipping during acquisition. When enabled, the CSP feature essentially holds the PFD gain at maximum until such time as the frequency difference is near zero. CSP allows significantly faster lock times as shown inFigure 14. The use of the CSP feature is enabled with *pfds_rstb* (*Reg01<15>* Table 7). The CSP feature may be optimized for a given set of PLL dynamics by adjusting the PFD sensitivity to cycle slipping. This is achieved by adjusting *pfds_sat_deltaN* (*Reg1C<3:0>* Table 33).

CSP will cause the VCO N divider to momentarily divide by a higher or lower N value in order to pull the divided VCO phase back towards the reference edge. The maximum recommended VCO N divider deviation is no more than 20% of the target N value programmed into Register F. For example, if N=50 for the target frequency, then the CSP Magnitude should be 10 or less so Register 1Ch Bits [3:0] would be programmed to Ah.

In situations where the target N value is low, for example 36 the CSP behavior will be compromised because the minimum VCO divide value is 32.

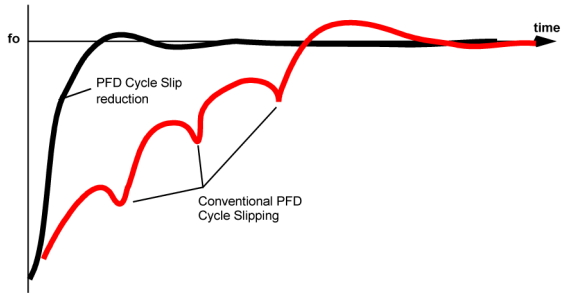

Figure 14. Cycle Slip Prevention (CSP)

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Charge Pump Gain

A simplified diagram of the charge pump is shown in Figure 15. Charge pump up and down gains are set by *cp_UPcurrent_sel* and *cp_DNcurrent_sel* respectively (*Reg07* Table 13). Normally the registers are set to the same value. Each of the UP and DN charge pumps consist of 5-bit charge pumps with lsb of 125 µA. The current gain of the pump, in Amps/radian, is equal to the gain setting of this register divided by 2π.

For example if both *cp_UPcurrent_sel* and *cp_DNcurrent_sel* are set to '01000' the output current of each pump will be 1mA and the gain *Kp* = 1mA/2π radians, or 159 uA/rad.

Charge Pump Gain Trim

In most applications Gain Trim is not used. However it is available for special applications.

Each of the UP and DN pumps may be trimmed separately to more precise values to improve current source matching of the UP and DN values, or to allow finer control of pump gain.

The pump trim controls are 3-bits, binary weighted for UP and DN, in *cp_UPtrim_sel* and *cp_DNtrim_sel* respectively (Reg 08h Table 14). LSB weight is 14.7 uA, x000 = 0 trim, x001 = 14.7 ua added trim, x111 = 100uA.

Charge Pump Phase Offset

Either of the UP or DN charge pumps may have a DC leakage or "offset" added. The leakage forces the phase detector to operate with a phase offset between the reference and the divided VCO inputs. It is recommended to operate with a phase offset when using fractional mode to reduce non-linear effects from the UP and DN pump mismatch. Phase noise in fractional mode is strongly affected by charge pump offset.

DC leakage or "offset" may be added to the UP or DN pumps using *cp_UPoffset_sel* and *cp_DNoffset_sel* (*Reg08* Table 14). These are 4 bit registers with 28.7uA LSB. Maximum offset is 430uA.

As an example, if the main pump gain was set at 1mA, an offset of 373uA would represent a phase offset of about (392/1000)*360 = 133 degrees. For best spectral performance in Fractional Mode the leakage current should be programmed to:

Required Leakage Current (µA) = (2.5E-9 + 8xTvco) x Fcomparison (Hz) x CP current (µA)

CP Offset Leakage Current should never exceed 25% of the programmed CP current.

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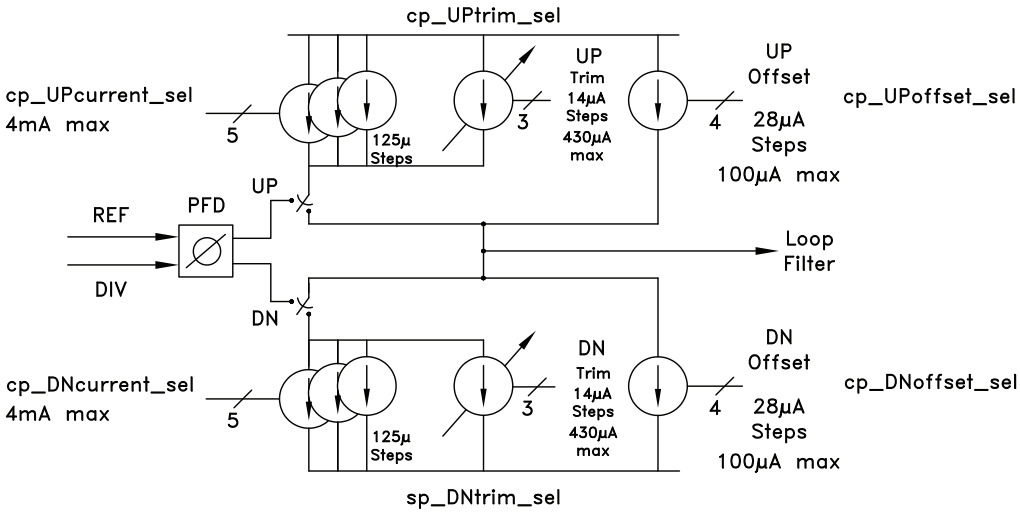

Figure 15. Charge Pump Gain, Trim and Phase Offset Control

Frequency Programming

The HMC702LP6CE can operate in either fractional mode or integer mode. In integer mode of operation the delta sigma modulator is disabled. Frequency programming and mode control is described below.

Fractional Frequency

The fractional frequency synthesizer, when operating in fractional mode, can lock to frequencies which are fractional multiples of the reference frequency.

Fractional mode is the default mode. To run in fractional mode ensure that *dsm_integer_mode* Reg12h<3> Table 24 is clear and *dsm_rstb* is set Reg01<13> Table 7. Then program the frequency as explained below:

The output frequency of the synthesizer is given by, f_{vco}, where

Fractional Frequency of VCO

$$f_{vco} = \frac{f_{xtal}}{R} 2N_{int} + \frac{f_{xtal} \cdot N_{frac}}{R \cdot 2^{23}} = f_{int} + f_{frac} \quad \text{(EQ 13)}$$

where

N_{int}	is the integer division ratio, an integer number between 36 and 65,533 (*dsm_intg* (*Reg0Fh* Table 21))
N_{frac}	is the fractional part, a number from 1 to 2^{24} (*dsm_frac Reg10h* Table 22)
R	is the reference path division ratio, (*rfp_div_ratio Reg03h<13:0>* Table 9)
f_{xtal}	is the frequency of the crystal oscillator input (XSIN or XREF Figure 4)

As an Example:

f_{xtal}	= 50 MHz
R	= 1
f_{ref}	= 50 MHz

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N_{int} = 92
N_{frac} = 1

$$f_{vco} = \frac{50e6}{1} 92 \cdot 2 + \frac{50e6 \cdot 1}{1 \cdot 2^{23}} 9.2\ GHz + 5.96\ Hz \quad \text{(EQ 14)}$$

In this example the output frequency of 9,600,000,005.96 Hz is achieved by programming the 16-bit binary value of 92d = 5C = 0000 0000 0101 1100 into *dsm_intg*.

Similarly the 24-bit binary value of the fractional word is written into *dsm_frac*,

1d = 000 001h = 0000 0000 0000 0000 0000 0001

Example 2: Set the output to 12.600 025 GHz using a 100 MHz reference, R=2.

Find the nearest integer value, N_{int}, N_{int} = 126, f_{int} = 12.600 000 GHz

This leaves the fractional part to be f_{frac} =25 kHz

$$N_{frac} = \frac{2^{23} \cdot R \cdot f_{frac}}{f_{xtal}} = \frac{2^{23} \cdot 2 \cdot 25e3}{100e6} = 4194.304 \quad \text{(EQ 15)}$$

Since N_{frac} must be an integer number, the actual fractional frequency will be 24,998.19 Hz, an error of 1.81 Hz.

Here we program the 16-bit N_{int} = 126d = 7Eh = 0000 0000 0111 1110 and

the 24-bit N_{frac} = 4194d = 1062h = 0000 0100 0001 0010

In addition to the above frequency programming words, the fractional mode must be enabled using the frac register. Other DSM configuration registers should be set to the recommended values. Register setup files are available on request.

Integer Frequency

The synthesizer is capable of operating in integer mode. In integer mode the digital ΔΣ modulator is normally shut off and the division ratio of the VCO divider is set at a fixed value. To run in integer mode set *dsm_integer_mode* (*Reg12h<3>* Table 24) and clear *dsm_rstb* (*Reg01h<13>* Table 7). Then program the integer portion of the frequency, N_{INT}, as explained by (EQ 13), ignoring the fractional part.

Frequency Hopping Trigger

If the synthesizer is in fractional mode, a write to the fractional frequency register, *Reg10h* Table 22, will initiate the frequency hop on the falling edge of the 31st clock edge of the serial port write (see Figure 19).

If the integer frequency register, *Reg0Fh* Table 21, is written when in fractional mode the information will be buffered and only executed when the fractional frequency register is written.

If the synthesizer is in integer mode, a write to the integer frequency register, *Reg0Fh* Table 21, will initiate the frequency hop on the falling edge of the 31st clock edge of the serial port write (see Figure 19).

Power On Reset (POR)

Normally all logic cells in the HMC702LP6CE are reset when the device digital power supply, DVDD, is applied. This is referred to as Power On Reset, or just POR. POR normally takes about 500us after the DVDD supply exceeds 1.5V, guaranteed to be reset in 1msec. Once the DVDD supply exceeds 1.5V, the POR will not reset the digital again unless the supply drops below 100mV.

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Soft Reset

The SPI registers may also be soft reset by an SPI write to strobe *global_swrst_regs* (*Reg00h<0>* Table 6).

All other digital, including the fractional modulator, may be reset with an SPI write to strobe *global_swrst_dig (Reg00h<1>* Table 6).

Hardware Reset

The SPI registers may also be hardware reset by holding RSTB, pin 19, low.

Power Down

The HMC702LP6CE may be powered down by writing a zero to *Reg01h* Table 7. In power down state the HMC702LP6CE should draw less than 10uA. It should be noted that *Reg01h* is the Enable and Reset Register which controls 16 separate functions in the chip. Depending upon the desired mode of operation of the chip, not all of the functions may be enabled when in operation. Hence power up of the chip requires a selective write to *Reg01* bits. An easy way to return the chip to its prior state after a power down is to first read *Reg01h* and save the state, then write a zero to *Reg01h* for reset and then simply rewrite the previous value to restore the chip to the desired operating mode.

CW Sweeper Mode

The HMC702LP6CE features a built in frequency sweeper function. This function supports external or automatic triggered sweeps. The maximum sweep range is limited to 510 x Fxtal/R. For example, with a 10 MHz comparison frequency, the maximum sweep range is 5100 MHz. The start and end frequency points must be within 5100 MHz of one another. For sweep operation the Delta-Sigma Modulator mode should be Feed Forward (Register 12h Bits [9:8] = 11) otherwise discontinuities may occur when crossing integer-N boundaries (harmonic multiples of the comparison frequency).

Sweeper Modes include:

a. 2-Way Sweep Mode: alternating positive and negative frequency ramps.

b. 1-Way Sweep Mode

c. Single Step Ramp Mode

Applications include test instrumentation, FMCW sensors, automotive radars and others. The parameters of the sweep function are illustrated in Figure 16.

CW Sweeper Mode *(Continued)*

The sweep generator is enabled with *ramp_enable* in (*Reg14h<1>* Table 25). The sweep function cycles through a series of discrete frequency values, which may be

a. Stepped by an automatic sequencer, or

b. Single stepped by individual triggers in Single Step Mode.

Triggering of each sweep, or step, may be configured to operate:

a. Via a serial port write to *Reg14h<2> ramp_trigg* (if Reg 14h<2> = 0)

b. Automatically generated internally,

c. Triggered via TTL input on GPO3 Reg14h<5> = 1.

Sweep parameters are set as follows:

Initial Frequency, f_o = Current frequency value of the synthesizer, (EQ 15)

Final Frequency, f_f = Frequency of the synthesizer at the end of the ramp

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The frequency step size while ramping is controlled by *rampstep*, (*Reg15h* Table 26).

Frequency Step Size $\Delta f_{step} = rampstep \bullet f_{xtal} / 2^{23} \bullet R$

where R is the value of the reference divider (*rfp_div_ratio in* Table 9)

Clearing or setting *ramp_startdir_dn*, (*Reg14h<4>* Table 25), sets the initial ramp direction to be increasing or decreasing in frequency respectively. Setting *ramp_singledir* (*Reg14h<7>* Table 25), restricts the direction of the sweep to the initial sweep direction only.

The sweeper timebase T_{ref} is the period of the divided reference, f_{PFD}, at the phase detector T_{ref}

The total number of ramp steps taken in a single sweep is given by ramp_steps_number in Reg16h Table 27.

The total time to ramp from f_o to f_f is given by $T_{ramp} = T_{ref} \bullet ramp_steps_number$

The final ramp frequency, f_f, is given by $f_f = f_i + \Delta f_{step} \bullet ramp_steps_number$

Sweeper action at the end of sweep depends upon the mode of the sweep:

a. With both *ramp_singledir* and *ramp_repeat_en* disabled, at the end of the ramp time, T_{ramp}, the sweeper will dwell at the final frequency f_f, until a new trigger is received. The next trigger will reverse the current sequence, starting from f_f, and stepping back to f_o. Odd triggers will ramp in the same direction as the initial ramp, even triggers will ramp in the opposite direction.

b. with *ramp_singledir* enabled and *ramp_repeat_en* disabled, at the end of the ramp time, T_{ramp}, the sweeper will dwell at the final frequency f_f, until a new trigger is received. The second trigger will hop the synthesizer back to the initial frequency, f_o. The third trigger will restart the sweep from f_o. Hence all odd numbered triggers will start a new ramp in the same direction as the initial ramp, even numbered triggers will hop the synthesizer from the current frequency to f_o , where it will wait for a trigger to start a sweep.

Ramp Busy

In all types of sweeps *ramp_busy* will indicate an active sweep and will stay high between the 1st and nth ramp step. *ramp_busy* may be monitored one of two ways. *ramp_busy* is readable via read only register *Reg1Fh<5>* Table 36.

ramp_busy may also be monitored on GPO2, hardware pin 24, by setting *Reg1Bh<3:0> =8h* Table 32.

Autosweep Mode

The Autosweep mode is similar to Figure 16 except that once started, triggers are not required. Once enabled, (*ramp_repeat_en=1 Reg14h<3>* Table 25) the Autosweep mode initiates the first trigger, steps n times, one step per ref clock cycle, and then waits for the programmed dwell period and automatically triggers the ramp in the opposite direction. The sweep process continues alternating sweep directions until disabled. *dwell_time* (*Reg17h* Table 28) controls the number of T_{ref} periods to wait at the end of the ramp before automatically retriggering a new sweep.

2-Way Sweeps

If *ramp_repeat_en* (*Reg14h<3>* Table 25) is cleared, then the ramps are triggered by

a. Writing to *ramp_trigg* (*Reg14h<2>* Table 25), if bit <2> = 0, or

b. by rising edge TTL signal input on GPO3, if *ramp_trig_ext_en* is set, and GPO3 is enabled.

All functions are the same in Figure 16 for Autosweep or 2-Way Triggered sweeps, the only difference is the trigger source is generated internally for autosweep, and is input via serial port or GPO3 for triggered sweeps. *Sweep_busy* will go high at the start of every ramp and stay high until the nth step in the ramp.

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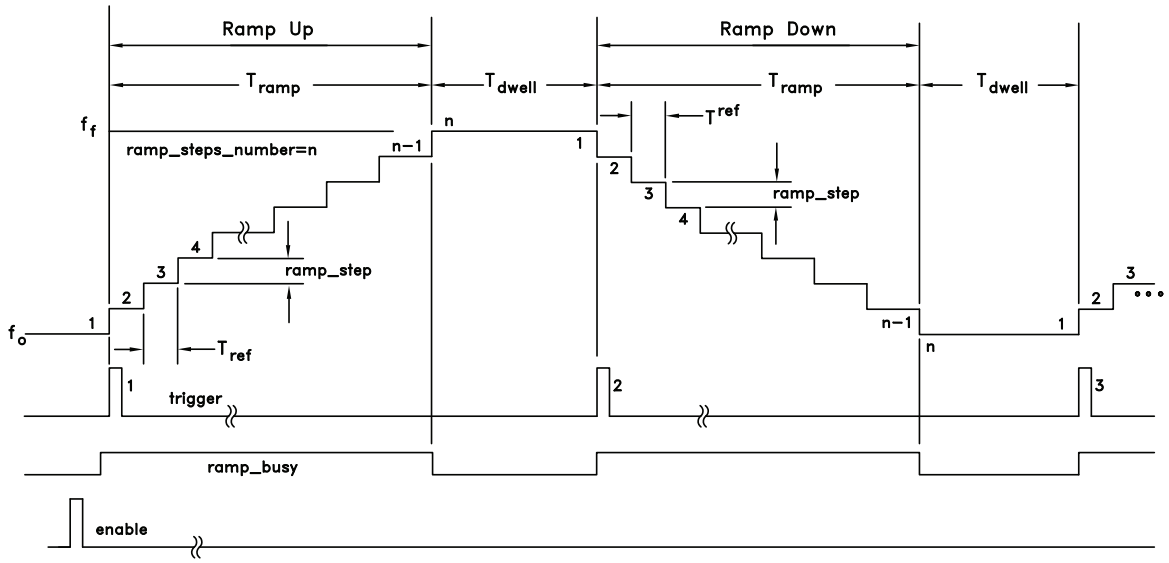

Figure 16. 2-Way Sweep Control via Trigger

Triggered 1-Way Sweeps

1-Way sweeps are shown in Figure 17.

Unlike 2-Way sweeps, 1-Way sweeps require that the VCO hop back to the start frequency after the dwell period. Triggered 1-Way sweeps also require a 3rd trigger to start the new sweep. The 3rd trigger must be timed appropriately to allow the VCO to settle after the large frequency hop back to the start frequency. Subsequent odd numbered triggers will start the 1-Way sweep and repeat the process.

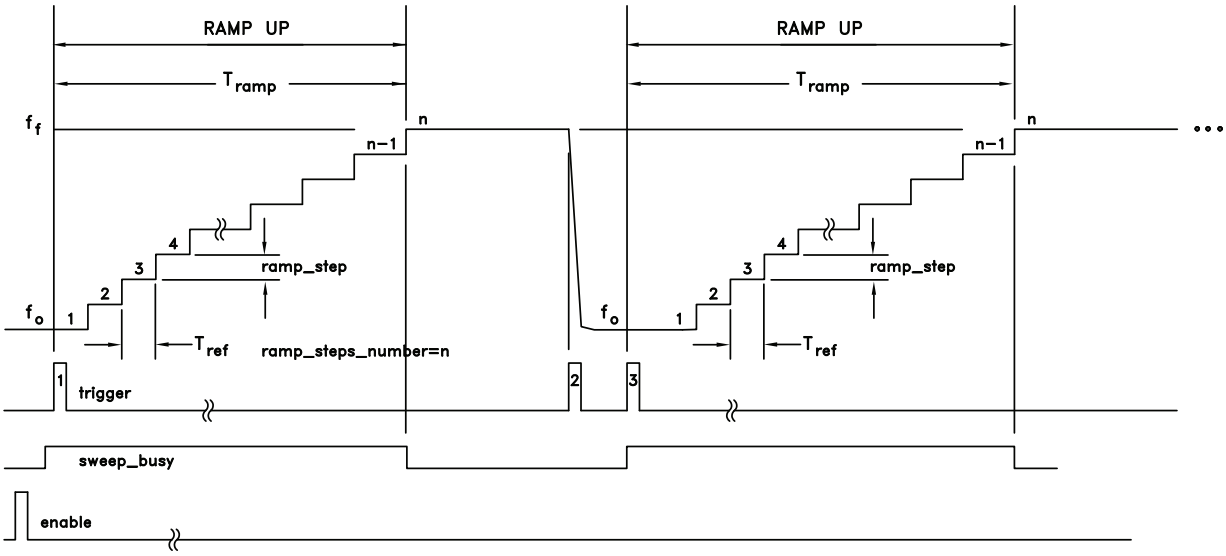

Figure 17. 1-Way Sweep Control

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Single Step Ramp Mode

A Single Step 1-Way Ramp is shown in Figure 18. In this mode, a trigger is required for each step of the ramp. Single step will function in either 1-Way or 2-Way ramps. Similar to autosweep, the ramp_busy flag will go high on the first trigger, and will stay high until the nth trigger. The n+1 trigger will cause the ramp to jump to the start frequency in 1-way ramp mode. The n+2 trigger will restart the 1-way ramp.

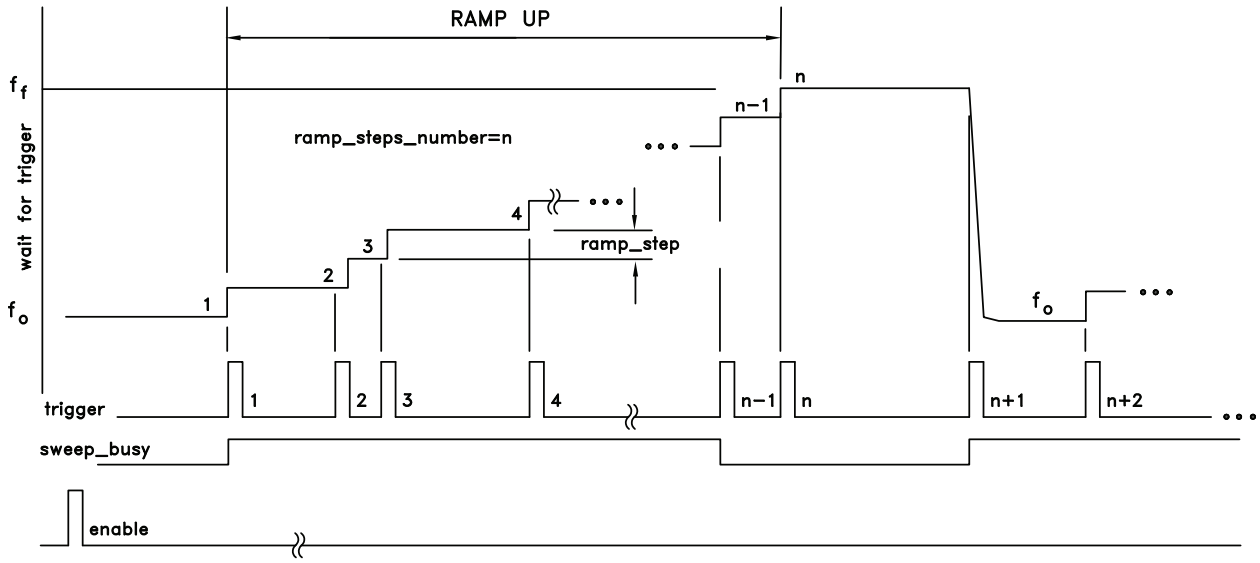

Figure 18. Single Step Ramp Mode

The user should be aware that the synthesized ramp is subject to normal phase locked loop dynamics. If the loop bandwidth in use is much wider than the rate of the steps then the locking will be very fast and the ramp will have a staircase shape. If the update rate is higher than the loop bandwidth, as is normally the case, then the loop will not fully settle before a new frequency step is received. Hence the swept output will have a small lag and will sweep in a near continuous fashion.

MAIN SERIAL PORT

The HMC702LP6CE features a four wire serial port for simple communication with the host controller. Register types may be Read Only, Write Only, Read/Write or Strobe, as described in the registers descriptions. The synthesizer also features an auxiliary 3-wire serial port, known as the VCO Serial Port. The VCO Serial Port is a write only interface from the synthesizer to an optional switched resonator VCO that supports 3-wire serial port control.

Typical main serial port operation can be run with SCLK at speeds up to 50 MHz. Serial port registers are described in the section REGISTER MAP.

LD_SDO Pin Operation

Configuration of the LD_SDO pin requires manipulation of both Reg2h[1:0] and Reg1Ah[13:12], as follows:

Serial data output (SDO) when a serial read occurs and high impedance at all other times:
Reg2h[1:0] = 0x (x=don't care)
Reg1Ah[13:12] = 0x (x=don't care)

Serial data output (SDO) when a serial read occurs and LD status at all other times (LD_SDO pin automatically mux'ed between LD and SDO):
Reg2h[1:0] = 11
Reg1Ah[13:12] = 01

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LD status always:
Reg2h[1:0] = 11
Reg1Ah[13:12] = 01

High impedance always:
Reg2h[1:0] = 10
Reg1Ah[13:12] = xx (x=don't care)

Serial Port WRITE Operation

AVDD = DVDD = 3V ±10%, AGND = DGND = 0V

Table 4. Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SEN to SCLK setup time	8			nsec
t_2	SDI to SCLK setup time	10			nsec
t_3	SDI to CLK hold time	10			nsec
t_4	SCLK high duration	8			nsec
t_5	SCLK low duration	8			nsec
t_6	SEN High duration	640			nsec
t_7	SEN low duration	20			nsec

A typical WRITE cycle is shown in Figure 19.

a. The Master (host) both asserts SEN (Serial Port Enable) and clears SDI to indicate a WRITE cycle, followed by a rising edge of SCLK.

b. The slave (synthesizer) reads SDI on the 1st rising edge of SCLK after SEN. SDI low initiates the WRITE cycle (/WR)

c. Host places the six address bits on the next six falling edges of SCLK, MSB first.

d. Slave registers the address bits in the next six rising edges of SCLK (2-7).

e. Host places the 24 data bits on the next 24 falling edges of SCK, MSB first .

f. Slave registers the data bits on the next 24 rising edges of SCK (8-31).

g. SEN is de-asserted on or after the 32nd falling edge of SCLK.

h. The 32nd rising edge of SCLK completes the cycle

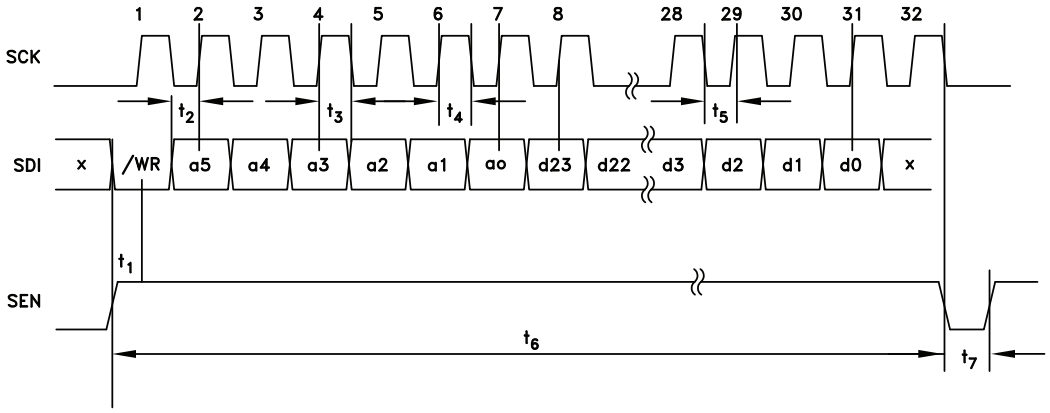

Figure 19. Serial Port Timing Diagram - WRITE

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Main Serial Port READ Operation

The synthesizer uses the multi-purpose pin, *LD_SDO*, for both Lock Detect and Serial Data Out (SDO) functions. The registers *lkd_to_sdo_automux_en (Reg1A<12>)* and *lkd_to_sdo_always* (*Reg1A<13>* Table 31) determine how the Data Output pin is muxed with the Lock Detect function. If both of the registers are cleared, then the pin is exclusively SDO. If automux is enabled, the pin switches to SDO when the RD function is sensed on the 1st rising edge of SCLK. If *lkd_to_sdo_always* is set, then the pin *LD_SDO* is dedicated for Lock Detect only, and it is not possible to read from the synthesizer.

A typical READ cycle is shown in Figure 20.

a. The Master (host) asserts both SEN (Serial Port Enable) and SDI to indicate a READ cycle, followed by a rising edge SCLK

b. The slave (synthesizer) reads SDI on the 1st rising edge of SCLK after SEN. SDI high initiates the READ cycle (RD)

c. Host places the six address bits on the next six falling edges of SCLK, MSB first.

d. Slave registers the address bits on the next six rising edges of SCLK (2-7).

e. Slave places the 24 data bits on the next 24 rising edges of SCK (8-31), MSB first .

f. Host registers the data bits on the next 24 falling edges of SCK (8-31).

g. SEN is de-asserted on or after the 32nd falling edge of SCLK.

h. The 32nd falling edge of SCLK completes the cycle

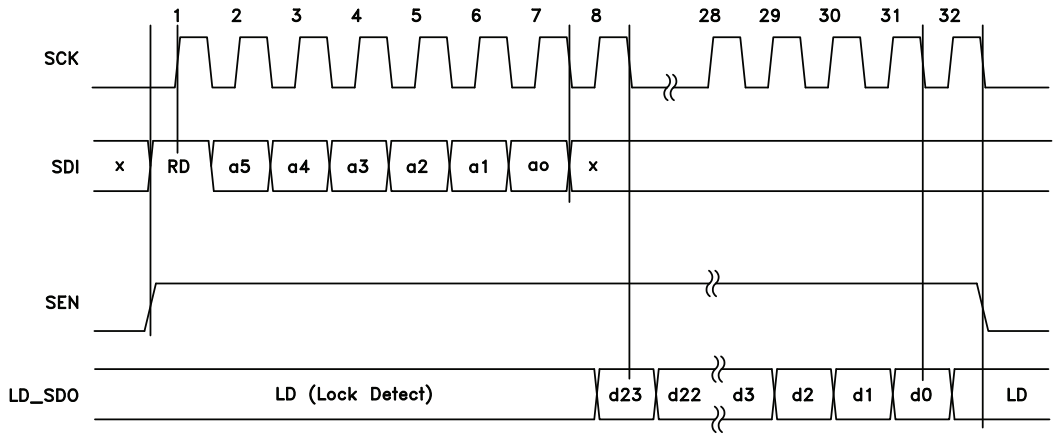

Figure 20. Serial Port Timing Diagram - READ

REGISTER MAP

Table 5. Reg 00h Chip ID (Read Only) Register

Bit	Type	Name	Width	Default	Description
[23:0]	RO	Chip ID	24	581504h	Chip ID

Table 6. Reg 00h Strobe (Write Only) Register

Bit	Type	Name	Width	Default	Description
0	STR	global_swrst_regs	1	0	Strobe to soft reset the SPI registers
1	STR	global_swrst_dig	1	0	Strobe to soft reset the rest of digital
2	STR	mcnt_resynch	1	0	Reserved
3	STR	tsens_spi_strobe	1	0	Strobe to clock the temperature measurement on demand

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Table 7. Reg 01h Enable & Reset Register

Bit	Type	Name		Default	Description
0	R/W	malg_vcobuf_en	1	1	VCO Buffer Enable
1	R/W	mag_bias_en	1	1	Bias enable. When 0 PLL is disabled.
2	R/W	rfp_div_en	1	0	Enables / Holds refdiv in reset Holding Ref divider in reset is equivalent to bypassing the divider, see Figure 4
3	R/W	xrefmux_todig_en	1	1	Enables clock gate for xtal muxed (sq or sin) reference to digital. Program 1
4	R/W	rfp_div_todig_en	1	1	Enables divided reference clock to the digital see Figure 4
5	R/W	rfp_sqr_todig_en	1	0	Enables square wave xtal clock to main digital see Figure 4 Program 0
6	R/W	rfp_sin_todig_en	1	0	Enables sine wave xtal clock to main digital see Figure 4
7	R/W	rfp_buf_sq_en	1	1	Enables Square wave Ref Buffer. Also requires Reg3h[16]=0 for Square wave Ref Buffer. See Figure 4
8	R/W	rfp_buf_sin_en	1	0	Enables Sine wave Ref Buffer also requires Reg3h[16]=1 for Sine wave Ref Buffer. See Figure 4
9	R/W	vcop_todig_en	1	1	1= Divided VCO as digital, ΔΣ modulator clock 0= Divided Ref path as the ΔΣ modulator clock Program 1
10	R/W	vcop_presc_en	1	1	Enables the prescaler bias
11	R/W	pfd_lkd_en	1	1	Enable / Resetb to digital lock detect circuit and PFD's lock detect output gates Program 1
12	R/W	cp_en	1	1	Charge Pump Enable, disable is tri-stated output
13	R/W	dsm_rstb	1	1	1 - Enables fractional modulator see also *dsm_integer_mode Reg12h<3>*
14	R/W	lkd_rstb	1	1	1 - enables lock detect circuit
15	R/W	pfds_rstb	1	1	CSP PFD FF rstb 1 - Enables the Cycle Slip Prevention (CSP) feature of the PFD (also need Reg 1C[5]=1)

Table 8. Reg 02h Serial Data Out Force Register

Bit	Type	Name	Default	Description
0	R/W	malg_sdo_driver_force_val	1	Serial Data Out Force value This value may be forced onto LD_SDO by setting malg_sdo_driver_force_en
1	R/W	malg_sdo_driver_force_en	1	Serial Data Out EN Force enable Places value from malg_sdo_driver_force_val on SDO

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Table 9. Reg 03h Reference Path Register

Bit	Type	Name	Default	Description
13:0	R/W	rfp_div_ratio also referred to as 'R'	1	Divides the crystal input by this number 'R' if rfp_div_en=1 and rfp_div_select = 1 rfp_div_ratio = 0 not allowed 2<=div_ratio<=2^14 see Figure 4
14	R/W	rfp_div_select	0	1 = reference divider enabled 0 = bypass ref divider see Figure 4
15	R/W	rfp_auto_refdiv_sel_en	1	1 = auto ref divider enable or bypass is automatic if rfp_div_ratio = 1, bypass divider if rfp_div_bypass ~=1 use divider see Figure 4
16	R/W	rfp_buf_sin_sel	0	Selects sine wave reference for normal operation Also requires Reg1h[8:7]=10 for sine wave reference buffer operation. See Figure 4

Table 10. Reg 04h Prescaler Duty Cycle Register

Bit	Type	Name	Default	Description
0	R/W	vcop_dutycycmode	0	Extends the low time from 30 to 94 VCO cycles for large divide ratios. Program 0.

Table 11. Reg 05h Phase Freq Detector Register (pfd)

Bit	Type	Name	Default	Description
0	R/W	pfd_phase_sel	0	Inverts PFD Polarity 0 = Passive Filter +ve slope VCO 1 = Passive Filter -ve slope VCO 1 = Active inverting filter, +ve slope VCO 0 = Active inverting filter, -ve slope VCO
1	R/W	pfd_upout_en	1	Allows masking of the up outputs between PFD and CP
2	R/W	pfd_dnout_en	1	Allows masking of the dn outputs between PFD and CP

Table 12. Reg 06h Phase Freq Detector Delay Register

Bit	Type	Name	Default	Description
2:0	R/W	pfd_del_sel	2h	Delay line set point to PFD Program 001

Table 13. Reg 07h Charge Pump UP/DN Control Register

Bit	Type	Name	Default	Description
4:0	R/W	cp_UPcurrent_sel	10h	Sets Charge-Pump Up gain, 125uA lsb, binary, 4mA max Program as needed
9:5	R/W	cp_DNcurrent_sel	10h	Sets Charge-Pump Dn gain, 125uA lsb, binary, 4mA max Program as needed

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Table 14. Reg 08h Charge Pump Trim & Offset Register

Bit	Type	Name	Default	Description
3:0	R/W	cp_UPtrim_sel	0	Trim Up gain, 14.3uA lsb, binary, 100uA max Program 0
7:4	R/W	cp_DNtrim_sel	0	Trim Dn gain, 14.3uA lsb, binary, 100uA max Program 0
11:8	R/W	cp_UPoffset_sel	4h	Up Offset leakage current, 28.7uA lsb, binary, 430uA max Program as needed. See Charge Pump Phase Offset section
15:12	R/W	cp_DNoffset_sel	0	Dn Offset leakage current, 28.7uA , binary, 430uAmax Program as needed. See Charge Pump Phase Offset section
17:16	R/W	cp_amp_bias_sel	2h	Charge Pump Dummy Branch Op amp bias selection, 100uA Program 10

Table 15. Reg 09h Charge Pump EN Register

Bit	Type	Name	Default	Description
0	R/W	cp_pull_updn_en	0	Enables CP UP/Down Control Reg09 [1]
1	R/W	cp_pull_dn_upb	0	0 - Forces Charge Pump Up when Reg09[0]=1 1 - Forces Charge Pump DN when Reg09[0]=1

Table 16. Reg 0Ah Reserved

Bit	Type	Name	Default	Description
23:0	R/W	Reserved	304h	Reserved

Table 17. Reg 0Bh Reserved

Bit	Type	Name	Default	Description
23:0	R/W	Reserved	0	Reserved

Table 18. Reg 0Ch Reserved

Bit	Type	Name	Default	Description
23:0	R/W	Reserved	100h	Reserved

Table 19. Reg 0Dh Reserved

Bit	Type	Name	Default	Description
23:0	R/W	Reserved	20h	Reserved

Table 20. Reg 0Eh Reserved

Bit	Type	Name	Default	Description
23:0	R/W	Reserved	0	Reserved

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Table 21. Reg 0Fh Integer Division Register

Bit	Type	Name	Default	Description
15:0	R/W	dsm_intg	C8h	unsigned integer portion of VCO divider value, also known as N_{INT}, see (EQ 12)

Table 22. Reg 10h Fractional Division Register

Bit	Type	Name	Default	Description
23:0	R/W	dsm_frac	0	unsigned fractional portion of VCO divider also known as N_{FRAC}, see (EQ 12)

Table 23. Reg 11h Seed Register

Bit	Type	Name	Default	Description
23:0	R/W	dsm_seed	0	Unsigned seed value for ΔΣ modulator Sets the start phase of the modulator. Use a random , non-repeating number for best results (examples: 3A1953h, DEADBEh, 50894Ch)

Table 24. Reg 12h Delta Sigma Modulator Register

Bit	Type	Name	Default	Description
0	R/W	dsm_ref_clk_select	0	use reference instead of divider Program 0
1	R/W	dsm_invert_clk_sd3	1	invert ΔΣ clk
2	R/W	dsm_invert_clk_rph	0	inverts the ref clock phase
3	R/W	dsm_integer_mode	0	1- enables Integer Mode, bypasses the ΔΣ modulator, leaves it running see also dsm_rstb Reg01h<13> to disable the modulator
4	R/W	Reserved	0	
5	R/W	Reserved	0	
6	R/W	dsm_xref_sin_select	0	when xref is selected specifies that the sine source is used
7	R/W	dsm_autoseed	1	automatic seed load when changing the frac part, uses value in seed
9:8	R/W	dsm_order	2h	Delta-Sigma Modulator configuration: 00-1st order 01-2nd order 10-3rd order Feedback 11-3rd order Feedforward Use either 10 or 11. For Sweeper operation use 11 only. Do not use 1st or 2nd order (for test only)
13:10	R/W	dsm_quant_max	3h	max value allowed out of ΔΣ modulator quantizer limits are +7 to -8, typ ±3 or ±4 Program 3h
17:14	R/W	dsm_quant_min	Ch	min value allowed out of ΔΣ modulator quantizer limits are +7 to -8, typ ±3 or ±4 Program Ch

[1] Phase-Error Measurement and Compensation in PLL Frequency Synthesizers for FMCW, Sensors—I: Context and Application, Pichler, Stelzer, Member, IEEE, Seisenberger, and Vossiek, IEEE Transactions on Circuits and Systems—I, VOL. 54, No. 5, May 2007

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Table 25. Reg 14h CW Sweep Control Register

The maximum sweep range is limited to 510 x Fxtal/R. Delta-Sigma Modulator mode should be Feed Forward when using Sweep feature (Register 12h Bits [9:8] = 11.

Bit	Type	Name	Default	Description
0	R/W	clear_ovf_undf	0	asynchronous clear for ovf/undf flags
1	R/W	ramp_enable	0	Ramp En/rstb 1= enables the CW Ramp Function
2	R/W	ramp_trigg	0	Write always triggers ramps if bit <2> = 0, if bit <2> = 1, Ramp will not trigger, bit <2> must be reset to 0 first
3	R/W	ramp_repeat_en	0	Ramp Repeat Seq enable 1= enables autotrigger of ramps 0 = ramp_trigg starts each ramp
4	R/W	ramp_startdir_dn	0	Ramp start direction 1= Start with Ramp Down 0= Start with Ramp Up
5	R/W	ramp_trig_ext_en	0	Enable hardware trigger on GPO3 pin
6	R/W	ramp_singlestep	0	Ramp single step, advances the ramp to the next step, and holds frequency
7	R/W	ramp_singledir	0	Ramps in one direction only with hop to start at end of ramp

Table 26. Reg 15h CW Sweep Ramp Step Register

The maximum sweep range is limited to 510 x Fxtal/R. Delta-Sigma Modulator mode should be Feed Forward when using Sweep feature (Register 12h Bits [9:8] = 11.

Bit	Type	Name	Default	Description
23:0	R/W	ramp_step	800h	Ramp Step size

Table 27. Reg 16h CW Sweep Ramp Step Number Register

The maximum sweep range is limited to 510 x Fxtal/R. Delta-Sigma Modulator mode should be Feed Forward when using Sweep feature (Register 12h Bits [9:8] = 11.

Bit	Type	Name	Default	Description
23:0	R/W	ramp_steps_number	800h	Ramp Number of steps in ramp

Table 28. Reg 17h CW Sweep Dwell Time Register

Bit	Type	Name	Default	Description
23:0	R/W	ramp_dwell_time	800h	Ramp Number of cycles to hold at top/bottom in repeat mode

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Table 29. Reg 18h Auxiliary Oscillator Register 1

Bit	Type	Name	Default	Description
1:0	R/W	dsmclk_auxclk_insel	0	Selects the input clk for auxclk Program 0 0:vcodiv Recommended 1:xrefsq or sin 2:refdiv 3:ring oscillator from mono, est 300 MHz to 1 GHz
3:2	R/W	dsmclk_auxclk_modesel	0	Program 0 0: bypass-no delay 1: pass through w/ delay 2: ring-out constant 3: ring-out seeded/gated
6:4	R/W	dsmclk_auxclk_divsel	2h	divider selection auxclk value divby Program 010 000 1 001 2 010 4 011 6 100 8 101 10 110 12 111 14
7	R/W	dsmclk_auxclk_sel	1	selects auxclk (if=1) as natural reference clk input of sigma delta Program 1
8	R/W	dsmclk_auxmod_lfsr_en	0	enables 10-bit lfsr inside the delay modulator (clocked by auxclk or auxclkb) Program 0
9	R/W	dsmclk_auxmod_accum_en	0	enables 8-bit accumulator inside the delay modulator (clocked by auxclk or auxclkb) Program 0
11:10	R/W	dsmclk_auxmod_mode	0	delay modulation mode Program 0 0: auxmod_lodly_in passthrough 1: accumulator based square-wave 2: lfsr (lo-amp) 3: lfsr (hi-amp)
19:12	R/W	dsmclk_auxmod_fracstep	0	step-size of accumulator (changes square-wave value once it wraps through 256) Program 0
22:20	R/W	dsmclk_auxmod_lodly	0	value of delay-element (when auxmod_mode=0) or low value used during sq-wave modulation Program 0

Table 30. Reg 19h Auxiliary Oscillator Register 2

Bit	Type	Name	Default	Description
2:0	R/W	dsmclk_auxmod_hidly	7h	high value of delay element during sq-wave modulation. Program 7h
3	R/W	dsmclk_auxmod_clkinv	1	optionally inverts auxclk as used by the modulator. Program 1
4	R/W	dsmclk_auxmod_clkwring	0	select LKD ringosc to clock the LFSR. Program 0

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Table 31. Reg 1Ah Lock Detect Register

Bit	Type	Name	Default	Description
9:0	R/W	lkd_wincnt_max	40h	threshold count in the timer window to declare lock (reference cycles)
10	R/W	lkd_win_asym_enable	0	Enables asymmetric lock detect window (nominal 10nsec)
11	R/W	lkd_win_asym_up_select	0	Sets polarity of the window
12	R/W	lkd_to_sdo_automux_en	1	Muxes the lkd output signal to SDO when SDO is not being used for Main Serial Port Data Outputs (Read Operation)
13	R/W	lkd_to_sdo_always	0	Muxes the lkd output signal to SDO always, not possible to do Main Serial Port Read in this state
14	R/W	lkd_ringosc_mono_select	0	1 select ringosc based oneshot for lock detect window 0 selects analog based oneshot
16:15	R/W	lkd_ringosc_cfg	0	“00” fastest “11” slowest
18:17	R/W	lkd_monost_duration	0	“00” shortest “11” longest
19	R/W	lkd_ringosc_testmode	0	enables the ring osc by itself for testing

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Table 32. Reg 1Bh GPO Control Register

Bit	Type	Name	Default	Description
3:0	R/W	gpo_sel	0	Selects data to be driven on GPO ports
		gpo_sel<3:0> = 0000		GPO3 <=gposel_0_data<2> GPO2 <= gposel_0_data<1> GPO1 <= gposel_0_data<0>
		gpo_sel<3:0> = 0001		GPO3 <= xref_clk_in GPO2 <= ref_clk_in GPO1 <= vco_div_clkin
		gpo_sel<3:0> = 0010		GP03 <= pfd_up_in GP02 <= pfd_dn_in GP01 <= LKD_monost_window
		gpo_sel<3:0> = 0011		GP03 <= pfd_sat_ref_in GP02 <= pfd_sat_vco_div_in GP01 <= delta_integer_cycslip_sel, this strobe holds the gain of the PFD at max for anti-cycle slipping
		gpo_sel<3:0> = 0100		GP03 <= xref_clk_in GP02 <= xref_sin_in GP01 <= sd_frac_strobe_sync, internally synchronized frac strobe
		gpo_sel<3:0> = 0101		Reserved
		gpo_sel<3:0> = 0110		GP03 <= SD_Intz1<1> GP02 <=SD_Intz1<2> GP01 <= SD_Intz1<3> 3-bit quantized version of the VCO phase
		gpo_sel<3:0> = 0111		GP03 <= aux_clk GP02 <= ringosc_test GP01 <= clk_SD
		gpo_sel<3:0> = 1000		GP03 <= 00 GP02 <= ramp_busy GP01 <= Reserved
		gpo_sel<3:0> = 1001		Not used
		gpo_sel<3:0> = 1010		GP03 <= ΔΣ Quantizer Output 3rd lsb GP02 <= ΔΣ Quantizer Output 2nd lsb GP01 <= ΔΣ Quantizer Output lsb
6:4	R/W	gpo_sel_0_data	0	this data is driven on gpo if gpo_sel==0
7	R/W	gpo_dig_drive_en	0	enables Tri-state drivers on GPO output pads
10:8	R/W	gpo_ind_drive_dis	000	000 = all GPO pad drivers enabled xx1 = disable GPO1 pad driver x1x = disable GPO2 pad driver 1xx = disable GPO3 pad driver

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Table 33. Reg 1Ch Phase Detector CSP Register

Bit	Type	Name	Default	Description
3:0	R/W	pfds_sat_deltaN	0	0= Cycle Slip Prevention (CSP) disabled 4-bit value to advance or retard phase detector in VCO cycles if it reaches 2pi , i.e. cycle slip prevention. 1st bit is polarity, enabled by rstb
4	R/W	pfds_rstb_force	0	CSP PFD Flip-flops RSTB: 1 - controlled by the pfds_rstb bit: 0 - auto-controlled by the CSP logic Forces the PFD into reset, which tri-states charge pump, freezes charge on the loop filter, and hence opens the loop. Program 0
5	R/W	pfds_rstb	1	CSP PFD FF rstb 1 - Enables the Cycle Slip Prevention (CSP) feature of the PFD (also need Reg 1[15]=1)

Table 34. Reg 1Dh Reserved

Bit	Type	Name	Default	Description
23:0	RO	Reserved	0	Reserved

Table 35. Reg 1Eh Temperature Sensor Register

Bit	Type	Name	Default	Description
0	R/W	tsens_spi_enable	0	Enable the temperature sensor, draws ~2mA current, must strobe tsens_spi_strobe Reg 00h <3>

Table 36. Reg 1Fh LD, VCO & Ramp Busy Read Only Register

Bit	Type	Name	Default	Description
0	RO	ro_lock_detect	0	1 = locked, 0 = unlocked
3:1	RO	ro_dsm_overflow	0	1 = modulator overflow
4	RO	Reserved	0	Reserved
5	RO	ro_ramp_busy	0	Sweeper status flag, set when ramp is busy, cleared when at end of ramp or not used

Table 37. Reg 20h Reserved

Bit	Type	Name	Default	Description
23:0	RO	Reserved	20h	Reserved

Table 38. Reg 21h Temperature Sensor Read Only Register

Bit	Type	Name	Default	Description
6:0	RO	tsens_temperature	1Fh	Current Temperature from temp sensor lsb = 17.5°C 0000111 = Temp >= 82.5°C 0000110 = Temp 0000000 = Temp <=-22.5°C tsens_temperature = floor ((Temp+40)/17.5)

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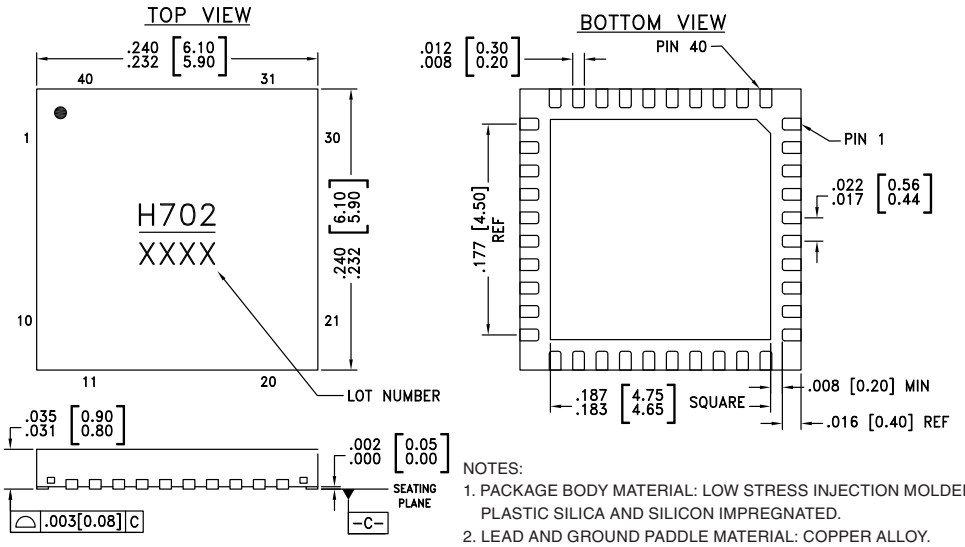
Table 39. Reg 22h Reserved

Bit	Type	Name	Default	Description
23:0	RO	Reserved	0	Reserved

Outline Drawing



NOTES:
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
9. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC702LP6CE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H702 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

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14 GHz 16-BIT FRACTIONAL-N PLL

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