13 Gbps, Fast Rise Time XOR/XNOR Gate with Programmable Output Voltage and Positive Supply

Data Sheet **HMC745**

FEATURES

- Inputs terminated internally at 50 Ω
- Differential and single-ended operation
- Fast rise and fall times: 21 ps and 19 ps
- Low power consumption: 240 mW (typical)
- Programmable differential
- Output voltage swing: 600 mV to 1200 mV
- Propagation delay: 95 ps
- Single supply: 3.3 V
- 16-terminal, ceramic 3 mm × 3 mm LCC package

APPLICATIONS

- RF automatic test equipment (ATE) applications
- Broadband test and measurement
- Serial data transmission up to 13 Gbps
- Digital logic systems up to 13 GHz

FUNCTIONAL BLOCK DIAGRAM

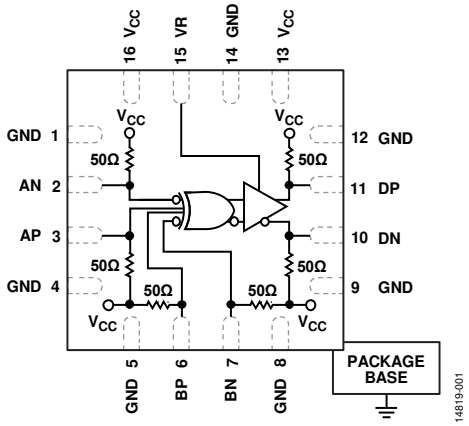


Figure 1.

GENERAL DESCRIPTION

The HMC745 is a XOR/XNOR gate function designed to support data transmission rates of up to 13 Gbps, and clock frequencies as high as 13 GHz. The HMC745 also features an output level control pin, VR, which permits loss compensation or signal level optimization.

All input and output signals to the HMC745 are terminated with 50 Ω to V_{CC} on-chip, and can be either ac-coupled or dc-coupled.

Inputs or outputs can be connected directly to a 50 Ω V_{CC} terminated system, while dc blocking capacitors may be used if the terminating system is 50 Ω to ground. The HMC745 operates from a single 3.3 V dc supply, and is available in a ceramic, RoHS compliant, 3 mm × 3 mm LCC package.

Rev. D
Document Feedback

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REVISION HISTORY

6/2018—Rev. C to Rev. D

Changes to Power Supply Voltage Parameter, Table 1 3
Changes to Input Signals Parameter and Output Signals Parameter, Table 2 4
Changes to Pin 14, Pin No. Column, Table 3 5
Change to Figure 19 10
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10/2017—Rev. 02.0514 to Rev. C

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

Updated Format ..... Universal
Change to Features Section, General Description Section, and Figure 1 Caption 1
Changes to Table 2 4
Changes to Figure 2 Caption 5
Deleted Figure 7; Renumbered Sequentially 5
Changes to Theory of Operation Section 8
Changes to Evaluation Printed Circuit Board (PCB) Section 9
Changes to Figure 18 Caption 10
Changes to Figure 19 Caption 11
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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C and V_{CC} = 3.3 V, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY VOLTAGE					
Voltage		3.0	3.3	3.6	V
Current			72		mA
MAXIMUM DATA RATE			13		Gbps
MAXIMUM CLOCK RATE			13		GHz
INPUT VOLTAGE					
High		2.8		3.8	V
Low		2.1		3.3	V
INPUT RETURN LOSS	Frequency < 13 GHz		10		dB
OUTPUT AMPLITUDE					
Single-Ended			550		mV p-p
Differential			1100		mV p-p
OUTPUT VOLTAGE					
High			3.25		V
Low			2		V
OUTPUT	Differential, 20 % to 80 %				
Rise Time			21		ps
Fall Time			19		ps
OUTPUT RETURN LOSS	Frequency < 13 GHz		10		dB
SMALL SIGNAL GAIN			27		dB
JITTER					
Random, J_R				0.2	ps, rms
Deterministic, J_D	$2^{15} - 1$ PRBS input[1]		2		ps p-p
PROPAGATION DELAY, t_D			95		ps

[1] Deterministic jitter is calculated by simultaneously measuring the jitter of a 300 mV input, 13 GHz input, a $2^{15} - 1$ PRBS input, and a single-ended output.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Power Supply Voltage (V_{CC})	V_{CC} – 0.5 V to 3.75 V
Input Signals	V_{CC} – 2 V to V_{CC} + 0.5 V
Output Signals	V_{CC} – 1.5 V to V_{CC} + 0.5 V
Continuous Power Dissipation, P_{DISS} (T_A = 85°C, Derate 17 mW/°C Above 85°C)	0.68 W
Thermal Resistance (R_{TH-JP}), Worst Case Junction to Package Pad	59°C/W
Maximum Junction Temperature	125°C
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +85°C
Electrostatic Discharge (ESD) Sensitivity Human Body Model (HBM)	Class 1C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

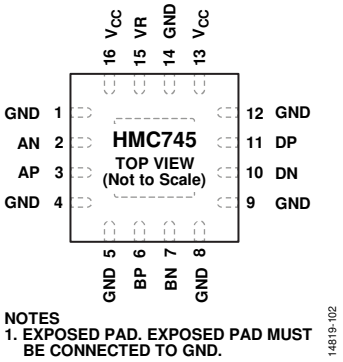


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 5, 8, 9, 12	GND	Signal Ground.
2, 3	AN, AP	Clock/Data Input A.
6, 7	BP, BN	Clock/Data Input B.
10, 11	DN, DP	Clock/Data Output.
13, 16	V_{CC}	Positive Supply.
14	GND	Supply Ground.
15	VR	Output Level Control. Output level can be adjusted by applying a voltage to VR per Figure 10.
	EPAD	Exposed Pad. Exposed pad must be connected to GND.

INTERFACE SCHEMATICS



Figure 3. GND Interface Schematic

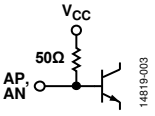


Figure 4. AN, AP Interface Schematic

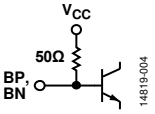


Figure 5. BP, BN Interface Schematic

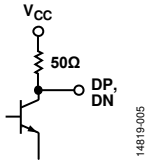


Figure 6. DN, DP Interface Schematic

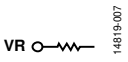


Figure 7. VR Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

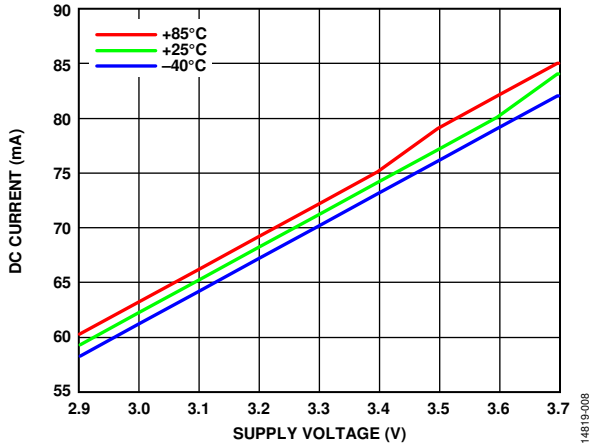


Figure 8. DC Current vs. Supply Voltage, VR = 3.3 V, Frequency = 13 GHz

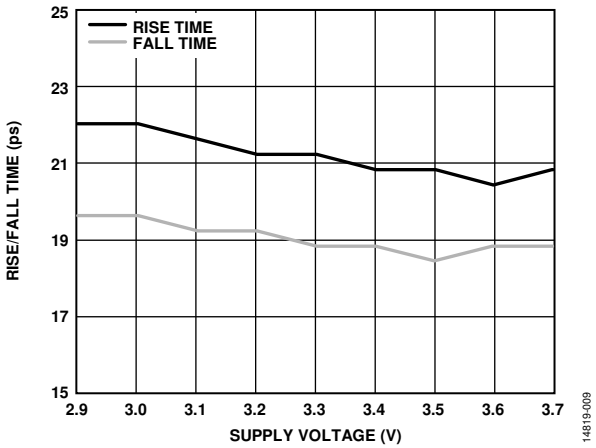


Figure 9. Rise/Fall Time vs. Supply Voltage, Frequency = 13 GHz

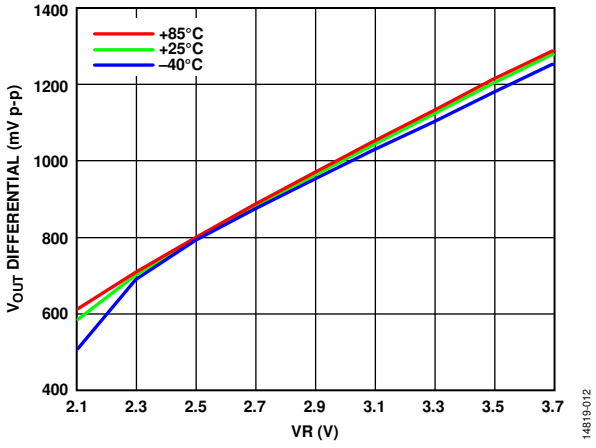


Figure 10. Output Voltage (V_{OUT}) Differential vs. VR, Frequency = 13 GHz

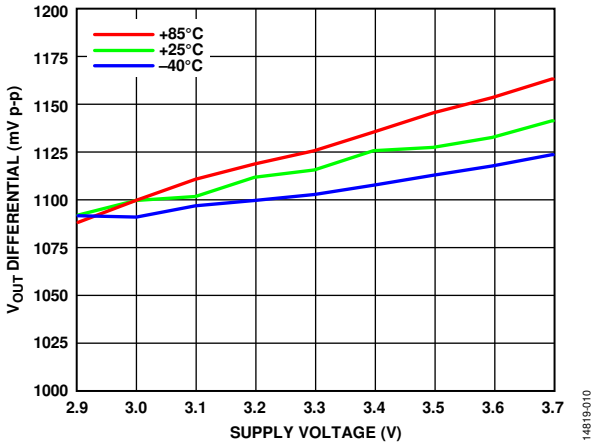


Figure 11. Output Voltage (V_{OUT}) Differential vs. Supply Voltage, VR = 3.3 V, Frequency = 13 GHz

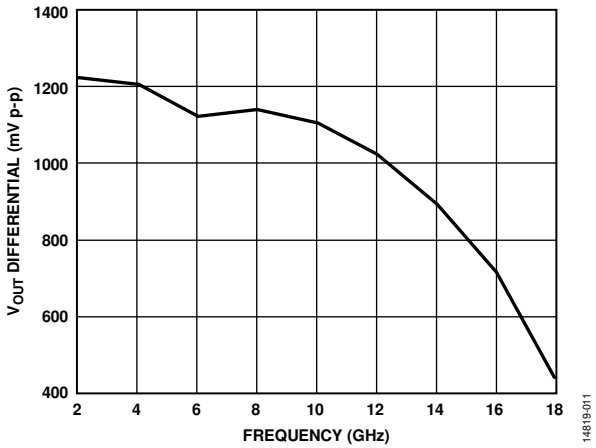


Figure 12. Output Voltage (V_{OUT}) Differential vs. Frequency, VR = 3.3 V

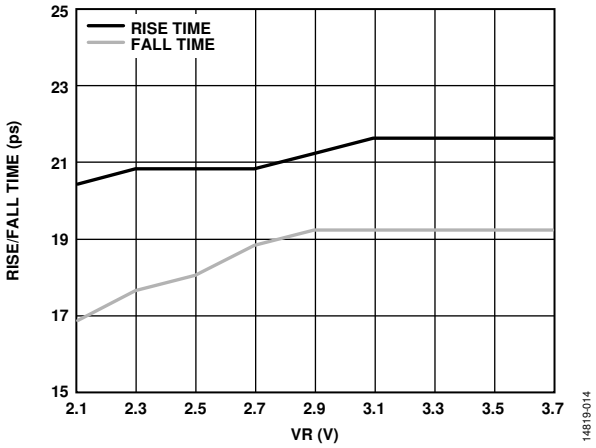


Figure 13. Rise/Fall Time vs. VR, Frequency = 13 GHz

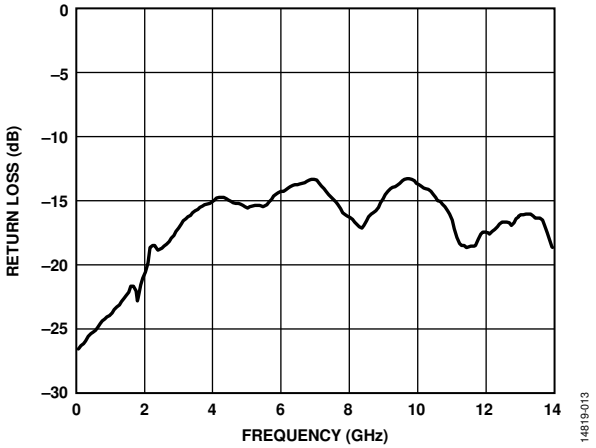


Figure 14. Input Return Loss vs. Frequency

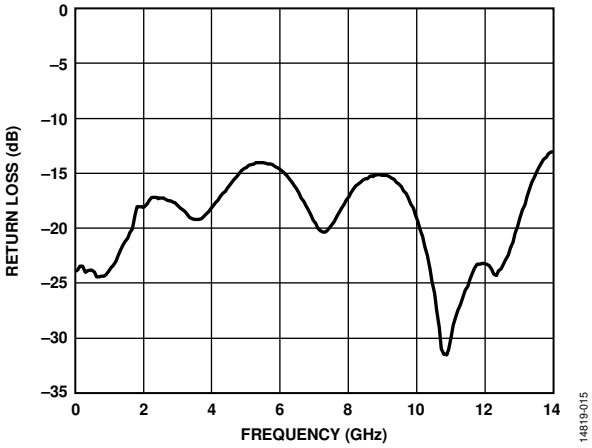


Figure 16. Output Return Loss vs. Frequency

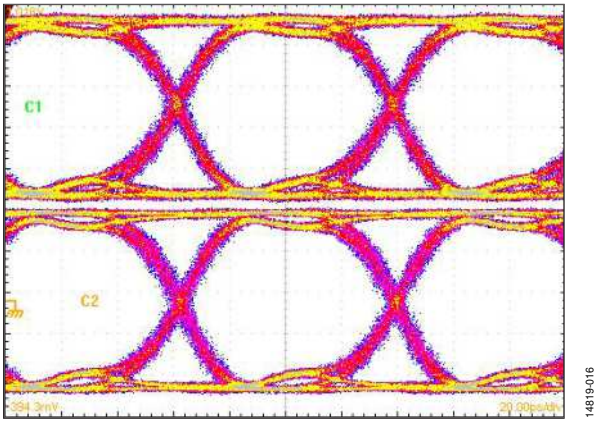


Figure 15. Eye Diagram, Waveform Generated with an Agilent N4903A J-Bert, Rate = 13 Gbps, Eye Diagram Data Presented on a Tektronix CSA 8000, Device is AC-Coupled to Scope

THEORY OF OPERATION

The HMC745 consists of an XOR/XNOR stage followed by an output driver stage. The XOR/XNOR stage accepts two differential input pairs; AN/AP and BN/BP, and gives one differential output. The following output driving stage drives the line with a 50 Ω single-ended or 100 Ω differential. The output stage has a tunable voltage swing feature that allows the tune to swing between 600 mV p-p to 1200 mV p–p. All input and output interfaces are referenced to 3.3 V with a 50 Ω resistor.

APPLICATIONS INFORMATION

Table 4 is the truth table, and Figure 17 is the timing diagram.

Table 4. Truth Table

Input[1]		Outputs[1]
A	B	D
L	L	L
L	H	H
H	L	H
H	H	L

[1] A = AP – AN, B = BP – BN, D = DP – DN, H is the positive voltage level, and L is the negative voltage level.

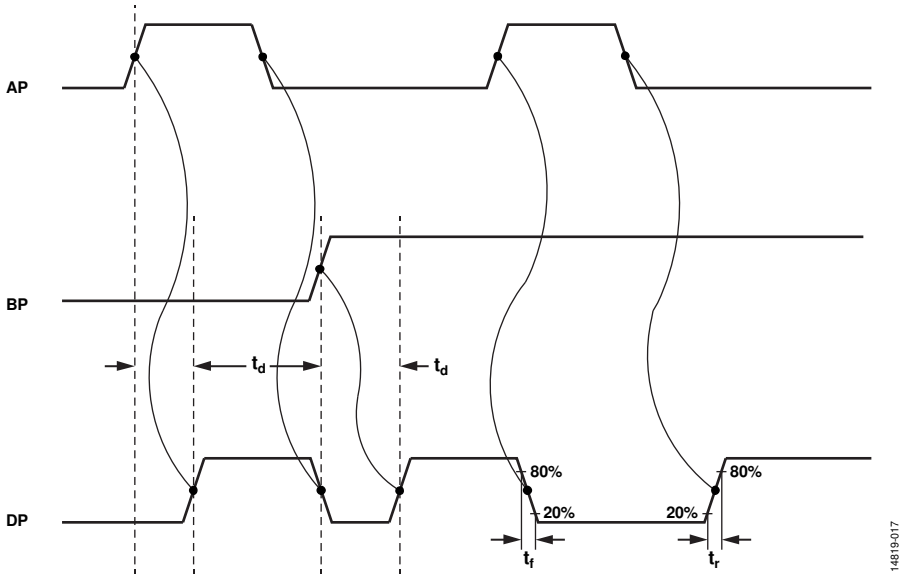


Figure 17. Timing Diagram

EVALUATION PRINTED CIRCUIT BOARD (PCB)

The circuit board used in the application must use RF circuit design techniques. Signal lines must have 50 Ω impedance while the package ground leads must be connected directly to the ground plane. The exposed package base must be connected to GND. A sufficient number of via holes must be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Analog Devices, Inc., upon request.

Table 5. Connector Description

Item	Description
J1	AN
J2	AP
J3	BP
J4	BN
J5	DN
J6	DP
J7	GND
J8	VR
J9	V_{CC}

Table 6. List of Materials for Evaluation PCB 122517[1]

Item	Description
J1 to J6	PCB mount SMA RF connectors
J7 to J9	DC pin
JP1	Shorting jumper
C1, C2	4.7 µF capacitor, tantalum
C3 to C5	100 pF capacitor, 0402 package
R2	10 Ω resistor, 0603 package
U1	HMC745LC3, high speed logic, XOR/XNOR
PCB[2]	122515 evaluation board

[1] Reference this number when ordering complete evaluation PCB.
[2] The circuit board material is Arlon 25FR.

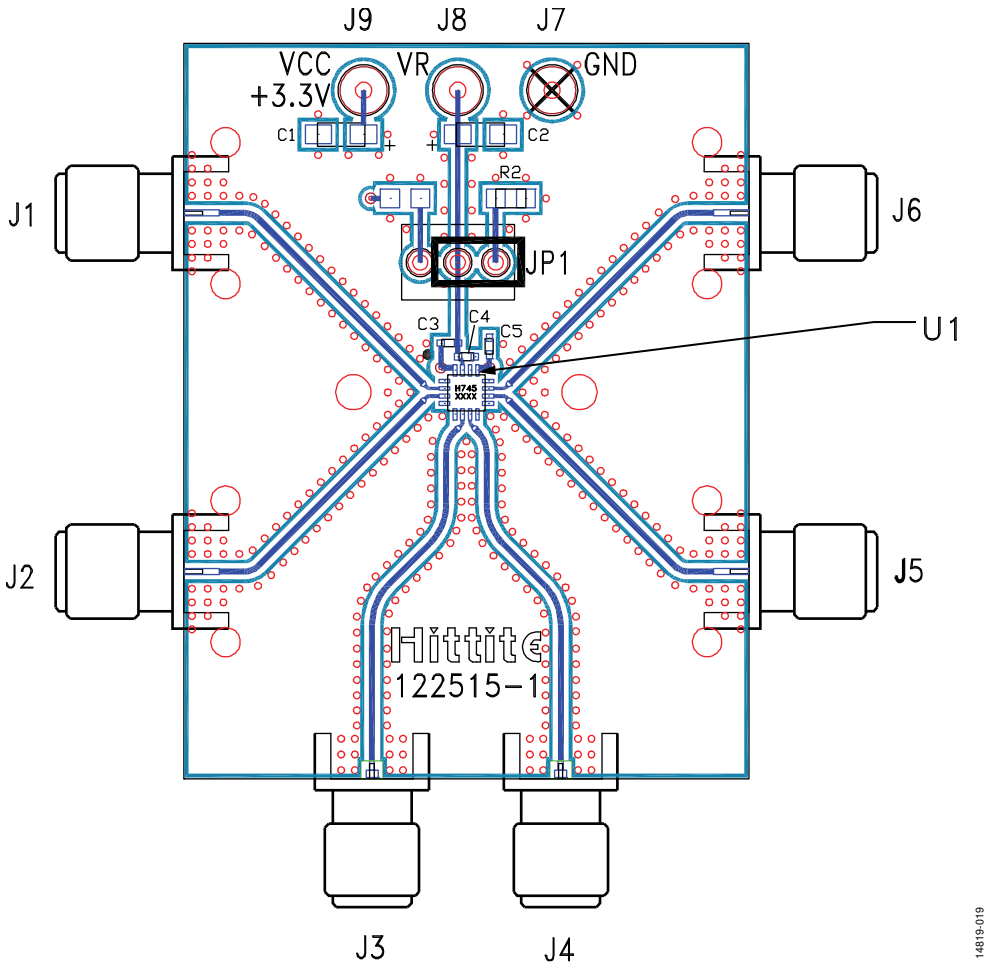


Figure 18. Evaluation Board

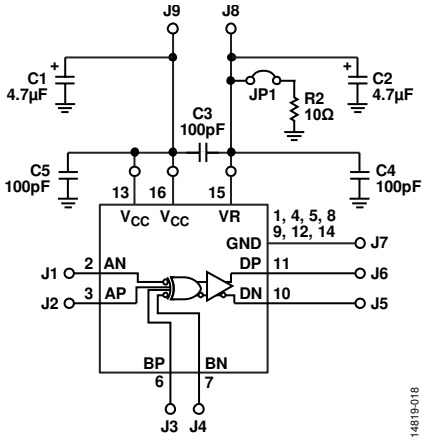


Figure 19. Evaluation Board Schematic

OUTLINE DIMENSIONS

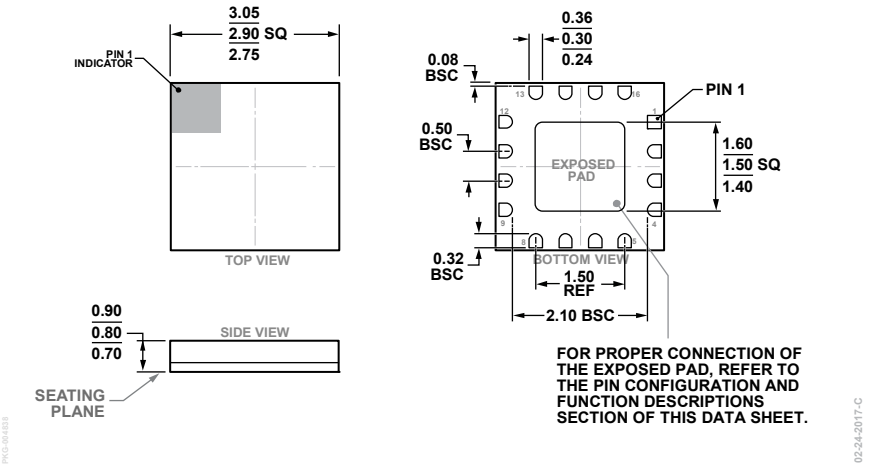


Figure 20. 16-Terminal Ceramic Leadless Chip Carrier [LCC]
(E-16-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	MSL Rating[2]	Temperature Range	Package Description	Package Option
HMC745LC3	MSL3	−40°C to +85°C	16-Terminal Ceramic Leadless Chip Carrier [LCC]	E-16-1
HMC745LC3TR	MSL3	−40°C to +85°C	16-Terminal Ceramic Leadless Chip Carrier [LCC]	E-16-1
HMC745LC3TR-R5	MSL3	−40°C to +85°C	16-Terminal Ceramic Leadless Chip Carrier [LCC]	E-16-1
122517-HMC745LC3			Evaluation Board	

[1] All models are RoHS compliant.
[2] Maximum peak reflow temperature of 260°C.

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